



9N95-E

Advance

Power MOSFET

9A, 950V N-CHANNEL POWER MOSFET

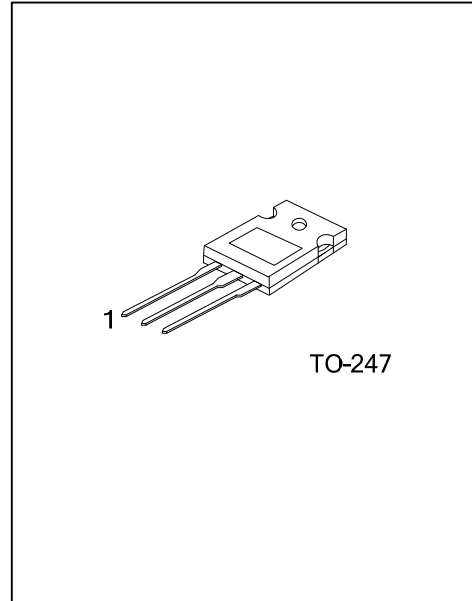
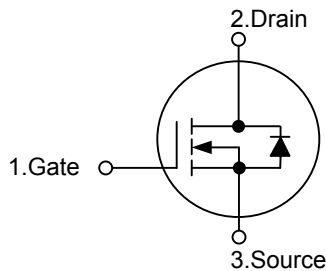
DESCRIPTION

The UTC **9N95-E** uses UTC's advanced proprietary, planar stripe, DMOS technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with low gate voltages. This device is suitable for use as a load switch or in PWM applications.

FEATURES

- * $R_{DS(ON)} \leq 1.4\Omega$ @ $V_{GS}=10V, I_D=4.5A$
- * Ultra Low Gate Charge (Typical 45 nC)
- * Low Reverse Transfer Capacitance ($C_{RSS} =$ Typical 14 pF)
- * Fast Switching Capability
- * Avalanche Energy Specified
- * Improved dv/dt Capability, High Ruggedness

SYMBOL



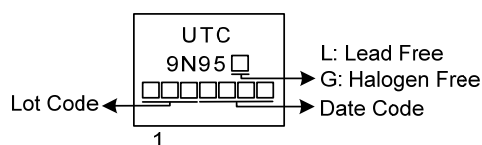
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
9N95L-T47-T	9N95G-T47-T	TO-247	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>9N95G-T47-T</p>	<p>(1) T: Tube (2) T47: TO-247 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATING ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DSS}	950	V
Gate-Source Voltage	V_{GSS}	± 30	V
Continuous Drain Current ($T_C = 25^\circ\text{C}$)	I_D	9.0	A
Pulsed Drain Current (Note 2)	I_{DM}	36	A
Avalanche Current (Note 2)	I_{AR}	9.0	A
Avalanche Energy	Single Pulsed(Note 3)	E_{AS}	900
	Repetitive(Note 2)	E_{AR}	28
Peak Diode Recovery dv/dt (Note 4)	dv/dt	4.0	V/ns
Power Dissipation	P_D	147	W
Linear Derating Factor above $T_C = 25^\circ\text{C}$		1.176	W/ $^\circ\text{C}$
Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by maximum junction temperature.

3. $L = 21\text{mH}$, $I_{AS} = 9.0\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 9.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	0.85	$^\circ\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

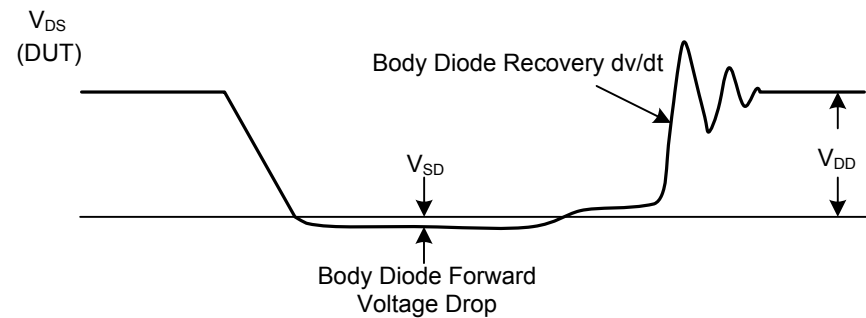
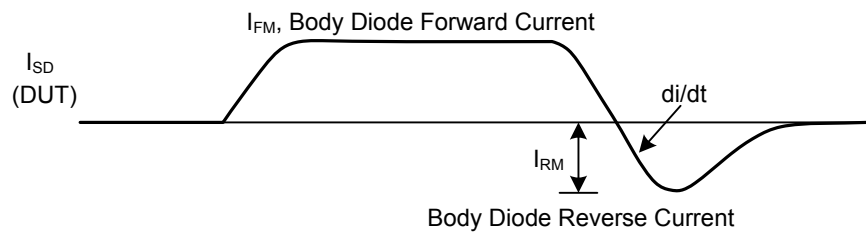
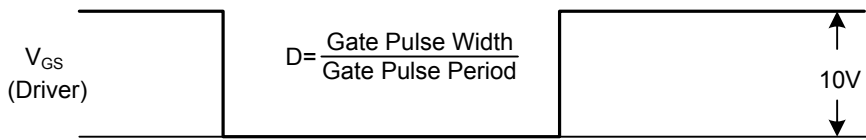
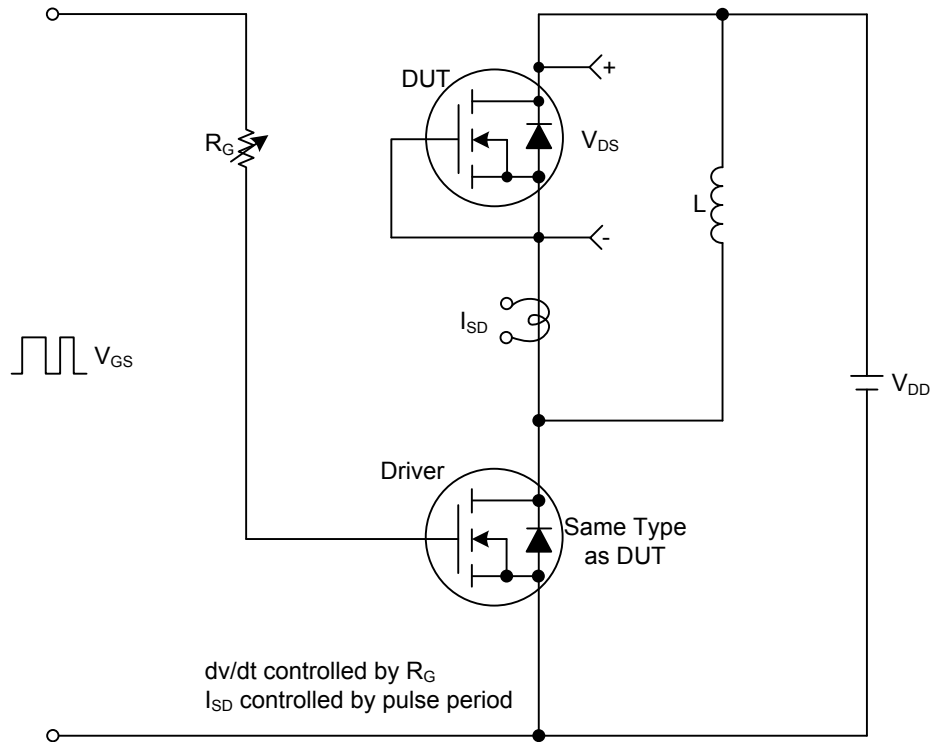
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	950			V	
Drain-Source Leakage Current	I _{DSS}	V _{DS} =950V, V _{GS} =0V			10	μA	
Gate-Body Leakage Current	Forward	I _{GSSF}	V _{GS} =30V, V _{DS} =0V			100	nA
	Reverse	I _{GSSR}	V _{GS} =-30V, V _{DS} =0V			-100	nA
Breakdown Voltage Temperature Coefficient	ΔBV _{DSS} /ΔT _J	I _D =250μA, Referenced to 25°C		0.99		V/°C	
ON CHARACTERISTICS							
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	3.0		5.0	V	
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =4.5A		1.05	1.4	Ω	
DYNAMIC PARAMETERS							
Input Capacitance	C _{ISS}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz		2100	2730	pF	
Output Capacitance	C _{OSS}			175	230	pF	
Reverse Transfer Capacitance	C _{RSS}			14	18	pF	
SWITCHING CHARACTERISTICS							
Total Gate Charge	Q _G	V _{DS} =760V, I _D =11A, V _{GS} =10V (Note1,2)		45	58	nC	
Gate-Source Charge	Q _{GS}			13		nC	
Gate-Drain Charge	Q _{GD}			18		nC	
Turn-On Delay Time	t _{D(ON)}	V _{DD} =475V, I _D =11.0A, R _G =25Ω (Note1,2)		50	110	ns	
Turn-On Rise Time	t _R			120	250	ns	
Turn-Off Delay Time	t _{D(OFF)}			100	210	ns	
Turn-Off Fall Time	t _F			75	160	ns	
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
Maximum Continuous Drain-Source Diode Forward Current	I _S				9.0	A	
Maximum Pulsed Drain-Source Diode Forward Current	I _{SM}				36	A	
Drain-Source Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =9.0A			1.4	V	
Reverse Recovery Time	t _{rr}	V _{GS} =0V, I _S =9.0A,		550		ns	
Reverse Recovery Charge	Q _{rr}	dI _F /dt=100A/μs(Note1)		6.5		μC	

Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.

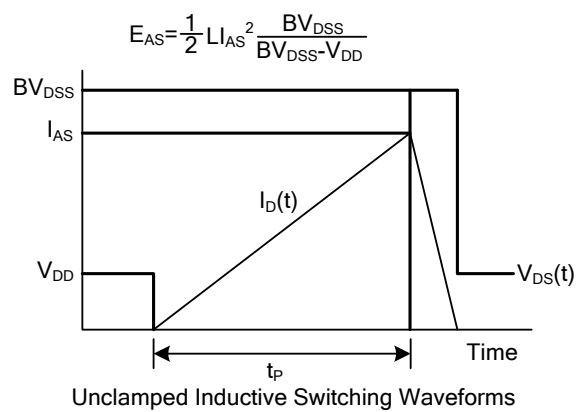
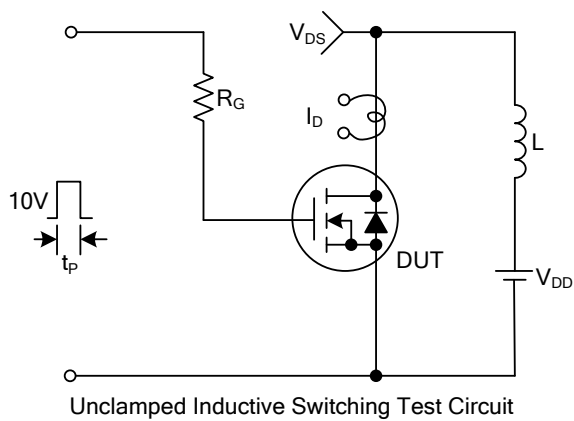
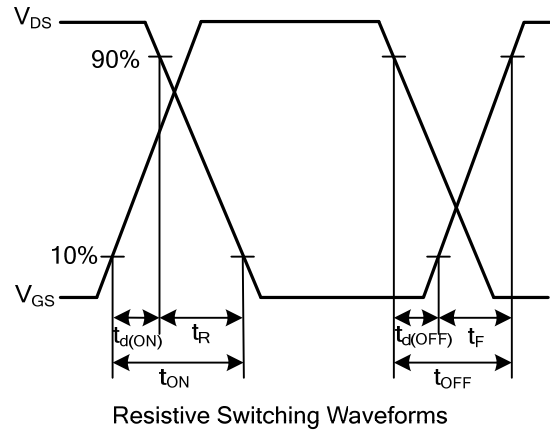
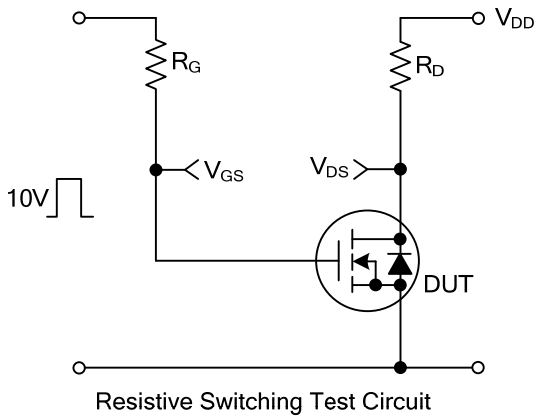
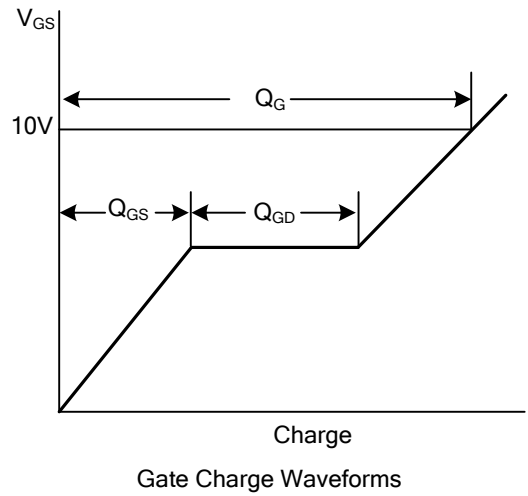
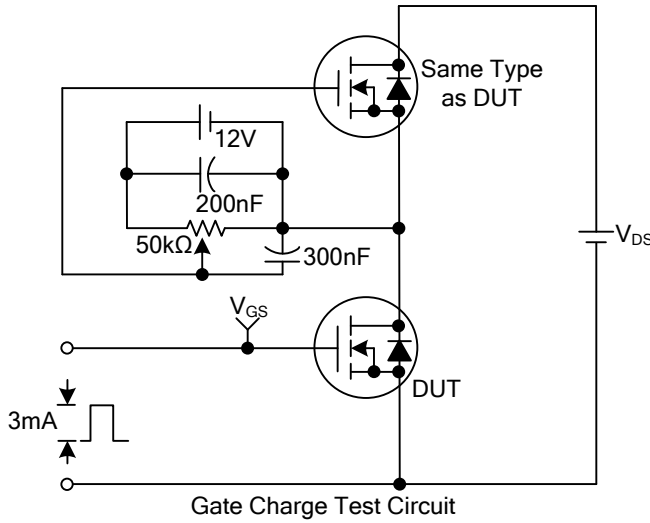
2. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

Peak Diode Recovery dv/dt Test Circuit & Waveforms



■ TEST CIRCUITS AND WAVEFORMS



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