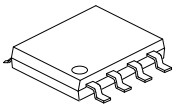
UD12N04Z **Advance** ***POWER MOSFET***

6A, 40V DUAL N-CHANNEL ENHANCEMENT MODE TRENCH POWER MOSFET



SOP-8

■ DESCRIPTION

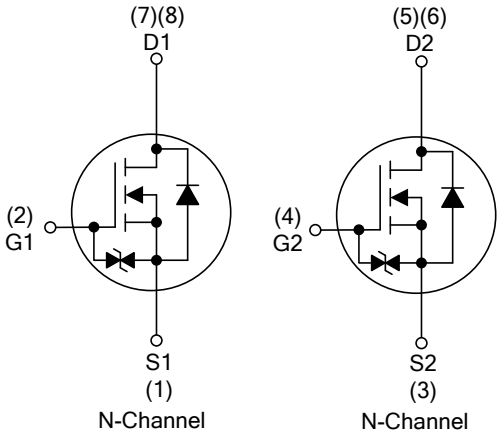
The UTC **UD12N04Z** is a Dual N-channel enhancement mode power MOSFET using UTC's advanced technology to provide customers with an extremely low on-state resistance and superior switching performance.

The UTC **UD12N04Z** is suitable for high frequency DC-DC converters with synchronous rectification applications.

■ FEATURES

* $R_{DS(ON)}$ ≤ 38 mΩ @ V_{GS}=10V, I_D=6.0A
  $R_{DS(ON)}$ ≤ 50 mΩ @ V_{GS}=4.5V, I_D=6.0A
* High Power and Current Handling Capability
* High Cell Density Trench Technology

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UD12N04ZL-S08-R	UD12N04ZG-S08-R	SOP-8	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel

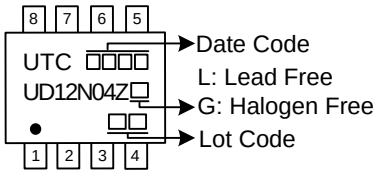
Note: Pin Assignment: G: Gate D: Drain S: Source

UD12N04ZG-S08-R

(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) S08: SOP-8
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING


8
7
6
5
UTC
UD12N04Z
1
2
3
4
Date Code
L: Lead Free
G: Halogen Free
Lot Code

■ ABSOLUTE MAXIMUM RATINGS (T_A=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	40	V
Gate-Source Voltage		V_{GSS}	±12	V
Continuous Drain Current	Continuous	I_D	6	A
Pulsed Drain Current	Pulsed (Note 2)	I_{DM}	12	A
Avalanche Current (Note 3)		I_{AS}	12	A
Avalanche energy	Single Pulsed (Note 3)	E_{AS}	1.08	mJ
Power Dissipation (Note 4)		P_D	1.47	W
Junction Temperature		T_J	+150	°C
Storage Temperature Range		T_{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature.
3. L=10μH, I_{AS}=12A, V_{DD}=20V, R_G=25Ω, Starting T_J = 25°C.
4. Mounted on a ceramic board.

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	85	°C/W

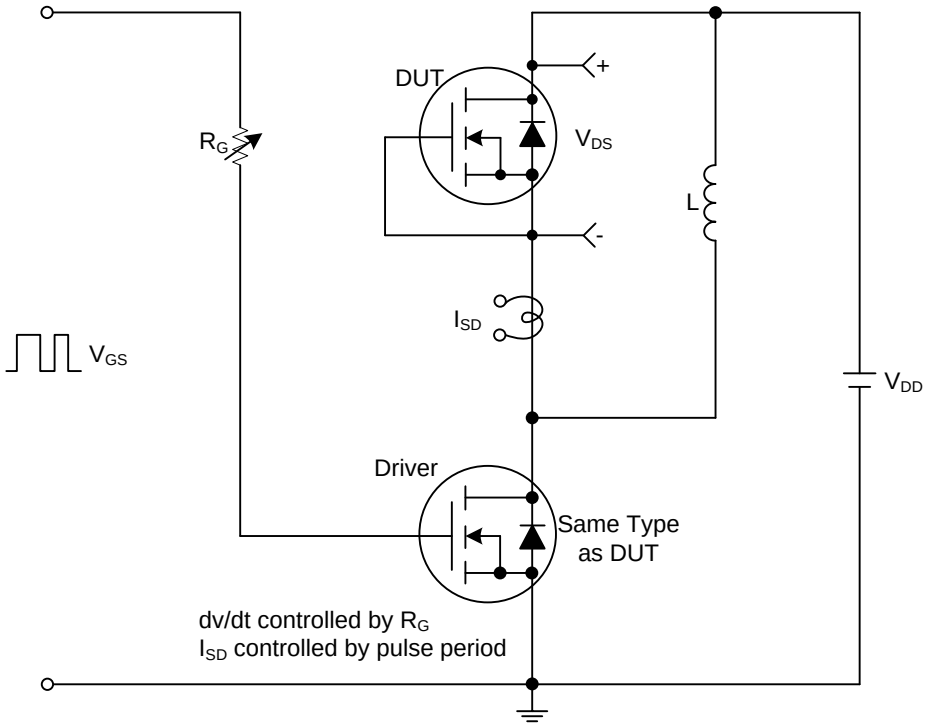
Note: Mounted on a ceramic board.

■ ELECTRICAL CHARACTERISTICS (T_A =25°C, unless otherwise specified)

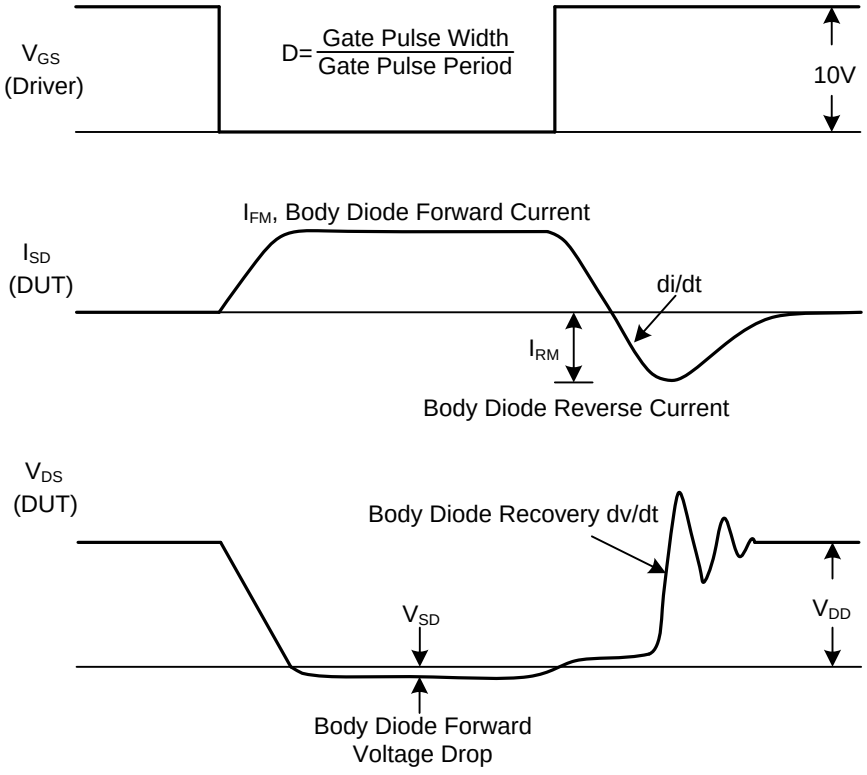
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	I_D=250μA, V_{GS}=0V	40			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=40V, V_{GS}=0V			1	μA
Gate-Source Leakage Current	Forward	I_{GSS}	V_{GS}=+12V, V_{DS}=0V			+10	μA
	Reverse		V_{GS}=-12V, V_{DS}=0V			-10	μA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	1.0		2.5	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=6.0A			38	mΩ
			V_{GS}=4.5V, I_D=6.0A			50	mΩ
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I_S				1.6	A
Maximum Body-Diode Pulsed Current		I_{SM}				12	A
Drain-Source Diode Forward Voltage (Note 1)		V_{SD}	I_S=6.0A, V_{GS}=0V			1.2	V

Notes: 1. Pulse Test: Pulse width ≤ 10μs, Duty cycle ≤ 1%.
2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



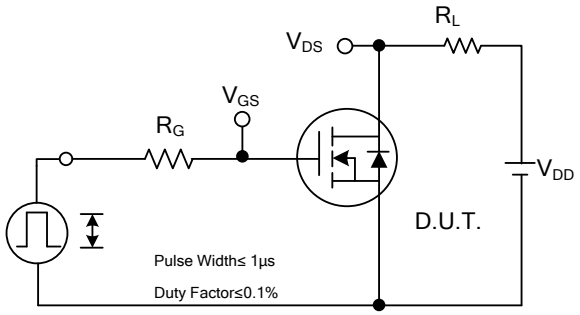
Peak Diode Recovery dv/dt Test Circuit



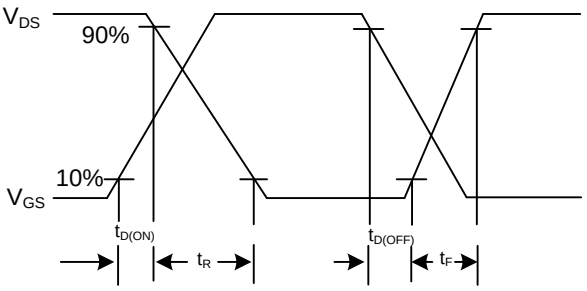
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

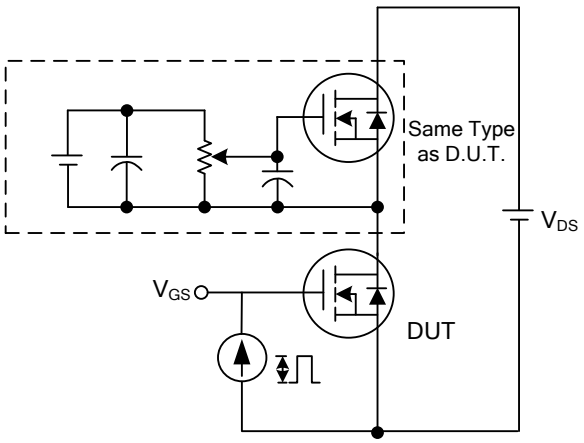
■ TEST CIRCUITS AND WAVEFORMS



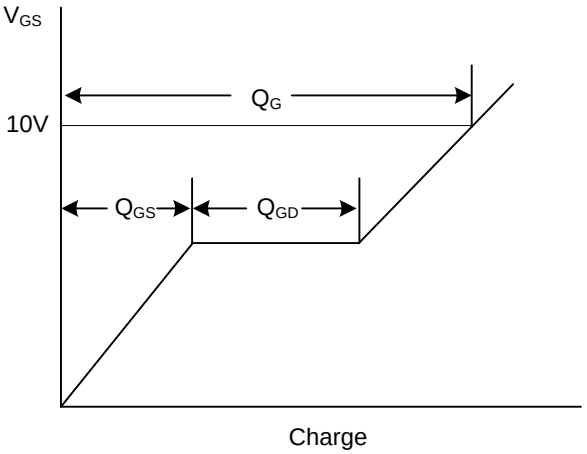
Switching Test Circuit



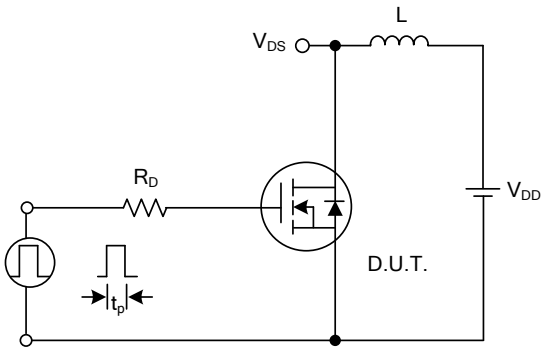
Switching Waveforms



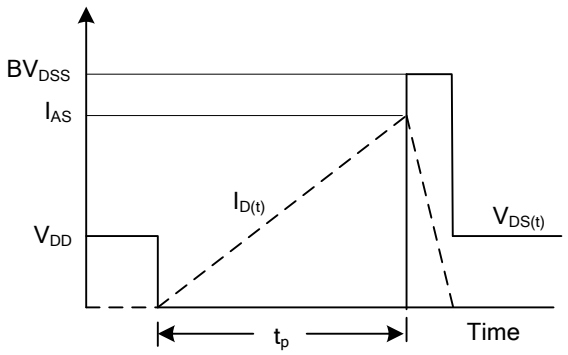
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms