

Specifications for Blanview TFT-LCD Monitor

Version 3.0

MODEL COM32H3N89ULC

(Please be sure to check the specifications latest version.)

Customer's Approval

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Section:

Title:

Date:

ORTUSTECH

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1. Application

This Specification is applicable to 8.05cm (3.2 inch) Blanview TFT-LCD monitor for non-military use.

- ⊙ ORTUS TECHNOLOGY makes no warranty or assume no liability that use of this Product and/or any information including drawings in this Specification by Purchaser is not infringing any patent or other intellectual property rights owned by third parties, and ORTUS TECHNOLOGY shall not grant to Purchaser any right to use any patent or other intellectual property rights owned by third parties. Since this Specification contains ORTUS TECHNOLOGY's confidential information and copy right, Purchaser shall use them with high degree of care to prevent any unauthorized use, disclosure, duplication, publication or dissemination of ORTUS TECHNOLOGY'S confidential information and copy right.
- ⊙ If Purchaser intends to use this Products for an application which requires higher level of reliability and/or safety in functionality and/or accuracy such as transport equipment (aircraft, train, automobile, etc.), disaster-prevention/security equipment or various safety equipment, Purchaser shall consult ORTUS TECHNOLOGY on such use in advance.
- ⊙ This Product shall not be used for application which requires extremely higher level of reliability and/or safety such as aerospace equipment, telecommunication equipment for trunk lines, control equipment for nuclear facilities or life-support medical equipment.
- ⊙ It must be noted as an mechanical design manner, especial attention in housing design to prevent arcuation/flexure or caused by stress to the LCD module shall be considered.
- ⊙ ORTUS TECHNOLOGY assumes no liability for any damage resulting from misuse, abuse, and/or miss-operation of the Product deviating from the operating conditions and precautions described in the Specification.
- ⊙ ORTUS TECHNOLOGY is not responsible for any nonconformities and defects that are not specified in this specifications.
- ⊙ If any issue arises as to information provided in this Specification or any other information, ORTUS TECHNOLOGY and Purchaser shall discuss them in good faith and seek solution.
- ⊙ ORTUS TECHNOLOGY assumes no liability for defects such as electrostatic discharge failure occurred during peeling off the protective film or Purchaser's assembly process.
- ⊙ This Product is compatible for RoHS directive.

Object substance	Maximum content [ppm]
Cadmium and its compound	100
Hexavalent Chromium Compound	1000
Lead & Lead compound	1000
Mercury & Mercury compound	1000
Polybrominated biphenyl series (PBB series)	1000
Polybrominated biphenyl ether series (PBDE series)	1000

2. Outline Specifications

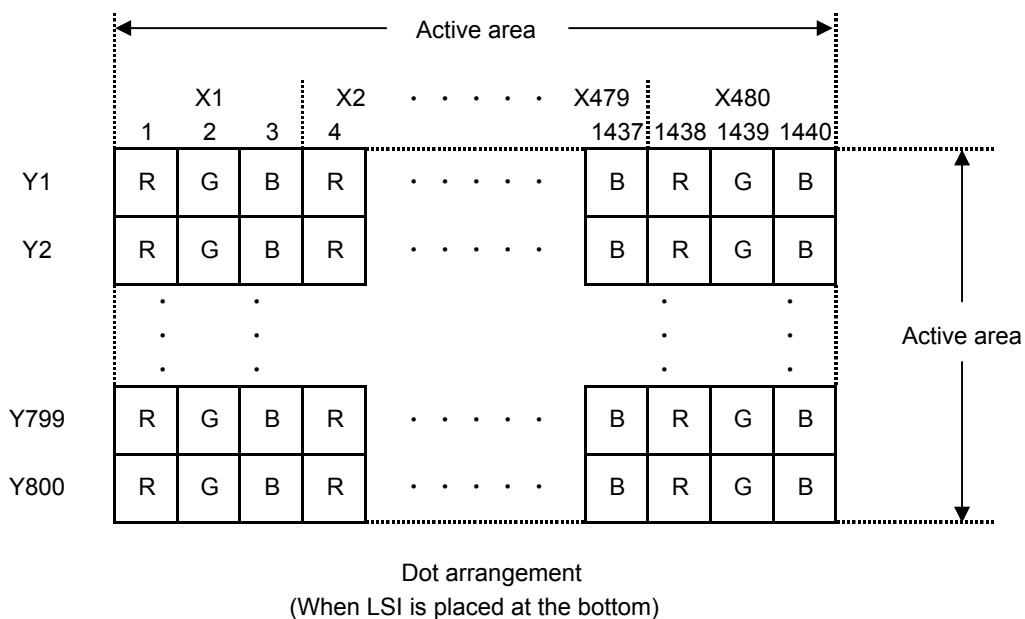
2.1 Features of the Product

- 3.2 inch diagonal display, 1,440 [H] x 800 [V] dots.
- 8-bit 16,777,216 color display capability.
- System Interface (Register setting)
- Serial Peripheral Interface (SPI)
- RGB interface with 24-bit data bus (VSYNC, HSYNC, ENABLE, DOTCLK, D23-0)
- Internal booster for various voltage levels to drive LC

		Indoor		Outdoor	
		Readability	Power Efficiency (Battery Life)	Readability	Power Efficiency (Battery Life)
Transmissive		Good	Good	Fair	Poor
Transflective		Fair	Poor	Good	Good
Blanview		Good	Good	Good	Good

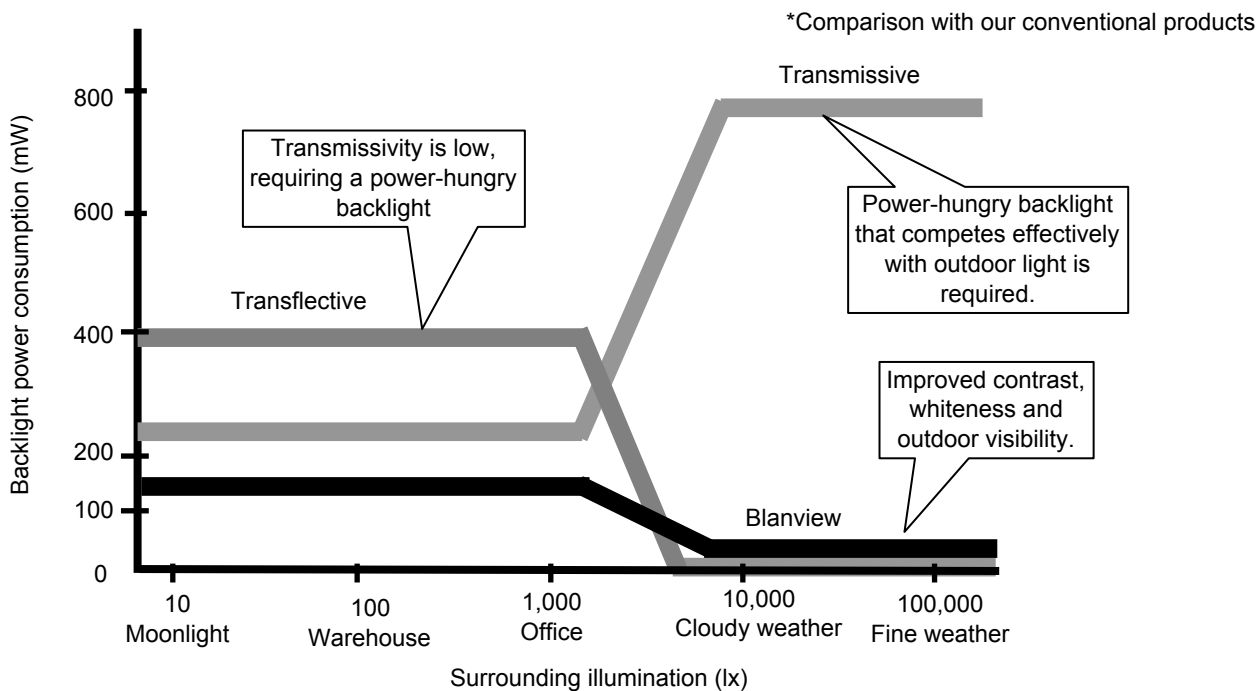
2.2 Display Method

Items	Specifications	Remarks
Display type	16,777,216 colors. Blanview, Normally Black	
Driving method	a-Si TFT Active matrix Line-scanning, Non-interface	
Dot arrangement	RGB stripe arrangement	Refer to "Dot arrangement"
Signal input method	Register : Serial Peripheral Interface (SPI) Data : 24 bit RGB interface	
Backlight type	Long life & High bright white LED.	



<Features of Blanview>

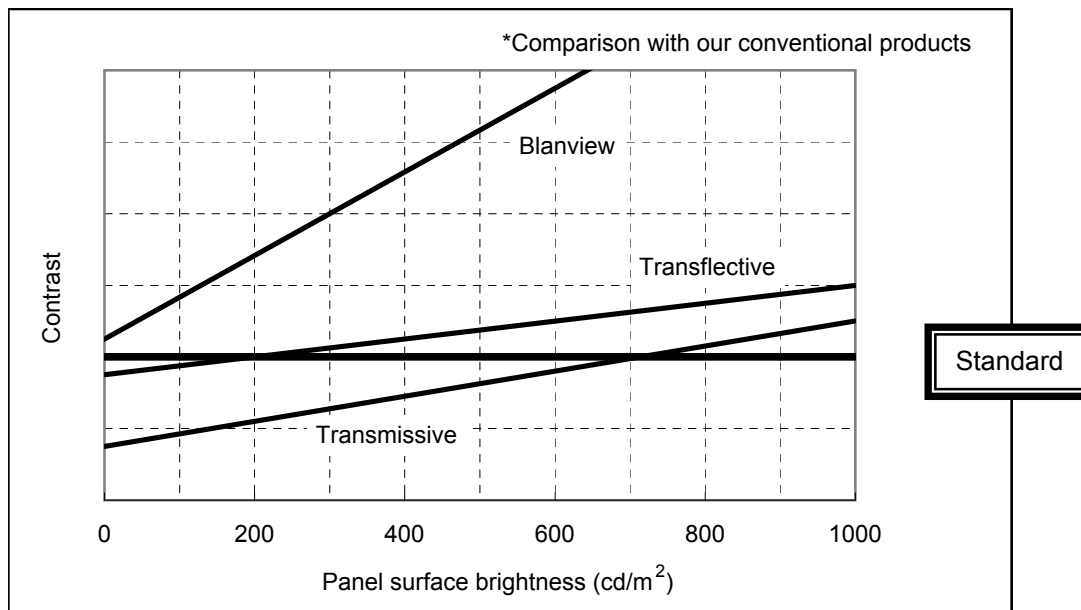
- Backlight power consumption required to assure visibility. (equivalent to 3.5"QVGA)



- Contrast characteristics under 100,000lx. (same condition as direct sunlight.)

With better contrast (higher contrast ratio), Blanview TFT-LCD has the best outdoor readability in three different types of TFT-LCD.

Below chart shows contrast value against panel surface brightness. (Horizontal: Panel surface brightness/ Vertical: Contrast value) LCD panel has enough outdoor readability above our Standard line. (ORTUS TECHNOLOGY criteria)



3. Dimensions and Shape

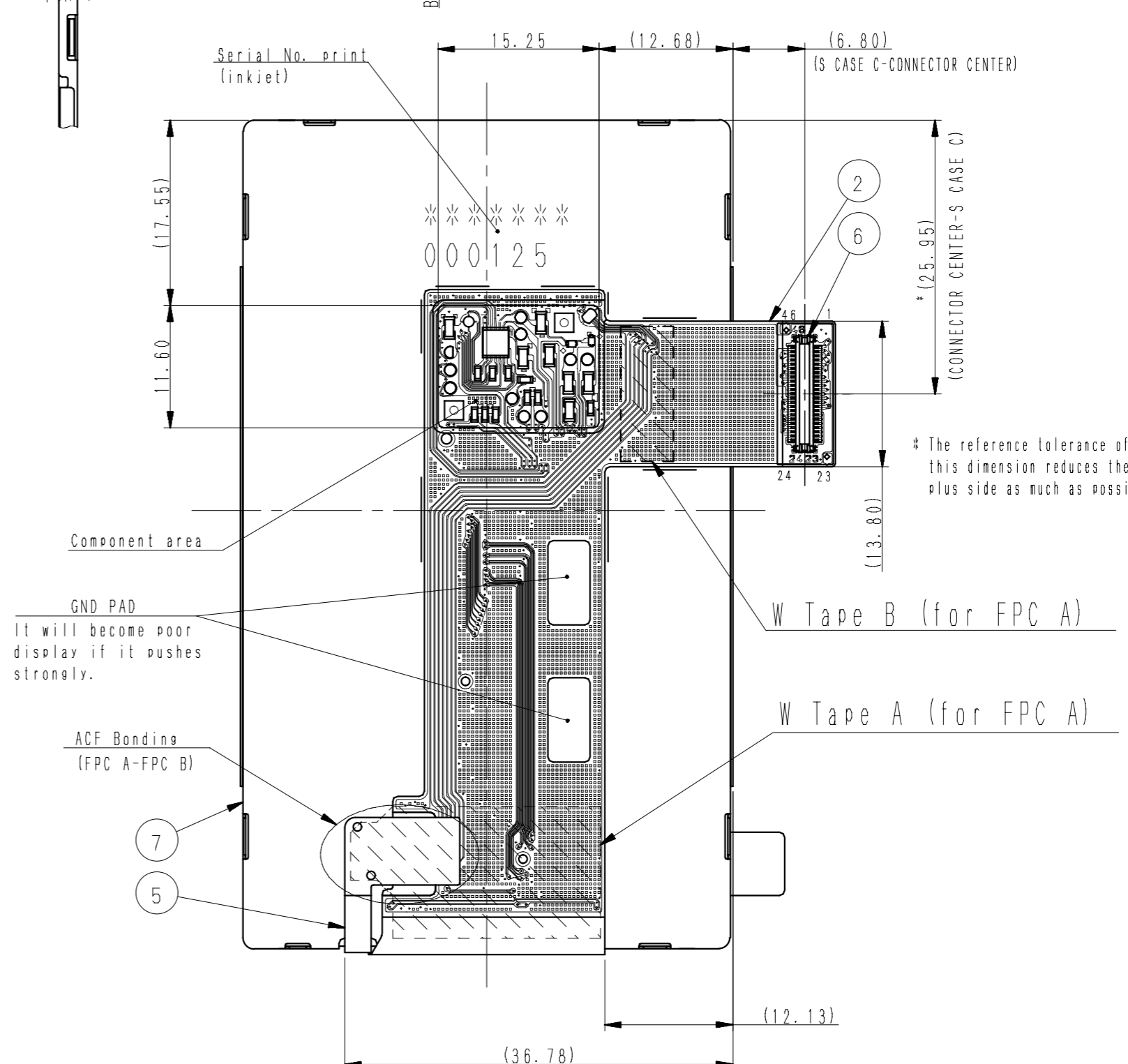
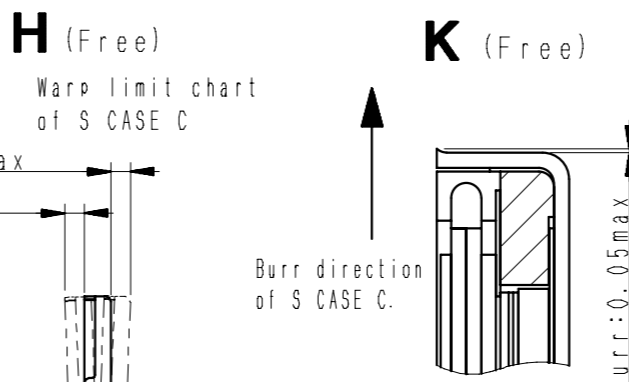
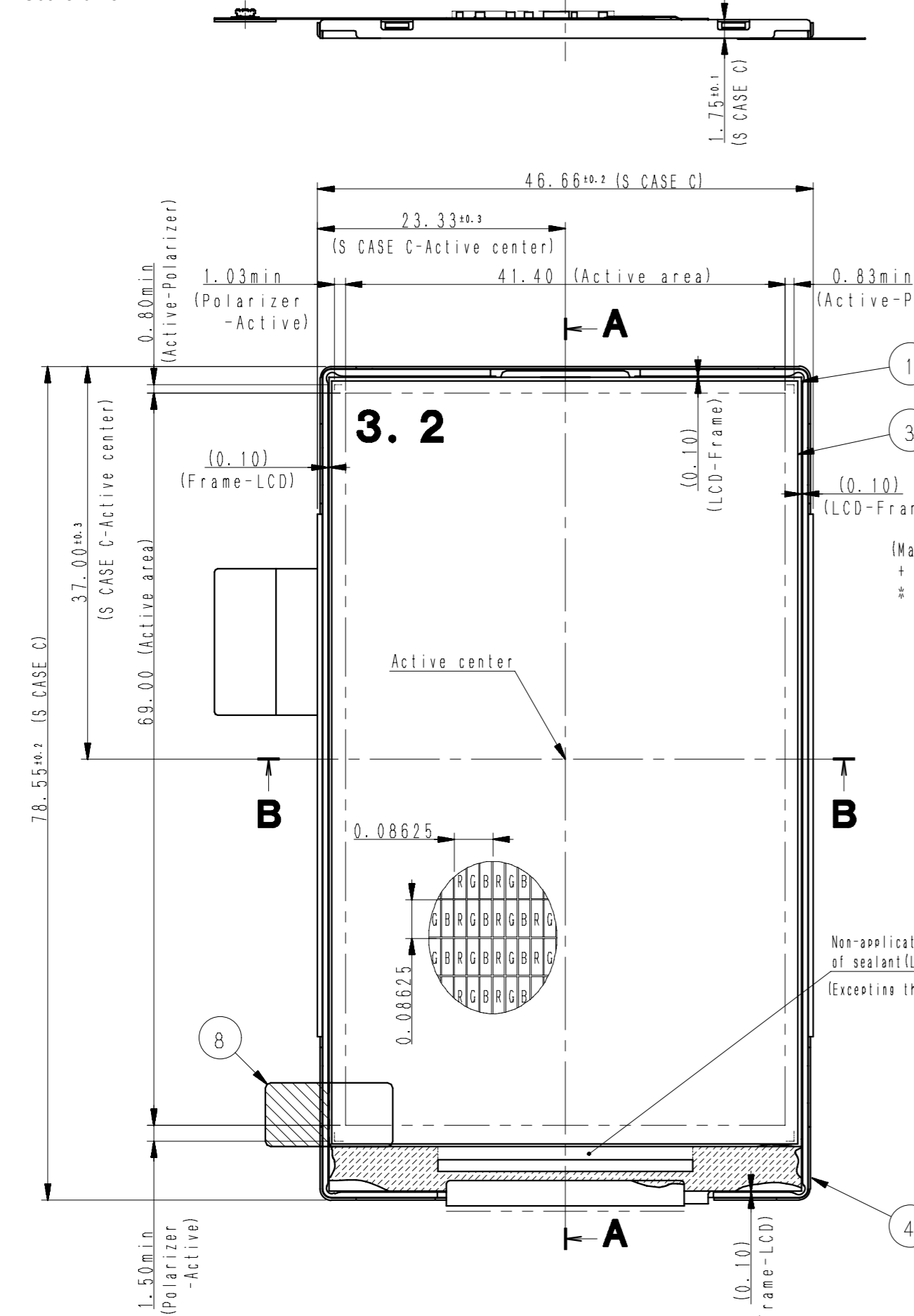
3.1 Dimensions

Items	Specifications	Unit	Remarks
Outline dimensions	46.66[H] × 78.55[V] × 1.75[D]	mm	Exclude FPC cable and parts on FPC
Active area	41.40[H] × 69.00[V]	mm	8.05cm diagonal
Number of dots	1440[H] × 800[V]	dot	
Dot pitch	28.75[H] × 86.25[V]	μm	
Surface hardness of the polarizer	3	H	Load:2.0N
Weight	14	g	Include FPC cable

3.2 Outward Form

EC No.	REV. No.	REVISE	DATE (Y:M:D)	APPROVED	CHECKED	PREPARED
	A × 1	Correct:Connector	16:03:16			

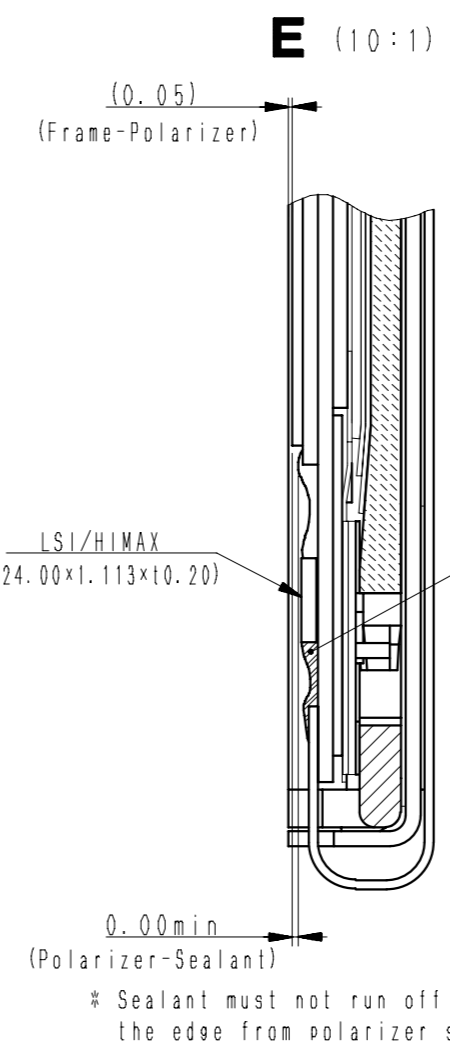
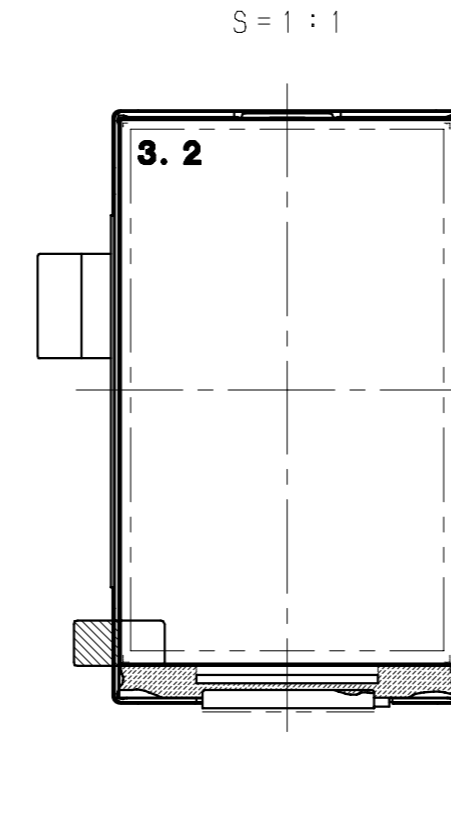
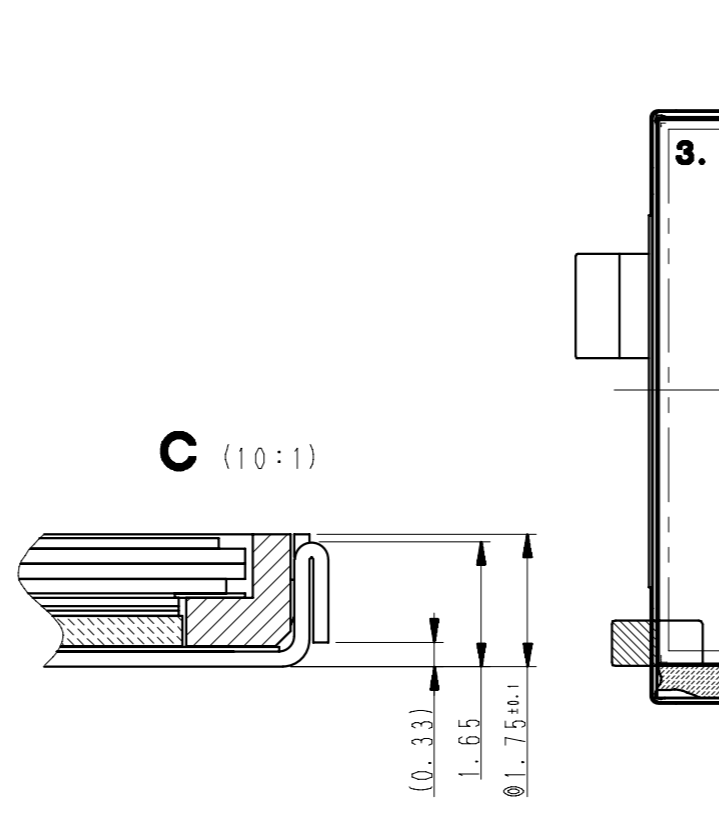
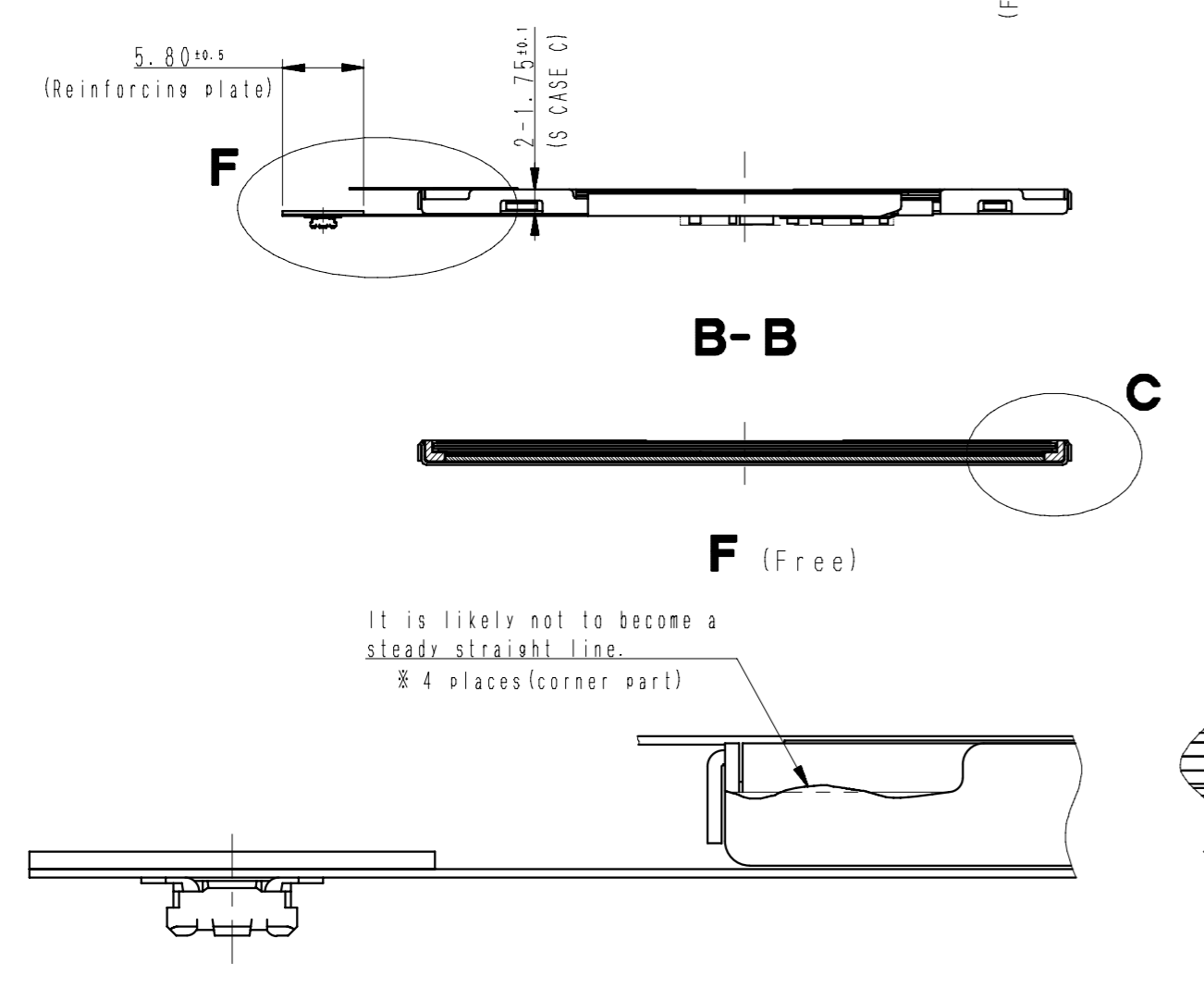
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Issue: Mar. 31, 2016



Pin-Arrangement

G4	GND	G1	GND
46	GND	1	LED5
45	VCC	2	LED4
44	VCC	3	LED3
43	IOVCC	4	LED2
42	ENABLE	5	LED1
41	SDI	6	VLED
40	SCL	7	VLED
39	CSB	8	DB7
38	DOTCLK	9	DB6
37	RESETB	10	DB5
36	VSYNC	11	DB4
35	HSYNC	12	DB3
34	GND	13	DB2
33	DB16	14	DB1
32	DB17	15	DB0
31	DB18	16	GND
30	DB19	17	DB15
29	DB20	18	DB14
28	DB21	19	DB13
27	DB22	20	DB12
26	DB23	21	DB11
25	GND	22	DB10
24	DB8	23	DB9
G3	GND	G2	GND

* The reference tolerance of this dimension reduces the plus side as much as possible.



- Note 1. Angular deviation of LCD cell from the TFT-LCD monitor's reference axis shall be less than [±40'].
2. Protective film is affixed on front surface of the screen. Location tolerance of the protective film shall be ±1.5 mm to the polarizing film.
3. Protective film is affixed on front surface of the screen.
4. Constant-current circuit is required for the LED drive circuit to make full use of original visual quality of the display.
- When other driving method is used for the LED driving circuit, original visual quality of the display is not guaranteed.

	12			
	11			
	10			
	9			
R Tape	8			
S CASE C	7		SUS304 (t=0.20)	
Connector	6	AXI446124		PANASONIC
FPC B	5	AXI446124		Use of LED
Frame	4		PC	
Polarizer	3		HC type	
FPC A	2			Use of LCD
TFT-LCD	1			Total t=0.40(0.20±0.20)
PART NAME	Part No.	Spec. No.	Standard	Material
APPROVED	K.Hashizume	GENERAL TOLERANCE ±0.3	SCALE 2:1	UNIT mm
CHECKED	J.Hiranobu	ISSUE (Y:M:D) 16:03:18	MODEL COM32H3N89U**	
CHECKED	J.Hiranobu	NAME		
DESIGN	J.Hiranobu			
DRAW	J.Hiranobu			
OUTLINE-D3N89				
				ORTUSTECH
				ORTUS TECHNOLOGY CO., LTD.
				DO NOT DUPLICATE. CONFIDENTIAL AND PROPRIETARY
DRAWING No.		REV.	SHEET	DIV.
RJD526609D201				

3.3 Serial № print (S-print)

1) Display Items

S-print indicates the least significant digit of manufacture year (1digit),
manufacture month with below alphabet (1letter), model code (4characters), serial number (6digits).

* Contents of Display

*	*	****	*****
-	-	-	-
a	b	c	d

Contents of display				
a	The least significant digit of manufacture year			
b	Manufacture month	Jan-A Feb-B Mar-C Apr-D	May-E Jun-F Jul-G Aug-H	Sep-I Oct-J Nov-K Dec-L
c	Model code	32SC (Made in Japan) 32TC (Made in Malaysia)		
d	Serial number			

* Example of indication of Serial № print (S-print)

•Made in Japan

5H32SC000125

means "manufactured in August 2015, 3.2" S type, C specifications, serial number 000125"

•Made in Malaysia

5H32TC000125

means "manufactured in August 2015, 3.2" T type, C specifications, serial number 000125"

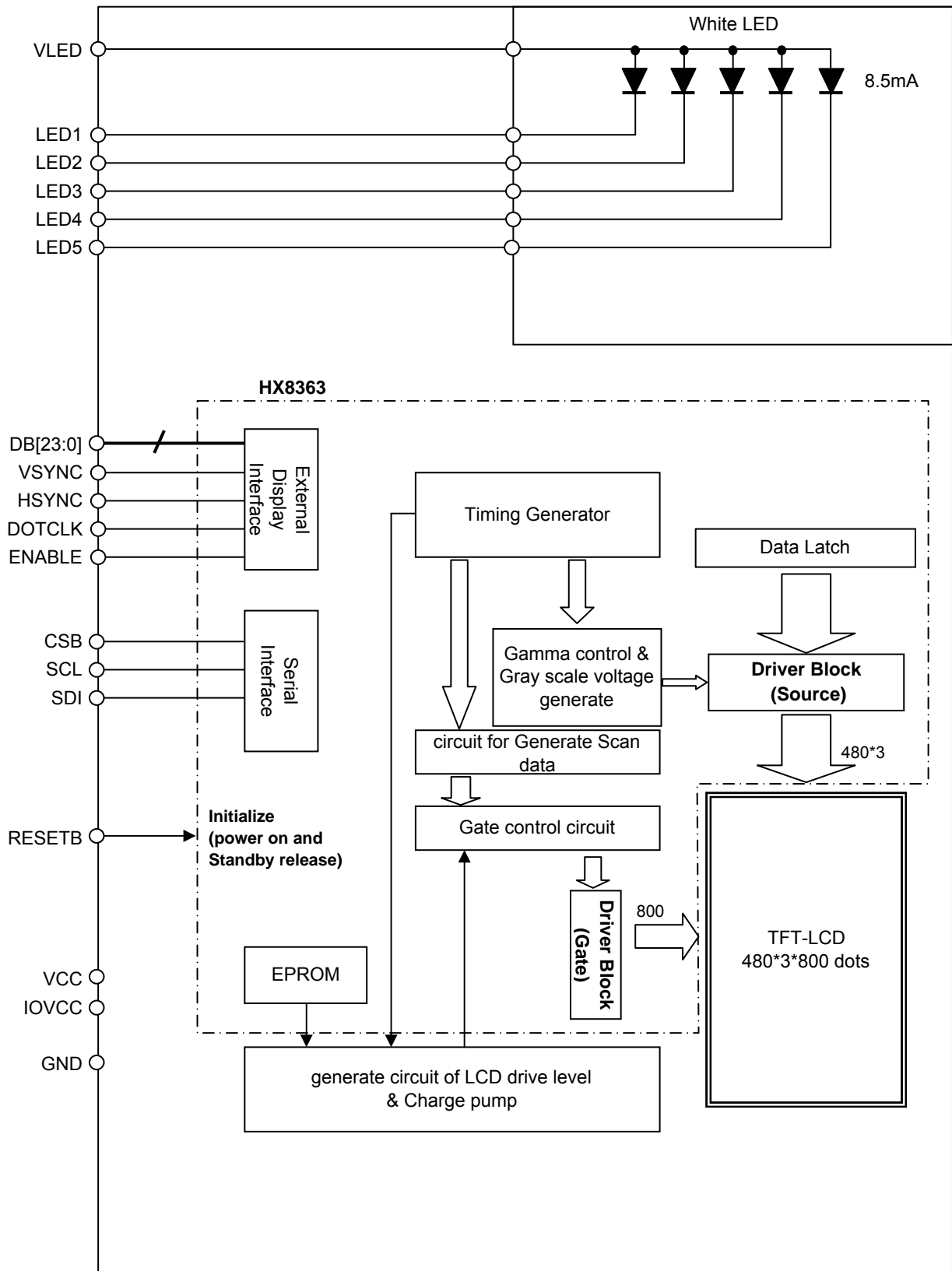
2) Location of Serial № print (S-print)

Refer to 3.2 "Outward Form".

3)Others

Please note that it is likely to disappear with an organic solvent about the Serial print.

4. Block Diagram



5.FPC Terminals

№	Symbol	Details	Remark	IO
1	LED5	Backlight LED Cathode5		P
2	LED4	Backlight LED Cathode4		P
3	LED3	Backlight LED Cathode3		P
4	LED2	Backlight LED Cathode2		P
5	LED1	Backlight LED Cathode1		P
6	VLED	Power supply for Backlight LED		P
7	VLED	Power supply for Backlight LED		P
8	DB7	B_Data	MSB	I
9	DB6			I
10	DB5			I
11	DB4			I
12	DB3			I
13	DB2			I
14	DB1			I
15	DB0		LSB	I
16	GND	GROUND		P
17	DB15	G_Data	MSB	I
18	DB14			I
19	DB13			I
20	DB12			I
21	DB11			I
22	DB10			I
23	DB9			I
24	DB8		LSB	I
25	GND	GROUND		P
26	DB23	R_Data	MSB	I
27	DB22			I
28	DB21			I
29	DB20			I
30	DB19			I
31	DB18			I
32	DB17			I
33	DB16		LSB	I
34	GND	GROUND		P
35	HSYNC	HSYNC		I
36	VSYNC	VSYNC		I
37	RESETB	LCD Reset	L:Initialize Power_ON Reset is Required when Turning on the Power	I
38	DOTCLK	DOTCLK		I
39	CSB	3-Wire SPI Chip Select		I
40	SCL	3-Wire SPI clock		I
41	SDI	3-Wire SPI DATA input		I
42	ENABLE	ENABLE		I
43	IOVCC	Power		P
44	VCC	Power		P
45	VCC	Power		P
46	GND	GROUND		P

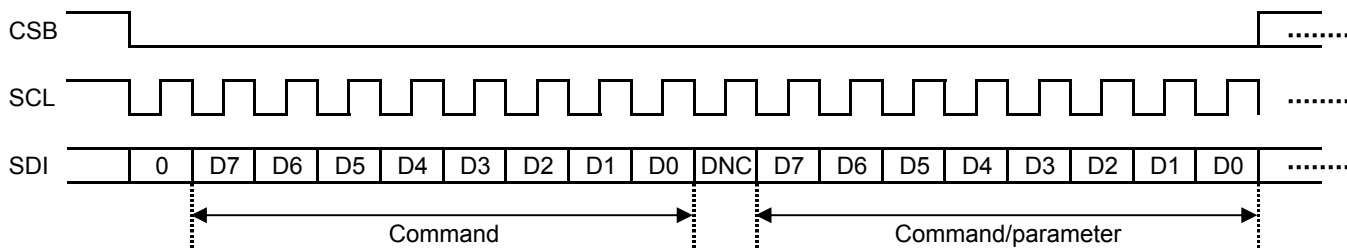
- Recommended connector: Panasonic corporation : AXT346124
- Please make sure to check a consistency between pin assignment in "3.2 Outward Form" and your connector pin assignment when designing your circuit.
Inconsistency in input signal assignment may cause a malfunction.
- Since FPC cable has gold plated terminals, gilt finish contact shoe connector is recommended.

6. Serial Data Transfer Interface

Instructions are transferred using 3 wire serial data transfer interface. The 3 wire serial bus uses chip select line (CSB), serial input data (SDI) and serial transfer clock line (SCL).

The 3 wire serial data packet is consists of control bit DNC and transmission byte. If the control bit is low, the transmission byte is command byte. If the control bit is high, the transmission byte is stored to command register. DNC should be transferred first , followed by MSB of transmission byte.

The serial interface is initialized when CSB is high, and the falling edge of CSB enables the serial interface.



7. Instruction list

(1)

(Hex)	Register	DNC	D7	D6	D5	D4	D3	D2	D1	D0
00	NOP	0	0	0	0	0	0	0	0	0
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
01	SWRESET	0	0	0	0	0	0	0	0	1
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
06	RDRED	0	0	0	0	0	0	1	1	0
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
07	RDGREEN	0	0	0	0	0	0	1	1	1
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
08	RDBLUE	0	0	0	0	0	1	0	0	0
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
0A	RDDPM	0	0	0	0	0	1	0	1	0
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
0B	RDDMADCTL	0	0	0	0	0	1	0	1	1
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
0C	RDDCOLMOD	0	0	0	0	0	1	1	0	0
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
0D	RDDIM	0	0	0	0	0	1	1	0	1
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
0E	RDDSM	0	0	0	0	0	1	1	1	0
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
0F	RDDSDR	0	0	0	0	0	1	1	1	1
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
10	SLPIN	0	0	0	0	1	0	0	0	0
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
11	SLPOUT	0	0	0	0	1	0	0	0	1
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
20	INVOFF	0	0	0	1	0	0	0	0	0
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
21	INVON	0	0	0	1	0	0	0	0	1
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
26	GAMSET	0	0	0	1	0	0	1	1	0
	initial	-	0	0	0	0	0	0	0	1
	recommend	-	-	-	-	-	-	-	-	-
28	DISPOFF	0	0	0	1	0	1	0	0	0
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
29	DISPON	0	0	0	1	0	1	0	0	1
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-

(2)

(Hex)	Register	DNC	D7	D6	D5	D4	D3	D2	D1	D0	
36	MADCTL	0	0	0	1	1	0	1	1	0	
		1	-	-	-	-	BGR	-	SS	GS	
	initial	-	0	0	0	0	0	0	0	0	
	recommend	-	0	0	0	0	0	0	0	0	
3A	COLMOD	0	0	0	1	1	1	0	1	0	
		1	-	CSEL_RGB[2:0]			-	-	-	-	
	initial	-	0	1	1	1	0	0	0	0	
	recommend	-	0	1	1	1	0	0	0	0	
B1	SETPOWER	0	1	0	1	1	0	0	0	1	
		1	-	VSN_EN	VSP_EN	VGL_EN	VGH_EN	-	VDDN_HZ	SLP	
	initial	-	1	0	0	0	0	0	0	1	
	recommend	-	0	1	1	1	1	0	0	0	
	initial	-	-	FS12	FS11	FS10	-	AP2	AP1	AP0	
	recommend	-	0	0	1	1	0	0	0	0	
	initial	-	0	0	1	0	0	1	0	0	
	recommend	-	0	0	1	0	0	1	0	0	
	initial	-	-	-	-	-	BT3	BT2	BT1	BT0	
	recommend	-	0	0	0	0	0	0	0	0	
	initial	-	0	0	0	0	0	1	0	0	
	recommend	-	0	0	0	0	0	0	1	0	
	initial	-	1	DT1	DT0	DC1	DC0	DC_DIV3	DC_DIV2	DC_DIV1	DC_DIV0
	recommend	-	0	0	1	1	0	0	0	0	
	initial	-	0	0	0	0	0	0	1	0	
	recommend	-	0	0	0	0	0	0	0	1	
	initial	-	1	-	DTPS2	DTPS1	DTPS0	-	DTP2	DTP1	DTP0
	recommend	-	0	0	0	0	0	0	1	0	
	initial	-	0	0	0	0	0	0	0	1	0
	recommend	-	0	0	0	0	0	0	0	1	0
	initial	-	1	-	DTNS2	DTNS1	DTNS0	-	DTN2	DTN1	DTN0
	recommend	-	0	0	0	1	0	0	1	1	0
	initial	-	0	0	0	0	0	0	0	1	1
	recommend	-	0	0	0	0	0	0	0	1	1
	initial	-	1	-	-	-	BTP4	BTP3	BTP2	BTP1	BTP0
	recommend	-	0	0	0	0	1	1	1	1	0
	initial	-	0	0	0	1	0	0	0	0	0
	recommend	-	0	0	0	1	0	0	0	0	0
	initial	-	1	-	-	-	BTN4	BTN3	BTN2	BTN1	BTN0
	recommend	-	0	0	0	0	1	1	1	1	0
initial	-	0	0	0	0	1	0	0	0	0	
recommend	-	0	0	0	1	0	0	0	0	0	
initial	-	1	VRHP7	VRHP6	VRHP5	VRHP4	VRHP3	VRHP2	VRHP1	VRHP0	
recommend	-	0	0	1	0	0	1	0	0	0	
initial	-	0	0	1	1	0	1	0	0	0	
recommend	-	0	0	1	1	0	1	0	0	0	
initial	-	1	VRHN7	VRHN6	VRHN5	VRHN4	VRHN3	VRHN2	VRHN1	VRHN0	
recommend	-	0	0	1	0	1	1	0	0	0	
initial	-	0	0	1	1	1	1	1	0	0	
recommend	-	0	0	1	1	1	1	1	0	0	
initial	-	1	-	-	VRMP5	VRMP4	VRMP3	VRMP2	VRMP1	VRMP0	
recommend	-	0	0	0	1	1	0	0	0	1	
initial	-	0	0	0	1	1	1	1	1	1	
recommend	-	0	0	0	1	1	1	1	1	1	
initial	-	1	-	-	VRMN5	VRMN4	VRMN3	VRMN2	VRMN1	VRMN0	
recommend	-	0	0	0	1	1	0	0	0	1	
initial	-	0	0	0	1	1	1	1	1	1	
recommend	-	0	0	0	1	1	1	1	1	1	
B3	SETRGBIF	0	1	0	1	1	0	0	1	1	
		1	-	-	-	-	DPL	HSPL	VSPL	EPL	
	initial	-	0	0	0	0	0	0	0	1	
	recommend	-	0	0	0	0	0	0	0	1	

(3)

(Hex)	Register	DNC	D7	D6	D5	D4	D3	D2	D1	D0	
B4	SETRGBIF	0	1	0	1	1	0	1	0	0	
		1	-	-	-	-	NW[1:0]		-	-	
	initial	-	0	0	0	0	1	0	0	0	
	recommend	-	0	0	0	0	0	0	0	0	
	1	SON[7:0]									
	initial	-	0	0	0	1	0	0	1	0	
	recommend	-	0	0	0	0	1	0	0	0	
	1	SOFF[7:0]									
	initial	-	0	1	1	1	0	0	1	0	
	recommend	-	0	1	0	1	0	1	1	0	
	1	EQS[7:0]									
	initial	-	0	0	0	1	0	0	1	0	
	recommend	-	0	0	0	0	0	1	1	1	
	1	EQON[7:0]									
	initial	-	0	0	0	0	0	1	1	0	
	recommend	-	0	0	0	0	0	0	0	1	
	1	GDON[7:0]									
	initial	-	0	0	0	0	0	0	1	1	
	recommend	-	0	0	0	0	0	0	0	1	
	1	GDOFF[7:0]									
	initial	-	0	1	1	0	0	0	0	0	
	recommend	-	0	1	0	0	1	1	1	0	
	1	GVSSP1[7:0]									
	initial	-	0	0	0	0	0	0	1	1	
recommend	-	0	0	0	0	0	0	0	1		
1	GVSSP2[7:0]										
initial	-	0	1	0	1	1	0	1	0		
recommend	-	0	1	0	0	0	0	1	0		
B9	SETRGBIF	0	1	0	1	1	1	0	0	1	
		1	EXTC1[7:0]								
	initial	-	0	0	0	0	0	0	0	0	
	recommend	-	1	1	1	1	1	1	1	1	
	1	EXTC2[7:0]									
	initial	-	0	0	0	0	0	0	0	0	
	recommend	-	1	0	0	0	0	0	1	1	
	1	EXTC3[7:0]									
	initial	-	0	0	0	0	0	0	0	0	
	recommend	-	0	1	1	0	0	0	1	1	
	C1	SETDGCLUT	0	1	1	0	0	0	0	0	1
			1	-	-	-	-	-	-	-	DGC_EN
initial		-	0	0	0	0	0	0	0	0	
recommend		-	0	0	0	0	0	0	0	1	
1		D1[7:0]									
initial		-	0	0	0	0	0	0	0	0	
recommend		-	1	1	1	0	1	1	1	1	
1		D2[7:0]									
initial		-	0	0	0	0	1	0	0	0	
recommend		-	1	1	0	1	0	1	1	1	
1		D3[7:0]									
initial		-	0	0	0	1	0	0	0	0	
recommend		-	1	0	1	1	1	1	0	1	
1		D4[7:0]									
initial	-	0	0	0	1	1	0	0	0		
recommend	-	1	0	0	1	1	0	1	0		

(4)

(Hex)	Register	DNC	D7	D6	D5	D4	D3	D2	D1	D0
C1	SETDGCLUT	1	D5[7:0]							
	initial	-	0	0	1	0	0	0	0	0
	recommend	-	0	1	1	1	1	0	1	0
		1	D6[7:0]							
	initial	-	0	0	1	0	1	0	0	0
	recommend	-	0	1	0	1	1	0	1	1
		1	D7[7:0]							
	initial	-	0	0	1	1	0	0	0	0
	recommend	-	0	0	1	1	1	1	0	1
		1	D8[7:0]							
	initial	-	0	0	1	1	1	0	0	0
	recommend	-	0	0	1	0	0	1	0	1
		1	D9[7:0]							
	initial	-	0	1	0	0	0	0	0	0
	recommend	-	0	0	0	0	1	0	0	1
		1	D10[7:0]							
	initial	-	0	1	0	0	1	0	0	0
	recommend	-	1	1	1	0	1	1	0	0
		1	D11[7:0]							
	initial	-	0	1	0	1	0	0	0	0
	recommend	-	1	1	0	1	0	0	1	0
		1	D12[7:0]							
initial	-	0	1	0	1	1	0	0	0	
recommend	-	1	0	1	1	0	1	0	0	
	1	D13[7:0]								
initial	-	0	1	1	0	0	0	0	0	
recommend	-	1	0	0	1	1	0	1	0	
	1	D14[7:0]								
initial	-	0	1	1	0	1	0	0	0	
recommend	-	0	1	1	1	1	1	1	1	
	1	D15[7:0]								
initial	-	0	1	1	1	0	0	0	0	
recommend	-	0	1	1	0	0	1	0	1	
	1	D16[7:0]								
initial	-	0	1	1	1	1	0	0	0	
recommend	-	0	1	0	0	1	0	0	0	
	1	D17[7:0]								
initial	-	1	0	0	0	0	0	0	0	
recommend	-	0	0	1	0	1	1	0	1	
	1	D18[7:0]								
initial	-	1	0	0	0	1	0	0	0	
recommend	-	0	0	0	1	0	1	0	0	
	1	D19[7:0]								
initial	-	1	0	0	1	0	0	0	0	
recommend	-	1	1	1	1	0	1	1	0	
	1	D20[7:0]								
initial	-	1	0	0	1	1	0	0	0	
recommend	-	1	1	0	1	1	1	0	0	
	1	D21[7:0]								
initial	-	1	0	1	0	0	0	0	0	
recommend	-	1	1	0	0	0	0	0	1	
	1	D22[7:0]								
initial	-	1	0	1	0	1	0	0	0	
recommend	-	1	0	1	0	1	0	0	0	

SETDGCLUT continues to the next page.

(5)

(Hex)	Register	DNC	D7	D6	D5	D4	D3	D2	D1	D0
C1	SETDGCLUT	1	D23[7:0]							
	initial	-	1	0	1	1	0	0	0	0
	recommend	-	1	0	0	0	1	1	0	0
		1	D24[7:0]							
	initial	-	1	0	1	1	1	0	0	0
	recommend	-	0	1	0	1	1	0	0	1
		1	D25[7:0]							
	initial	-	1	1	0	0	0	0	0	0
	recommend	-	0	0	1	1	0	1	1	0
		1	D26[7:0]							
	initial	-	1	1	0	0	1	0	0	0
	recommend	-	0	0	0	1	0	1	0	1
		1	D27[7:0]							
	initial	-	1	1	0	1	0	0	0	0
	recommend	-	1	1	1	1	0	0	1	1
		1	D28[7:0]							
	initial	-	1	1	0	1	1	0	0	0
	recommend	-	1	1	0	1	0	0	1	0
		1	D29[7:0]							
	initial	-	1	1	1	0	0	0	0	0
	recommend	-	1	0	1	1	1	0	1	1
		1	D30[7:0]							
	initial	-	1	1	1	0	1	0	0	0
	recommend	-	1	0	0	0	1	1	1	0
		1	D31[7:0]							
	initial	-	1	1	1	1	0	0	0	0
	recommend	-	0	0	0	0	1	1	1	1
		1	D32[7:0]							
	initial	-	1	1	1	1	1	0	0	0
	recommend	-	0	0	0	0	1	0	0	1
		1	D33[7:0]							
	initial	-	1	1	1	1	1	1	1	1
	recommend	-	0	0	0	0	0	0	0	0
		1	D34[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	1	1	1	1	1	1	1	1
		1	D35[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	1	1	1	1	1	1	1	1
		1	D36[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	1	1	1	0	1	0	1	0
		1	D37[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	1	0	1	0	1	0	1	0
		1	D38[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	1	0	1	0	0	1	0	1
		1	D39[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	1	0	1	0	1	0	1
		1	D40[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	1	0	1	0	0	0	0

SETDGCLUT continues to the next page.

(6)

(Hex)	Register	DNC	D7	D6	D5	D4	D3	D2	D1	D0
C1	SETDGCLUT	1	D41[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	0	0	0	0	0	0	0
		1	D42[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	0	0	0	0	0	0	0
		1	D43[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	1	1	1	0	1	0	1	0
		1	D44[7:0]							
	initial	-	0	0	0	0	1	0	0	0
	recommend	-	1	1	0	0	1	1	1	1
		1	D45[7:0]							
	initial	-	0	0	0	1	0	0	0	0
	recommend	-	1	0	1	0	1	0	0	0
		1	D46[7:0]							
	initial	-	0	0	0	1	1	0	0	0
	recommend	-	1	0	0	0	0	0	0	1
		1	D47[7:0]							
	initial	-	0	0	1	0	0	0	0	0
	recommend	-	0	1	0	1	1	1	1	1
		1	D48[7:0]							
	initial	-	0	0	1	0	1	0	0	0
	recommend	-	0	0	1	1	1	1	1	0
		1	D49[7:0]							
	initial	-	0	0	1	1	0	0	0	0
	recommend	-	0	0	1	0	0	1	0	1
		1	D50[7:0]							
	initial	-	0	0	1	1	1	0	0	0
	recommend	-	0	0	0	0	0	1	1	0
		1	D51[7:0]							
	initial	-	0	1	0	0	0	0	0	0
	recommend	-	0	0	0	0	0	0	0	0
		1	D52[7:0]							
	initial	-	0	1	0	0	1	0	0	0
	recommend	-	1	1	0	1	0	0	0	0
		1	D53[7:0]							
	initial	-	0	1	0	1	0	0	0	0
	recommend	-	1	0	1	1	0	0	1	1
		1	D54[7:0]							
	initial	-	0	1	0	1	1	0	0	0
	recommend	-	1	0	0	1	0	1	1	1
		1	D55[7:0]							
	initial	-	0	1	1	0	0	0	0	0
	recommend	-	0	1	1	1	1	1	1	1
		1	D56[7:0]							
	initial	-	0	1	1	0	1	0	0	0
	recommend	-	0	1	1	0	0	1	0	1
		1	D57[7:0]							
	initial	-	0	1	1	1	0	0	0	0
	recommend	-	0	1	0	0	1	0	1	0
		1	D58[7:0]							
	initial	-	0	1	1	1	1	0	0	0
	recommend	-	0	0	1	0	1	1	1	1

SETDGCLUT continues to the next page.

(7)

(Hex)	Register	DNC	D7	D6	D5	D4	D3	D2	D1	D0
C1	SETDGCLUT	1	D59[7:0]							
	initial	-	1	0	0	0	0	0	0	0
	recommend	-	0	0	0	1	0	1	1	0
		1	D60[7:0]							
	initial	-	1	0	0	0	1	0	0	0
	recommend	-	1	1	1	1	1	1	0	1
		1	D61[7:0]							
	initial	-	1	0	0	1	0	0	0	0
	recommend	-	0	0	0	1	0	0	0	0
		1	D62[7:0]							
	initial	-	1	0	0	1	1	0	0	0
	recommend	-	1	1	0	0	1	0	1	0
		1	D63[7:0]							
	initial	-	1	0	1	0	0	0	0	0
	recommend	-	1	0	1	0	1	1	1	1
		1	D64[7:0]							
	initial	-	1	0	1	0	1	0	0	0
	recommend	-	1	0	0	1	1	0	0	1
		1	D65[7:0]							
	initial	-	1	0	1	1	0	0	0	0
	recommend	-	0	1	1	1	0	1	0	0
		1	D66[7:0]							
	initial	-	1	0	1	1	1	0	0	0
	recommend	-	0	1	0	0	0	0	1	1
		1	D67[7:0]							
	initial	-	1	1	0	0	0	0	0	0
	recommend	-	0	0	1	0	1	1	0	0
		1	D68[7:0]							
	initial	-	1	1	0	0	1	0	0	0
	recommend	-	0	0	0	0	1	0	0	1
		1	D69[7:0]							
	initial	-	1	1	0	1	0	0	0	0
	recommend	-	1	1	1	1	0	0	0	1
		1	D70[7:0]							
	initial	-	1	1	0	1	1	0	0	0
	recommend	-	1	1	0	1	0	0	1	1
		1	D71[7:0]							
	initial	-	1	1	1	0	0	0	0	0
	recommend	-	1	1	0	0	0	0	0	1
		1	D72[7:0]							
	initial	-	1	1	1	0	1	0	0	0
	recommend	-	1	0	1	0	0	0	1	0
		1	D73[7:0]							
	initial	-	1	1	1	1	0	0	0	0
	recommend	-	0	1	1	0	1	0	1	1
		1	D74[7:0]							
	initial	-	1	1	1	1	1	0	0	0
	recommend	-	0	0	0	1	0	0	0	0
		1	D75[7:0]							
	initial	-	1	1	1	1	1	1	1	1
	recommend	-	0	0	0	0	0	0	0	0
		1	D76[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	1	1	1	1	1	1	1	1

SETDGCLUT continues to the next page.

(8)

(Hex)	Register	DNC	D7	D6	D5	D4	D3	D2	D1	D0	
C1	SETDGCLUT	1	D77[7:0]								
	initial	-	0	0	0	0	0	0	0	0	
	recommend	-	1	1	1	1	1	1	1	1	
		1	D78[7:0]								
	initial	-	0	0	0	0	0	0	0	0	
	recommend	-	0	0	1	0	1	0	0	1	0
		1	D79[7:0]								
	initial	-	0	0	0	0	0	0	0	0	0
	recommend	-	1	0	1	0	1	0	0	1	0
		1	D80[7:0]								
	initial	-	0	0	0	0	0	0	0	0	0
	recommend	-	1	0	0	1	0	0	0	0	1
		1	D81[7:0]								
	initial	-	0	0	0	0	0	0	0	0	0
	recommend	-	0	1	0	1	0	1	0	0	1
		1	D82[7:0]								
	initial	-	0	0	0	0	0	0	0	0	0
	recommend	-	0	1	0	1	0	0	0	0	0
		1	D83[7:0]								
	initial	-	0	0	0	0	0	0	0	0	0
	recommend	-	0	0	0	0	0	0	0	0	0
		1	D84[7:0]								
	initial	-	0	0	0	0	0	0	0	0	0
	recommend	-	0	0	0	0	0	0	0	0	0
		1	D85[7:0]								
	initial	-	0	0	0	0	0	0	0	0	0
	recommend	-	0	0	0	0	0	0	0	0	0
		1	D86[7:0]								
	initial	-	0	0	0	0	1	0	0	0	0
	recommend	-	1	1	0	0	1	0	0	0	1
		1	D87[7:0]								
	initial	-	0	0	0	1	0	0	0	0	0
recommend	-	1	0	0	1	1	1	1	0	0	
	1	D88[7:0]									
initial	-	0	0	0	1	1	0	0	0	0	
recommend	-	0	1	1	1	0	1	1	1	1	
	1	D89[7:0]									
initial	-	0	0	1	0	0	0	0	0	0	
recommend	-	0	1	0	1	0	0	0	1	1	
	1	D90[7:0]									
initial	-	0	0	1	0	1	0	0	0	0	
recommend	-	0	0	1	1	0	1	0	0	0	
	1	D91[7:0]									
initial	-	0	0	1	1	0	0	0	0	0	
recommend	-	0	0	0	1	1	1	1	0	0	
	1	D92[7:0]									
initial	-	0	0	1	1	1	0	0	0	0	
recommend	-	1	1	1	1	1	0	0	1	1	
	1	D93[7:0]									
initial	-	0	1	0	0	0	0	0	0	0	
recommend	-	0	0	1	0	0	0	0	0	0	
	1	D94[7:0]									
initial	-	0	1	0	0	1	0	0	0	0	
recommend	-	1	1	0	0	0	1	0	0	1	

SETDGCLUT continues to the next page.

(9)

(Hex)	Register	DNC	D7	D6	D5	D4	D3	D2	D1	D0
C1	SETDGCLUT	1	D95[7:0]							
	initial	-	0	1	0	1	0	0	0	0
	recommend	-	1	0	1	0	1	0	1	0
		1	D96[7:0]							
	initial	-	0	1	0	1	1	0	0	0
	recommend	-	1	0	0	0	1	1	0	0
		1	D97[7:0]							
	initial	-	0	1	1	0	0	0	0	0
	recommend	-	0	1	1	1	0	0	1	1
		1	D98[7:0]							
	initial	-	0	1	1	0	1	0	0	0
	recommend	-	0	1	0	1	1	0	0	1
		1	D99[7:0]							
	initial	-	0	1	1	1	0	0	0	0
	recommend	-	0	1	0	0	0	0	0	1
		1	D100[7:0]							
	initial	-	0	1	1	1	1	0	0	0
	recommend	-	0	0	1	0	1	0	0	0
		1	D101[7:0]							
	initial	-	1	0	0	0	0	0	0	0
	recommend	-	0	0	0	1	0	0	0	0
		1	D102[7:0]							
	initial	-	1	0	0	0	1	0	0	0
	recommend	-	1	1	1	1	0	1	1	0
		1	D103[7:0]							
	initial	-	1	0	0	1	0	0	0	0
	recommend	-	1	1	0	1	1	1	0	0
		1	D104[7:0]							
	initial	-	1	0	0	1	1	0	0	0
	recommend	-	1	1	0	0	0	1	0	0
		1	D105[7:0]							
	initial	-	1	0	1	0	0	0	0	0
	recommend	-	1	0	1	0	1	0	1	0
		1	D106[7:0]							
	initial	-	1	0	1	0	1	0	0	0
	recommend	-	1	0	0	1	0	0	1	1
		1	D107[7:0]							
	initial	-	1	0	1	1	0	0	0	0
	recommend	-	0	1	1	0	1	0	1	0
		1	D108[7:0]							
	initial	-	1	0	1	1	1	0	0	0
	recommend	-	0	1	0	0	0	0	0	0
		1	D109[7:0]							
	initial	-	1	1	0	0	0	0	0	0
	recommend	-	0	0	1	0	0	1	0	1
		1	D110[7:0]							
	initial	-	1	1	0	0	1	0	0	0
	recommend	-	0	0	0	0	0	0	0	0
		1	D111[7:0]							
	initial	-	1	1	0	1	0	0	0	0
	recommend	-	1	1	1	0	1	0	0	0
		1	D112[7:0]							
	initial	-	1	1	0	1	1	0	0	0
	recommend	-	1	1	0	0	1	0	1	0

SETDGCLUT continues to the next page.

(10)

(Hex)	Register	DNC	D7	D6	D5	D4	D3	D2	D1	D0
C1	SETDGCLUT	1	D113[7:0]							
	initial	-	1	1	1	0	0	0	0	0
	recommend	-	1	0	1	1	0	1	1	1
		1	D114[7:0]							
	initial	-	1	1	1	0	1	0	0	0
	recommend	-	1	0	0	1	1	1	0	0
		1	D115[7:0]							
	initial	-	1	1	1	1	0	0	0	0
	recommend	-	0	0	0	1	1	0	1	0
		1	D116[7:0]							
	initial	-	1	1	1	1	1	0	0	0
	recommend	-	0	0	0	0	0	1	0	1
		1	D117[7:0]							
	initial	-	1	1	1	1	1	1	1	1
	recommend	-	0	0	0	0	0	0	0	0
		1	D118[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	0	1	1	1	1	1	1
		1	D119[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	1	1	1	1	1	1	1	0
		1	D120[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	0	1	0	1	0	1	0
		1	D121[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	1	0	1	0	1	0	1	0
		1	D122[7:0]							
initial	-	0	0	0	0	0	0	0	0	
recommend	-	1	0	0	1	0	1	0	1	
	1	D123[7:0]								
initial	-	0	0	0	0	0	0	0	0	
recommend	-	0	1	0	1	0	1	0	1	
	1	D124[7:0]								
initial	-	0	0	0	0	0	0	0	0	
recommend	-	0	1	0	1	0	0	0	0	
	1	D125[7:0]								
initial	-	0	0	0	0	0	0	0	0	
recommend	-	0	0	0	0	0	0	0	0	
	1	D126[7:0]								
initial	-	0	0	0	0	0	0	0	0	
recommend	-	0	0	0	0	0	0	0	0	
CC	SETDGCLUT	0	1	1	0	0	1	1	0	0
		1	-	-	-	SM_PANEL	SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL
	initial	-	0	0	0	0	0	0	0	0
recommend	-	0	0	0	0	1	0	1	1	

(11)

(Hex)	Register	DNC	D7	D6	D5	D4	D3	D2	D1	D0
E0	SET SIP READ INDEX	0	1	1	1	0	0	0	0	0
		1	-	-	G1_VRP0[5:0]					
	initial	-	0	0	0	0	0	1	0	1
	recommend	1	0	0	0	0	0	0	0	1
		1	G1_CGMP0[1:0]		G1_VRP1[5:0]					
	initial	-	0	0	0	1	0	0	0	1
	recommend	1	0	1	0	0	1	0	0	0
		1	G1_CGMP1[1:0]		G1_VRP2[5:0]					
	initial	-	0	0	0	1	0	1	0	1
	recommend	1	0	1	0	0	1	1	0	1
		1	G1_CGMP2[1:0]		G1_VRP3[5:0]					
	initial	-	0	0	1	0	0	1	0	0
	recommend	1	0	1	0	0	1	1	1	0
		1	G1_CGMP3[1:0]		G1_VRP4[5:0]					
	initial	-	0	0	1	0	0	1	1	1
	recommend	1	0	1	0	1	0	0	0	0
		1	G1_CGMP5	G1_CGMP4	G1_VRP5[5:0]					
	initial	-	0	0	1	0	0	1	1	1
	recommend	1	1	1	1	1	0	1	1	0
		1	-	G1_PRP0[6]	-	G1_PKP0[4:0]				
	initial	-	0	0	0	0	0	1	1	0
	recommend	1	0	0	0	0	1	0	1	1
		1	G1_PRP0[5:4]		-	G1_PKP1[4:0]				
	initial	-	1	0	0	0	1	1	0	1
	recommend	1	0	1	0	0	1	1	1	0
		1	G1_PRP0[3:2]		-	G1_PKP2[4:0]				
	initial	-	0	0	0	1	0	0	0	1
	recommend	1	0	0	0	1	0	0	1	0
		1	G1_PRP0[1:0]		-	G1_PKP3[4:0]				
	initial	-	1	1	0	1	0	1	0	1
	recommend	-	1	1	0	1	0	1	0	1
		1	-	G1_PRP1[6]	-	G1_PKP4[4:0]				
	initial	-	0	0	0	1	1	0	0	1
	recommend	-	0	0	0	1	0	1	0	1
		1	G1_PRP1[5:4]		-	G1_PKP5[4:0]				
	initial	-	1	1	0	1	0	1	1	0
	recommend	-	1	0	0	1	0	1	0	1
		1	G1_PRP1[3:2]		-	G1_PKP6[4:0]				
	initial	-	1	0	0	1	0	1	1	1
	recommend	-	0	1	0	1	0	1	0	1
		1	G1_PRP1[1:0]		-	G1_PKP7[4:0]				
	initial	-	0	0	0	0	1	0	0	1
	recommend	-	1	0	0	0	1	1	1	0
		1	-	-	G1_PKP8[4:0]					
	initial	-	0	0	0	0	1	0	0	1
	recommend	-	0	0	0	1	0	0	0	1
		1	-			G1_VRN0[5:0]				
	initial	-	0	0	0	0	0	1	0	1
	recommend	-	0	0	0	0	0	0	0	1
		1	G1_CGMN0[1:0]		G1_VRN1[5:0]					
	initial	-	0	0	0	1	0	0	0	1
	recommend	-	0	1	0	0	1	0	0	0

SET SPI READ INDEX continues to the next page.

(12)

(Hex)	Register	DNC	D7	D6	D5	D4	D3	D2	D1	D0
		1	G1_CGMN1[1:0]		G1_VRN2[5:0]					
	initial	-	0	0	0	1	0	1	0	1
	recommend	-	0	1	0	0	1	1	0	1
		1	G1_CGMN2[1:0]		G1_VRN3[5:0]					
	initial	-	0	0	1	0	0	1	0	0
	recommend	-	0	1	0	1	0	1	0	1
		1	G1_CGMN3[1:0]		G1_VRN4[5:0]					
	initial	-	0	0	1	0	0	1	1	1
	recommend	-	0	1	0	1	1	1	1	1
		1	G1_CGMN5	G1_CGMN4	G1_VRN5[5:0]					
	initial	-	0	0	1	0	0	1	1	1
	recommend	-	1	1	1	1	1	1	0	1
		1	-	G1_PRN0[6]	-	G1_PKN0[4:0]				
	initial	-	0	0	0	0	0	1	1	0
	recommend	-	0	0	0	0	1	0	1	0
		1	G1_PRN0[5:4]		-	G1_PKN1[4:0]				
	initial	-	1	0	0	0	1	1	0	1
	recommend	-	0	1	0	0	1	1	1	0
		1	G1_PRN0[3:2]		-	G1_PKN2[4:0]				
	initial	-	0	0	0	1	0	0	0	1
	recommend	-	0	1	0	1	0	0	0	1
		1	G1_PRN0[1:0]		-	G1_PKN3[4:0]				
	initial	-	1	1	0	1	0	1	0	1
	recommend	-	1	1	0	1	0	0	1	1
		1	-	G1_PRN1[6]	-	G1_PKN4[4:0]				
	initial	-	0	0	0	1	0	1	1	0
	recommend	-	0	0	0	1	0	1	1	1
		1	G1_PRN1[5:4]		-	G1_PKN5[4:0]				
	initial	-	1	1	0	1	0	1	1	0
	recommend	-	1	0	0	1	0	0	0	1
		1	G1_PRN1[3:2]		-	G1_PKN6[4:0]				
	initial	-	1	0	0	1	0	1	1	1
	recommend	-	1	0	0	1	0	1	1	0
		1	G1_PRN1[1:0]		-	G1_PKN7[4:0]				
	initial	-	0	0	0	0	1	0	0	1
	recommend	-	0	1	0	0	1	1	1	0
		1	-	-	-	G1_PKN8[4:0]				
	initial	-	0	0	0	0	1	0	0	1
	recommend	-	0	0	0	1	0	0	0	1
FE	SET SPI READ INDEX	0	1	1	1	1	1	1	1	0
		1	CMD_ADD[7:0]							
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
FF	SPIREAD	0	1	1	1	1	1	1	1	1
		1	CMD_DATA1[7:0]							
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
		1	...							
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
		1	CMD_DATAN[7:0]							
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-

8. Sequence

Power on sequence

№		Function	DNC	Command/Parameter
		RESETB=0		
	Wait	wait 1 msec or more		
	Power on	IOVCC, VCC on		
	Wait	wait 10 msec or more		
		RESETB=1		
	Wait	wait 10 msec or more		
	RGB signals	RGB signals start		
	Wait	wait 2 frames or more		
1	Enable extended commands	Enable extended commands	0	B9h
		Parameter 1	1	FFh
		Parameter 2	1	83h
		Parameter 3	1	63h
2	Set power	Set power	0	B1h
		Parameter 1	1	81h
		Parameter 2	1	24h
		Parameter 3	1	04h
		Parameter 4	1	02h
		Parameter 5	1	02h
		Parameter 6	1	03h
		Parameter 7	1	10h
		Parameter 8	1	10h
		Parameter 9	1	34h
		Parameter 10	1	3Ch
		Parameter 11	1	3Fh
		Parameter 12	1	3Fh
3	Sleep out	Sleep out	0	11h
	Wait	wait 5 msec or more		
4	Display inversion off	Display inversion off	0	20h
5	Memory access control	Memory access control	0	36h
		Parameter 1	1	00h
6	Interface pixel format	Interface pixel format	0	3Ah
		Parameter 1	1	70h
	Wait	wait 120 msec or more		
7	Set power	Set power	0	B1h
		Parameter 1	1	78h
		Parameter 2	1	24h
		Parameter 3	1	04h
		Parameter 4	1	02h
		Parameter 5	1	02h
		Parameter 6	1	03h
		Parameter 7	1	10h
		Parameter 8	1	10h
		Parameter 9	1	34h
		Parameter 10	1	3Ch
		Parameter 11	1	3Fh
		Parameter 12	1	3Fh
8	Set RGB interface related register	Set RGB interface related register	0	B3h
		Parameter 1	1	01h
9	Set display waveform cycle	Set display waveform cycle	1	B4h
		Parameter 1	1	00h
		Parameter 2	1	08h
		Parameter 3	1	56h
		Parameter 4	1	07h
		Parameter 5	1	01h
		Parameter 6	1	01h
		Parameter 7	1	4Dh
		Parameter 8	1	01h
		Parameter 9	1	42h

№		Function	DNC	Command/Parameter
10	Set panel	Set panel	0	CCh
		Parameter 1	1	0Bh
11	Set gamma curve related setting	Set gamma curve related setting	0	E0h
		Parameter 1	1	01h
		Parameter 2	1	48h
		Parameter 3	1	4Dh
		Parameter 4	1	4Eh
		Parameter 5	1	58h
		Parameter 6	1	F6h
		Parameter 7	1	0Bh
		Parameter 8	1	4Eh
		Parameter 9	1	12h
		Parameter 10	1	D5h
		Parameter 11	1	15h
		Parameter 12	1	95h
		Parameter 13	1	55h
		Parameter 14	1	8Eh
		Parameter 15	1	11h
		Parameter 16	1	01h
		Parameter 17	1	48h
		Parameter 18	1	4Dh
		Parameter 19	1	55h
		Parameter 20	1	5Fh
		Parameter 21	1	FDh
		Parameter 22	1	0Ah
		Parameter 23	1	4Eh
		Parameter 24	1	51h
		Parameter 25	1	D3h
		Parameter 26	1	17h
		Parameter 27	1	95h
		Parameter 28	1	96h
		Parameter 29	1	4Eh
		Parameter 30	1	11h
	Wait	wait 5 msec or more		
12	Display on	Display on	0	29h

Power off sequence

No		Function	DNC	Command/Parameter
1	Display off	Display off	0	28h
	Wait	wait 5 msec or more		
2	Sleep in	Sleep in	0	10h
	Wait	wait 2 frames or more		
3	RGB signals	RGB signals stop		



Power off

Sleep sequence

No		Function	DNC	Command/Parameter
1	Sleep in	Sleep in	0	10h
	Wait	wait 2 frames or more		
2	RGB signals	RGB signals stop		

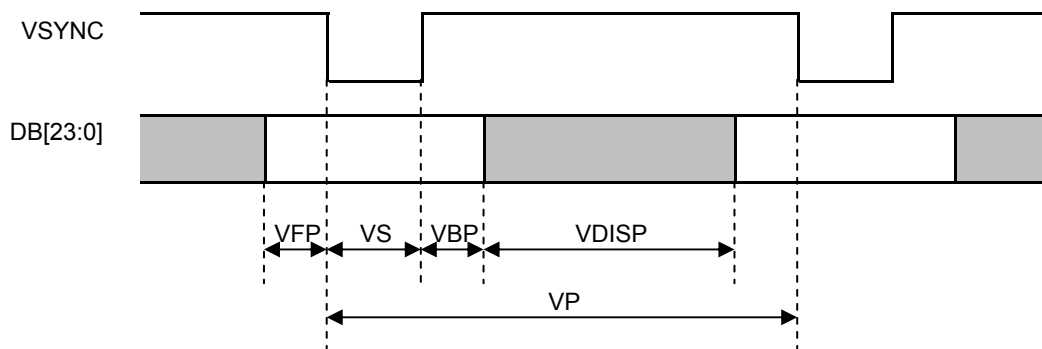
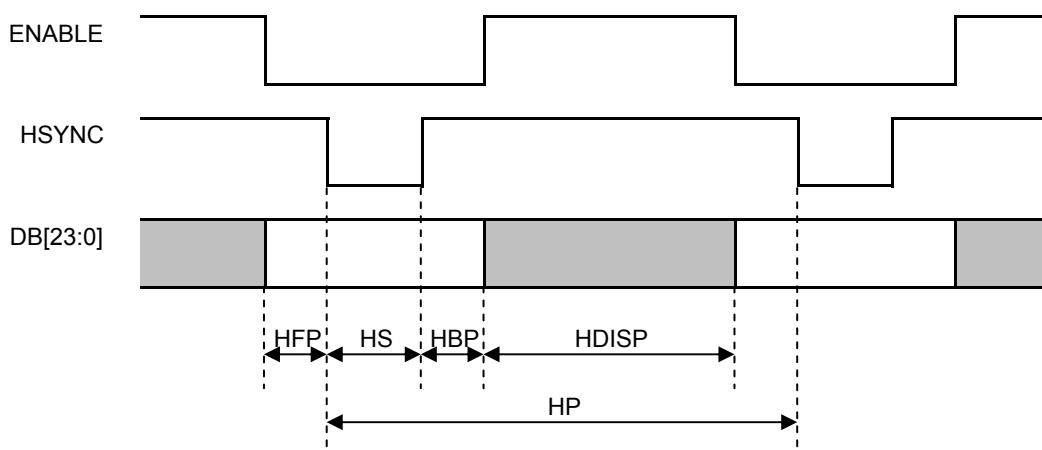
Sleep release sequence

No		Function	DNC	Command/Parameter
1	RGB signals	RGB signals start		
	Wait	wait 2 frames or more		
2	Sleep out	Sleep out	0	11h

9. RGB Interface

Recommended RGB interface timing

Item	Symbol	Recommended	Unit
Vertical cycle	VP	806	Line
Vertical low pulse width	VS	2	Line
Vertical front porch	VFP	2	Line
Vertical back porch	VBP	2	Line
Vertical active area	VDISP	800	Line
Vertical refresh rate	VRR	75	Hz
HS cycle	HP	508	DOTCLK
HS low pulse width	HS	10	DOTCLK
Horizontal back porch	HBP	10	DOTCLK
Horizontal front porch	HFP	8	DOTCLK
Horizontal active area	HDISP	480	MHz
Pixel clock frequency	DCK	30.72	MHz

Vertical timingHorizontal timing

10. Absolute Maximum Rating

Item	Symbol	Condition	Rating		Unit	Terminal
			MIN	MAX		
Power supply voltage	VCC		-0.3	4.6	V	VCC
IO logic voltage	IOVCC		-0.3	4.6	V	IOVCC
Input voltage	VI		-0.3	IOVCC+0.3	V	RESETB, SDI, SCL, CSB, VSYNC, HSYNC, DOTCLK, ENABLE, DB[23:0]
LED current	ILED		0	25	mA	VLED, LED1, ..., LEDn
Storage temperature	Tstg		-30	+80	°C	

11. Recommended Operating Conditions

Item	Symbol	Rating			Unit	Terminal
		MIN	TYP	MAX		
Supply voltage	VCC	2.6	2.7	2.9	V	VCC
IO logic voltage	IOVCC	1.7	1.8	1.9	V	IOVCC (VCC ≥ IOVCC)
LED current	ILED		8.5		mA	VLED, LED1, LEDn
Operation temperature	Top	-20	+25	+70	°C	Temperature at the surface of the display

12. Electrical Characteristics

12.1 DC Characteristics

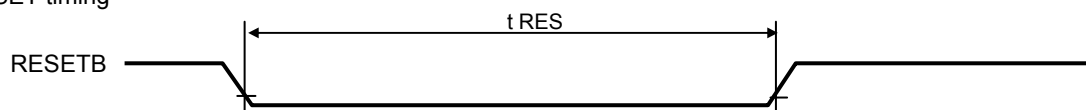
If no conditions are specified, then VCC=2.7V, IOVCC=1.8V, Ta=25°C

Items	Symbol	Condition	Rating			Unit	Terminal
			MIN	TYP	MAX		
High level input voltage	VIH1		0.7 IOVCC		IOVCC	V	RESETB, SDI, SCL, CSB, VSYNC, HSYNC, DOTCLK, ENABLE, DB[23:0]
Low level input voltage	VIL1		0		0.3 IOVCC	V	
Current Consumption	ICC1	VCC=2.7V, IOVCC=1.8V Still image *		12.0		mA	VCC
	ICC2	VCC=2.7V, IOVCC=1.8V stand by		10.0		µA	
	IOICC1	VCC=2.7V, IOVCC=1.8V Still image *		12.0		µA	IOVCC
	IOICC2	VCC=2.7V, IOVCC=1.8V stand by		1.0		µA	

* A still image (color bar) on display, when accessing to the driver by RGB interface mode.

12.2 AC Characteristics

RESET timing



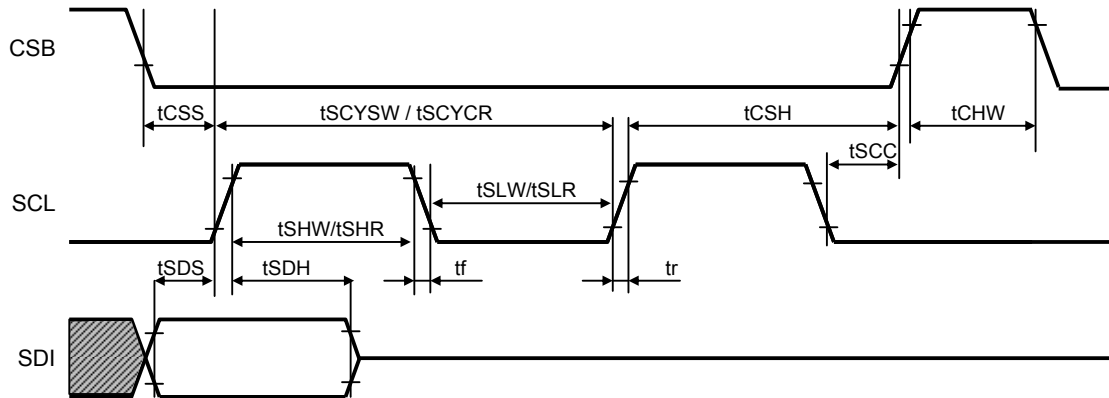
Reset low pulse width shorter than 10us do not make reset. It means undesired short pulse such as glitch, bouncing noise or electrostatic discharge do not cause irregular system reset. Please refer to the table below.

RESET timing spec

Item	Symbol	Condition	Rating			Unit
			MIN	TYP	MAX	
Reset low pulse width	tRES		10	-	-	μs

tRES Pulse	Action
Shorter than 5μs	No reset
Longer than 10μs	Reset
Between 5μs and 10μs	Not determined

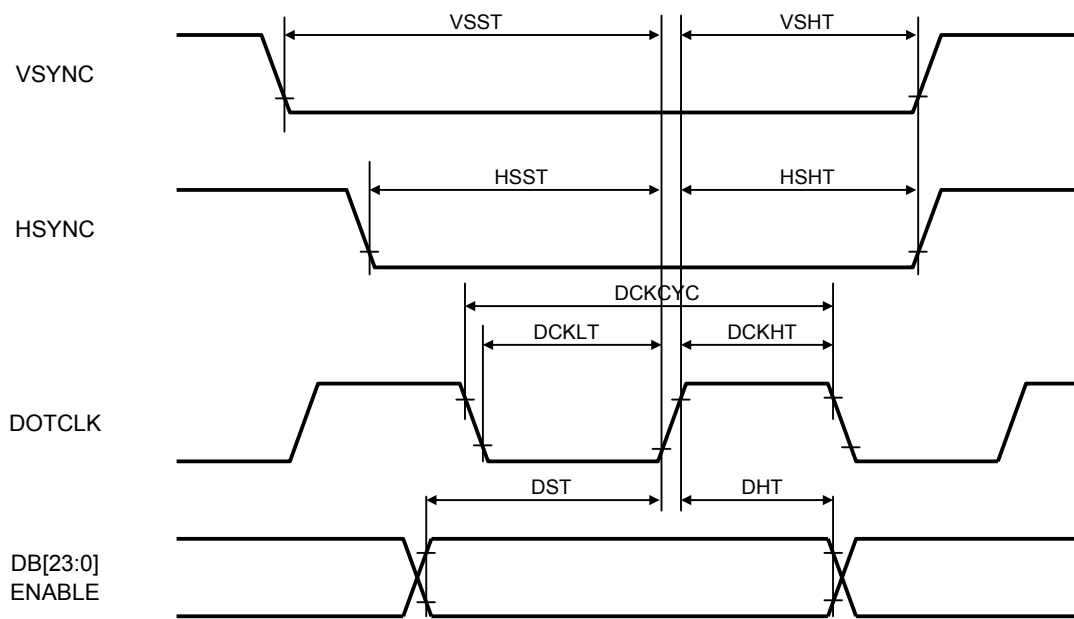
Serial Peripheral Interface(SPI)



Item	Symbol	Condition	Rating			Unit
			MIN	TYP	MAX	
Serial Clock Write Cycle	tSCYCW		100		-	ns
Serial Clock Read Cycle	tSCYCR		200		-	ns
Pulse Width High at Write	tSHW		50		-	ns
Pulse Width High at Read	tSHR		100		-	ns
Pulse Width Low at Write	tSLW		50		-	ns
Pulse Width Low at Read	tSLR		100		-	ns
CSB Setup Time at Write	tCSS		50		-	ns
CSB Setup Time at Read	tCSS		100		-	ns
CSB Hold Time at Write	tSCH		50		-	ns
CSB Hold Time at Read	tSCH		100		-	ns
SDI Setup Time	tSDS		50		-	ns
SDI Hold Time	tSDH		50		-	ns
Rising/Falling Time	tR, tF		-		10	ns

Remarks 1. All timing data is specified at 30 to 70% of VCCIO.

24 bit RGB interface



Item	Symbol	Condition	Rating			Unit
			MIN	TYP	MAX	
VSYNC Setup Time	VSST		10	-	-	ns
VSYNC Hold Time	VSHT		10	-	-	ns
HSYNC Setup Time	HSST		10	-	-	ns
HSYNC Hold Time	HSHT		10	-	-	ns
DOTCLK Clock Cycle	DCKCYC	Frame Frequency= 50 to 70 Hz	31	-	49.2	ns
DOTCLK Low Time	DCKLT		10	-	-	ns
DOTCLK High Time	DCKHT		10	-	-	ns
Data Setup Time for DB[23:0]	DST		10	-	-	ns
Data Hold Time for DB[23:0]	DHT		10	-	-	ns

Note: (1) Signal rise and fall times are equal to or less than 20 ns.

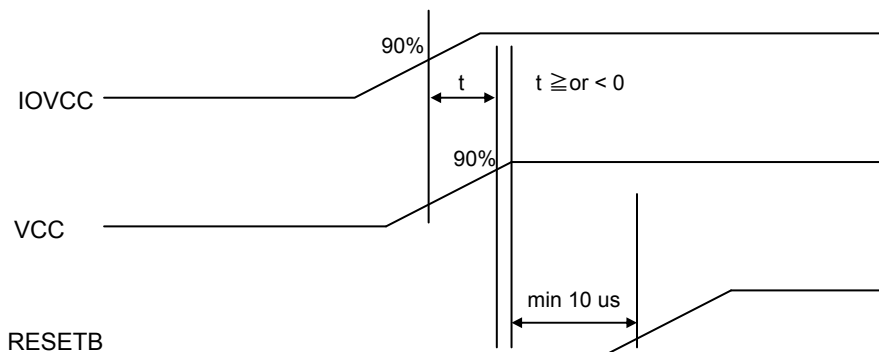
(2) Input signals are measured by $0.30 \times IOVCC$ for low state and $0.70 \times IOVCC$ for high state.

13. External Power on / off Sequence

13.1 External Power On sequence

VCC and IOVCC can be applied in any order.

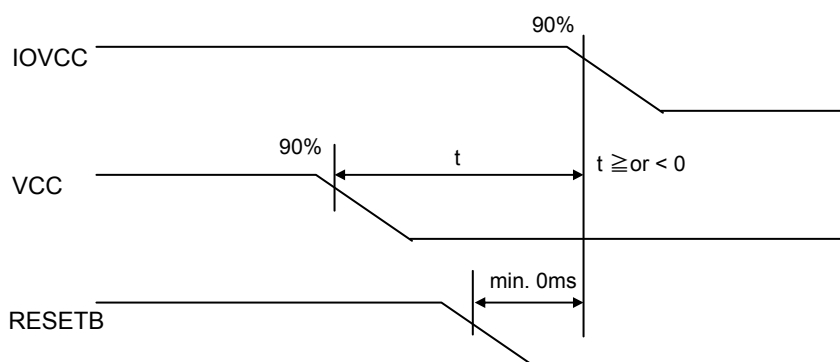
RESETB must be kept low for minimum 10 usec after both VCC and IOVCC have reached it's target voltage.



13.2 External Power Off sequence

VCC and IOVCC can be powered down in any order.

If the module is in "Sleep In" mode, IOVCC and VCC can be powered down minimum 0 msec after RESETB has been released.



14. Characteristics

14.1 Optical Characteristics

< Measurement Condition >

Measuring instruments: CS1000 (KONICA MINOLTA) , LCD7200(OTSUKA ELECTRONICS) ,
EZcontrast160D (ELDIM)

Driving condition: VCC=2.7V, IOVCC=1.8V
Optimized VCOMDC

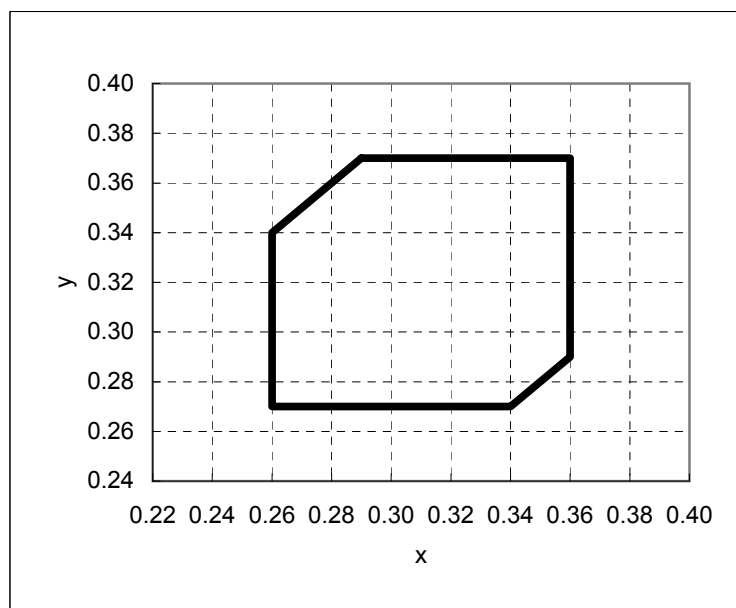
Backlight: IL=8.5mA

Measured temperature: Ta=25° C

Item		Symbol	Condition	MIN	TYP	MAX	Unit	Note No.	Remark
Response time	Rise time	TON	[Data]= 00h → FFh	—	—	40	ms	1	※
	Fall time	TOFF	[Data]= FFh → 00h	—	—	60	ms		
Contrast ratio	Backlight ON	CR	[Data]= FFh / 00h	600	1000	—		2	
	Backlight OFF			—	2.9	—			
Viewing angle	Left	θL	[Data]= FFh / 00h CR ≥ 10	80	—	—	deg	3	※
	Right	θR		80	—	—	deg		
	Up	φU		80	—	—	deg		
	Down	φD		80	—	—	deg		
White Chromaticity	x	[Data]=FFh	White chromaticity range					4	
	y								
Burn-in				No noticeable burn-in image should be observed after 2 hours of window pattern display.				5	
Center brightness			[Data]=FFh	240	380	—	cd/m ²	6	
Brightness distribution			[Data]=FFh	70	—	—	%	7	

* Note number 1 to 7: Refer to the APPENDIX of "Reference Method for Measuring Optical Characteristics".

※ Measured in the form of LCD module.



White Chromaticity Range

【White Chromaticity Range】

x	y
0.29	0.37
0.26	0.34
0.26	0.27
0.34	0.27
0.36	0.29
0.36	0.37

14.2 Temperature Characteristics

< Measurement Condition >

Measuring instruments: CS1000 (KONICA MINOLTA) , LCD7200(OTSUKA ELECTRONICS)

Driving condition: VCC=2.7V, IOVCC=1.8V

Optimized VCOMDC

Backlight: IL=8.5mA

Item		Specification		Remark	
		Ta = -10 °C	Ta = 70 °C		
Contrast ratio	CR	40 or more	40 or more	Backlight ON	
Response time	Rise time	TON	200 msec or less	30 msec or less	※
	Fall time	TOFF	300 msec or less	50 msec or less	※
Display Quality		No noticeable display defect or nonuniformity should be observed.		Use the criteria for judgment specified in the section 15.	

※ Measured in the form of LCD module.

15. Criteria of Judgment

15.1 Defective Display and Screen Quality

Test Condition:	Observed TFT-LCD monitor from front during operation with the following conditions
Driving Signal	Raster Patter (RGB in monochrome, white, black)
Signal condition	[Data] = FFh, BCh, 00h (3steps)
Observation distance	30 cm
Illuminance	200 to 350 lx
Backlight	IL=8.5mA

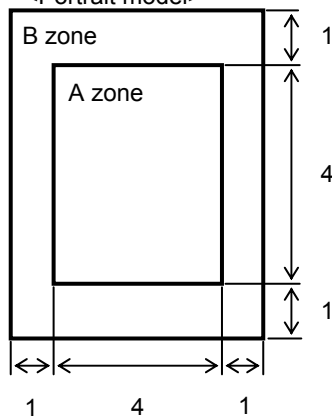
Defect item	Defect content	Criteria		
Display Quality	Line defect	Black, white or color line, 3 or more neighboring defective dots	Not exists	
	Dot defect	Uneven brightness on dot-by-dot base due to defective TFT or CF, or dust is counted as dot defect (brighter dot, darker dot)	Refer to table 1	
		High bright dot: Visible through 2% ND filter at [Data]=00h	Ignored	
		Low bright dot: Visible through 5% ND filter at [Data]=00h		
	Dark dot: Appear dark through white display at [Data]=BCh			
	Invisible through 5% ND filter at [Data]=00h	Ignored		
Screen Quality	Dirt	Uneven brightness (white stain, black stain etc)	Invisible through 1% ND filter	
	Foreign particle	Point-like	$0.25\text{mm} < \varphi$	$N=0$
			$0.20\text{mm} < \varphi \leq 0.25\text{mm}$	$N \leq 2$
			$\varphi \leq 0.20\text{mm}$	Ignored
		Liner	$3.0\text{mm} < \text{length and } 0.08\text{mm} < \text{width}$	$N=0$
	$\text{length} \leq 3.0\text{mm}$ or $\text{width} \leq 0.08\text{mm}$		Ignored	
Others		Use boundary sample for judgment when necessary		

$\varphi(\text{mm})$: Average diameter = (major axis + minor axis)/2
Permissible number: N

Table 1

Area	High bright dot	Low bright dot	Dark dot	Total	Criteria
A	0	2	2	3	Permissible distance between same color bright dots (includes neighboring dots): 3 mm or more Permissible distance between same color high bright dots (includes neighboring dots): 5 mm or more
B	2	4	4	6	
Total	2	4	4	6	

<Portrait model>



Division of A and B areas

B area: Active area

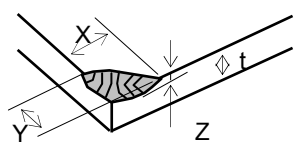
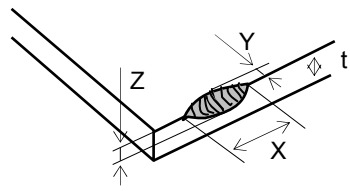
Dimensional ratio between A and B areas: 1: 4: 1 (Refer to the left figure)

15.2 Screen and Other Appearance

Testing conditions

Observation distance	30cm
Illuminance	1200~2000 lx

Item	Criteria	Remark
Polarizer Flaw Stain Bubble Dust Dent	Ignore invisible defect when the backlight is on.	Applicable area: Active area only (Refer to the section 3.2 "Outward form")
S-case	No functional defect occurs	
FPC cable	No functional defect occurs	

Item	Appearance	Criteria
Glass Chipping	Corner area 	Unit: mm $X \leq 3$ $Y \leq 3$ $Z \leq t$ (t:glass thickness) $X, Y \leq 0.5$ is ignored.
	Others 	Unit: mm $X \leq 5$ $Y \leq 1$ $Z \leq t$ (t:glass thickness) $X, Y \leq 0.5$ is ignored.
	Progressive crack	None

16. Reliability Test

Test item		Test condition		number of failures /number of examinations
Durability test	High temperature storage	Ta=80°C	240H	0/3
	Low temperature storage	Ta=-30°C	240H	0/3
	High temperature & high humidity storage	Ta=60°C, RH=90% non condensing	240H	0/3
	High temperature operation	Tp=70°C	240H	0/3
	Low temperature operation	Tp=-20°C	240H	0/3
	High temp & humid operation	Tp=40°C, RH=90% non condensing	240H	0/3
	Thermal shock storage	-30↔80°C(30min/30min)	100 cycles	0/3
Mechanical environmental test	Electrostatic discharge test (Non operation)	Confirms to EIAJ ED-4701/300 C=200pF,R=0Ω,V=±200V Each 3 times of discharge on and power supply and other terminals.		0/3
	Surface discharge test (Non operation)	C=250pF, R=100Ω, V=±6kV Each 5 times of discharge in both polarities on the center of screen with the case grounded.		0/3
	Vibration test	Total amplitude 1.5mm, f=10~55Hz, X,Y,Z directions for each 2 hours		0/3
	Impact test	Use ORTUS TECHNOLOGY original jig (see next page)and make an impact with peak acceleration of 1000m/s ² for 6 msec with half sine-curve at 3 times to each X, Y, Z directions in conformance with JIS C 60068-2-27-2011.		0/3
Packing test	Packing vibration-proof test	Acceleration of 19.6m/s ² with frequency of 10→55→10Hz, X,Y, Zdirection for each 30 minutes		0/1 Packing
	Packing drop test	Drop from 75cm high. 1 time to each 6 surfaces, 3 edges, 1 corner		0/1 Packing

Note: Ta=ambient temperature Tp=Panel temperature

※ The profile of high temperature/humidity storage and High Temperature/humidity operation (Pure water of over 10MΩ·cm shall be used.)

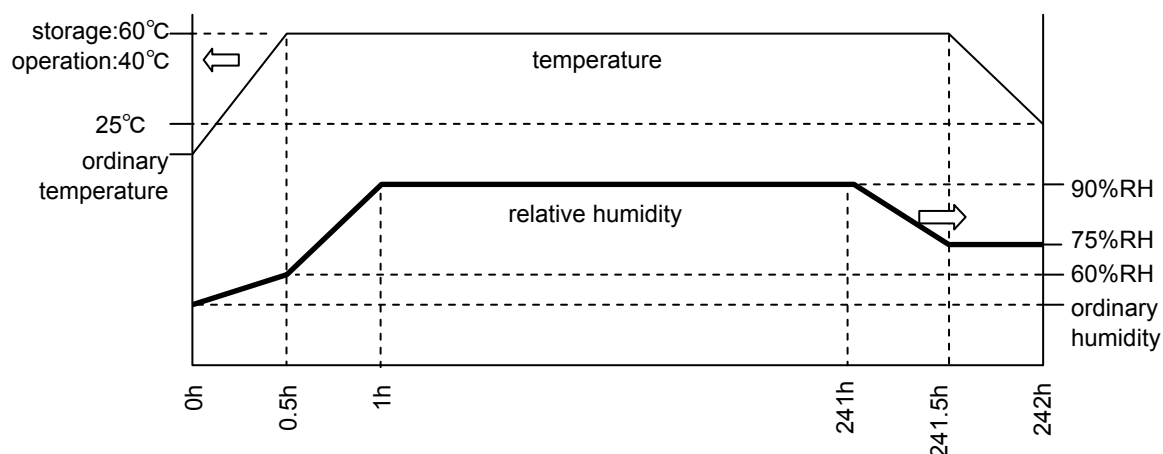
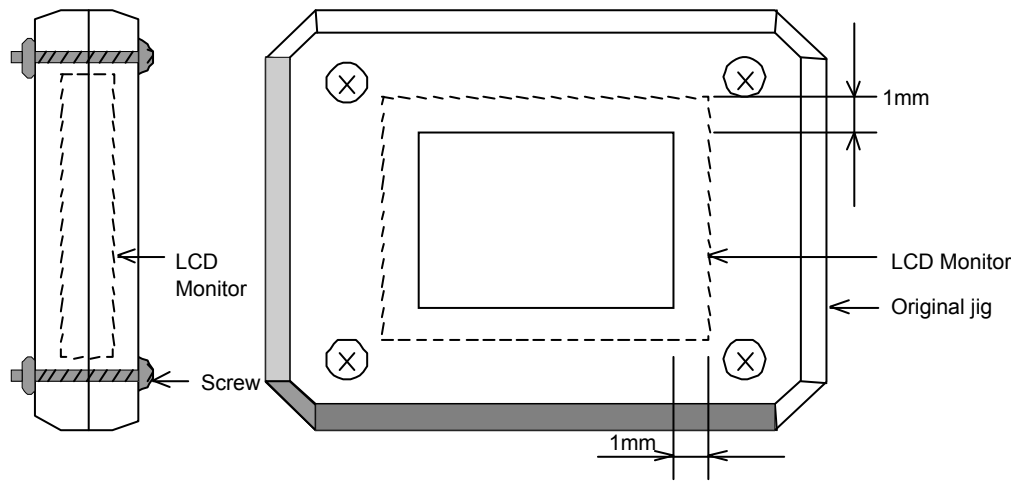


Table2.Reliability Criteria

The parameters should be measured after leaving the monitor at the ordinary temperature for 24 hours or more after the test completion.

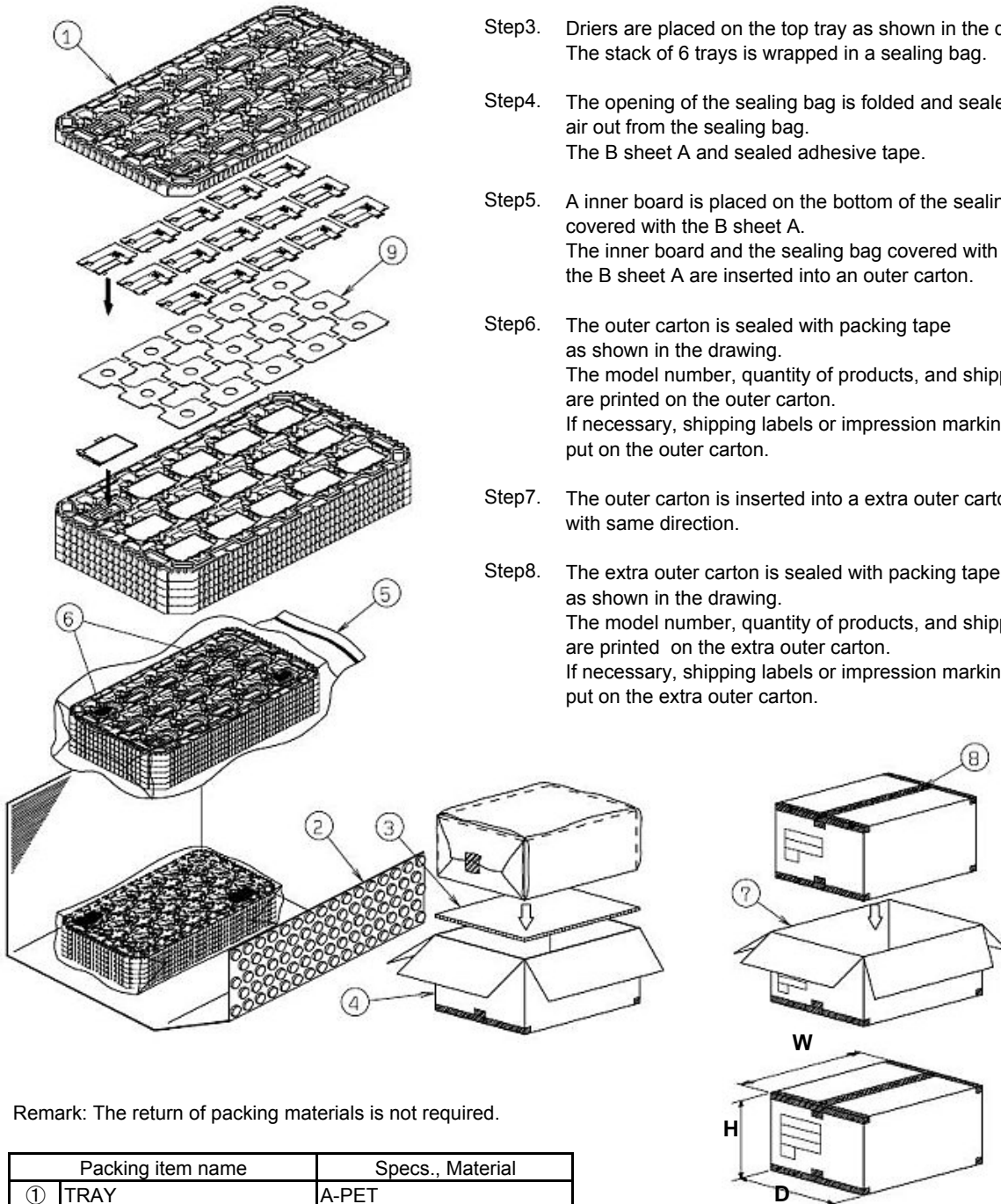
item	Standard	Remarks
Display quality	No visible abnormality shall be seen.	
Contrast ratio	40 or more	Backlight ON

ORTUS TECHNOLOGY Original Jig



17. Packing Specifications

- Step1. Each lower product is placed in one of the cut-outs of the tray with the LCD surface facing upward, and foam sheet is put on products, and upper products are placed facing downward. (30 pieces / 1 tray)
- Step2. 5 trays containing products are stacked. One empty tray is put on the top of the stack of 5 trays.
- Step3. Driers are placed on the top tray as shown in the drawing. The stack of 6 trays is wrapped in a sealing bag.
- Step4. The opening of the sealing bag is folded and sealed with air out from the sealing bag. The B sheet A and sealed adhesive tape.
- Step5. A inner board is placed on the bottom of the sealing bag covered with the B sheet A. The inner board and the sealing bag covered with the B sheet A are inserted into an outer carton.
- Step6. The outer carton is sealed with packing tape as shown in the drawing. The model number, quantity of products, and shipping date are printed on the outer carton. If necessary, shipping labels or impression markings are put on the outer carton.
- Step7. The outer carton is inserted into a extra outer carton with same direction.
- Step8. The extra outer carton is sealed with packing tape as shown in the drawing. The model number, quantity of products, and shipping date are printed on the extra outer carton. If necessary, shipping labels or impression markings are put on the extra outer carton.



Remark: The return of packing materials is not required.

	Packing item name	Specs., Material
①	TRAY	A-PET
②	B SHEET A	Anti-static air bubble sheet
③	INNER BOARD	Corrugated cardboard
④	OUTER CARTON	Corrugated cardboard
⑤	SEALING BAG	
⑥	Drier	Moisture absorber
⑦	EXTRA OUTER CARTON	Corrugated cardboard
⑧	SEALING BAG	
⑨	FOAM SHEET	Anti-static polyethylene

Dimension of extra outer carton	
D : Approx.	(337mm)
W : Approx.	(618mm)
H : Approx.	(179mm)
Quantity of products packed in one carton:	150
Gross weight : Approx.	5.0kg

18. Handling Instruction

18.1 Cautions for Handling LCD panels

**Caution**

- (1) Do not make an impact on the LCD panel glass because it may break and you may get injured from it.
- (2) If the glass breaks, do not touch it with bare hands.
(Fragment of broken glass may stick you or you cut yourself on it.)
- (3) If you get injured, receive adequate first aid and consult a medial doctor.
- (4) Do not let liquid crystal get into your mouth.
(If the LCD panel glass breaks, try not let liquid crystal get into your mouth even toxic property of liquid crystal has not been confirmed.)
- (5) If liquid crystal adheres, rinse it out thoroughly.
(If liquid crystal adheres to your cloth or skin, wipe it off with rubbing alcohol or wash it thoroughly with soap. If liquid crystal gets into eyes, rinse it with clean water for at least 15 minutes and consult an eye doctor.)
- (6) If you scrap this products, follow a disposal standard of industrial waste that is legally valid in the community, country or territory where you reside.
- (7) Do not connect or disconnect this product while its application products is powered on.
- (8) Do not attempt to disassemble or modify this product as it is precision component.
- (9) If a part of soldering part has been exposed, and avoid contact (short-circuit) with a metallic part of the case etc. about FPC of this model, please.
Please insulate it with the insulating tape etc. if necessary.
The defective operation is caused, and there is a possibility to generation of heat and the ignition.
- (10) Since excess current protection circuit is not built in this TFT module, there is the possibility that LCD module or peripheral circuit become feverish and burned in case abnormal operation is generated.
We recommend you to add excess current protection circuit to power supply.
- (11) The devices on the FPC are damageable to electrostatic discharge, because the terminals of the devices are exposed.
Wear grounded wrist-straps and use electrostatic neutralization blowers to prevent static charge and discharge when handling the TFT monitors.
Designate an appropriate operating area, and set equipment, tools, and machines properly when handling this product.

**Caution**

This mark is used to indicate a precaution or an instruction which, if not correctly observed, may result in bodily injury, or material damages alone.

18.2 Precautions for Handling

- 1) Wear finger tips at incoming inspection and for handling the TFT monitors to keep display quality and keep the working area clean.
Do not touch the surface of the monitor as it is easily scratched.
- 2) Wear grounded wrist-straps and use electrostatic neutralization blowers to prevent static charge and discharge when handling the TFT monitors as the LED in this TFT monitors is damageable to electrostatic discharge.
Designate an appropriate operating area, and set equipment, tools, and machines properly when handling this product.
- 3) Avoid strong mechanical shock including knocking, hitting or dropping to the TFT monitors for protecting their glass parts. Do not use the TFT monitors that have been experienced dropping or strong mechanical shock.
- 4) Do not use or storage the TFT monitors at high temperature and high humidity environment. Particularly, never use or storage the TFT monitors at a location where condensation builds up.
- 5) Avoid using and storing TFT monitors at a location where they are exposed to direct sunlight or ultraviolet rays to prevent the LCD panels from deterioration by ultraviolet rays.
- 6) Do not stain or damage the contacts of the FPC cable .
FPC cable needs to be inserted until it can reach to the end of connector slot.
During insertion, make sure to keep the cable in a horizontal position to avoid an oblique insertion.
Otherwise, it may cause poor contact or deteriorate reliability of the FPC cable.
- 7) The FPC cable is a design very weak to the bend and the pull as it is fixed with the tape.
Do not bend or pull the FPC cable or carry the TFT monitor by holding the FPC cable.
- 8) Peel off the protective film on the TFT monitors during mounting process.
Refer to the section 18.5 on how to peel off the protective film.
We are not responsible for electrostatic discharge failures or other defects occur when peeling off the protective film.
- 9) Please make it to the structure to suppress surroundings of the front polarizer for the display irregularity prevention.

18.3 Precautions for Operation

- 1) Since this TFT monitors are not equipped with light shielding for the driver IC, do not expose the driver IC to strong lights during operation as it may cause functional failures.
- 2) In case of powering up or powering off this LCD module, be sure to comply the sequence as instructed in this specification.
- 3) Optimize VCOMDC within recommended operating conditions.
* When VCOMDC is not an optimal value, flicker and image sticking will be occurred.
- 4) Do not plug in or out the FPC cable while power supply is switch on.
Plug the FPC cable in and out while power supply is switched off.
- 5) Do not operate the TFT monitors in the strong magnetic field. It may break the TFT monitors.
- 6) Do not display a fixed image on the screen for a long time.
Use a screen-saver or other measures to avoid a fixed image displayed on the screen for a long time.
Otherwise, it may cause burn-in image on the screen due the characteristics of liquid crystal.

18.4 Storage Condition for Shipping Cartons

Storage environment

- Temperature 0 to 40° C
- Humidity 60%RH or less
No-condensing occurs under low temperature with high humidity condition.
- Atmosphere No poisonous gas that can erode electronic components and/or wiring materials should be detected.
- Time period 3 months
- Unpacking To prevent damages caused by static electricity, anti-static precautionary measures (e.g. earthing, anti-static mat) should be implemented.
- Maximum piling up 7 cartons

18.5 Precautions for Peeling off the Protective film

The followings work environment and work method are recommended to prevent the TFT monitors from static damage or adhesion of dust when peeling off the protective films.

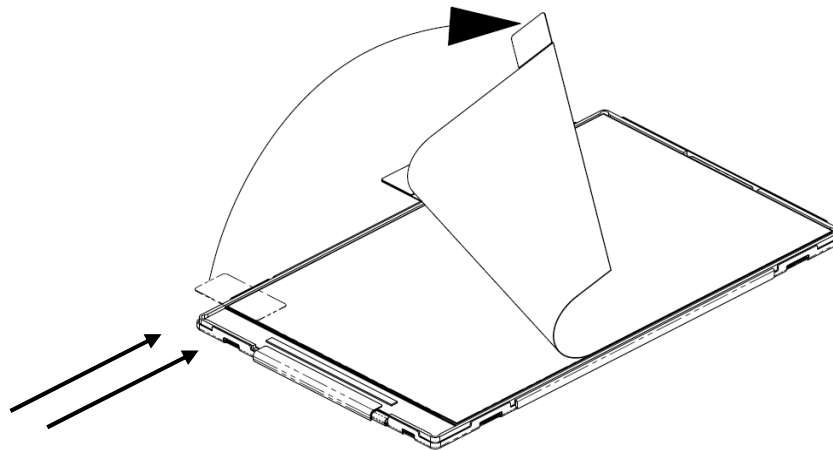
A) Work Environment

- a) Humidity: 50 to 70 %RH, Temperature 15 to 27° C
- b) Operators should wear conductive shoes, conductive clothes, conductive finger tips and grounded wrist-straps. Anti-static treatment should be implemented to work area's floor.
- c) Use a room shielded against outside dust with sticky floor mat laid at the entrance to eliminate dirt.

B) Work Method

The following procedures should taken to prevent the driver ICs from charging and discharging.

- a) Use an electrostatic neutralization blower to blow air on the TFT monitors to its lower left when LSI is placed at the bottom.
Optimize direction of the blowing air and the distance between the TFT monitors and the electrostatic neutralization blower.
- b) Peel off the tab slowly (spending more than 2 secs to complete) by pulling it to opposite direction.



Direction of blowing air
(Optimize air direction and the distance)

APPENDIX

Reference Method for Measuring Optical Characteristics and Performance

1. Measurement Condition (Backlight ON)

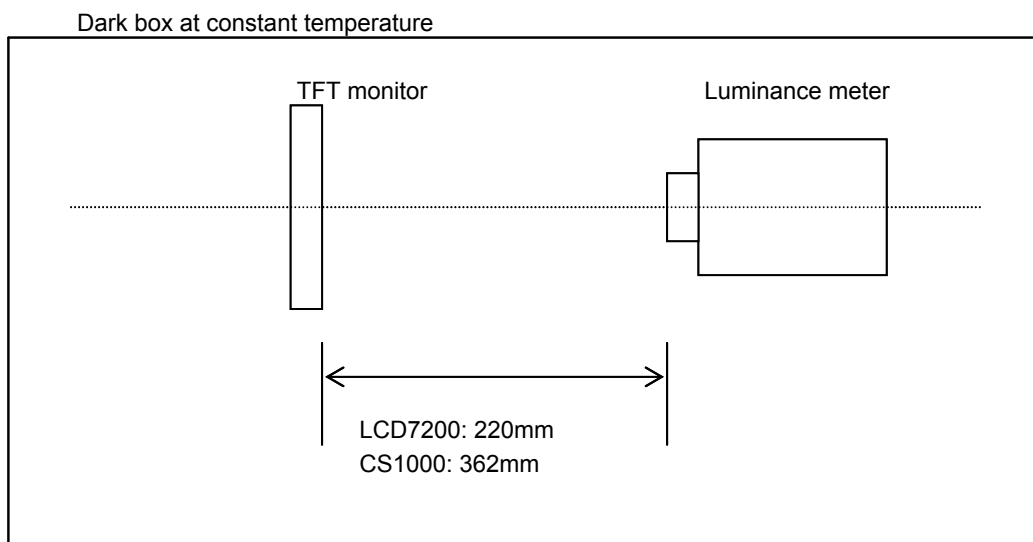
Measuring instruments: CS1000 (KONICA MINOLTA) , LCD7200(OTSUKA ELECTRONICS) ,EZcontrast160D (ELDIM)

Driving condition: Refer to the section "Optical Characteristics"

Measured temperature: 25° C unless specified

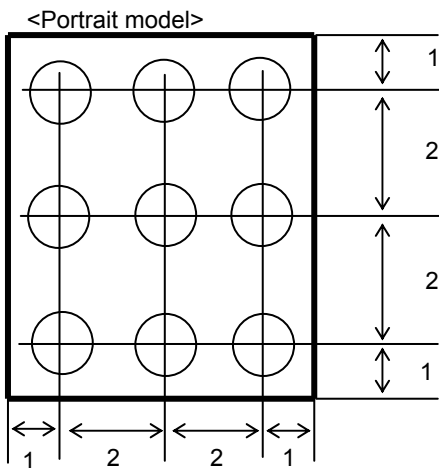
Measurement system: See the chart below. The luminance meter is placed on the normal line of measurement system.

Measurement point: At the center of the screen unless otherwise specified



Measurement is made after 30 minutes of lighting of the backlight.

Measurement point: At the center point of the screen
Brightness distribution: 9 points shown in the following drawing.



Dimensional ratio of active area

Backlight IL=8.5mA

Measurement Condition (Contrast ratio Backlight OFF only)

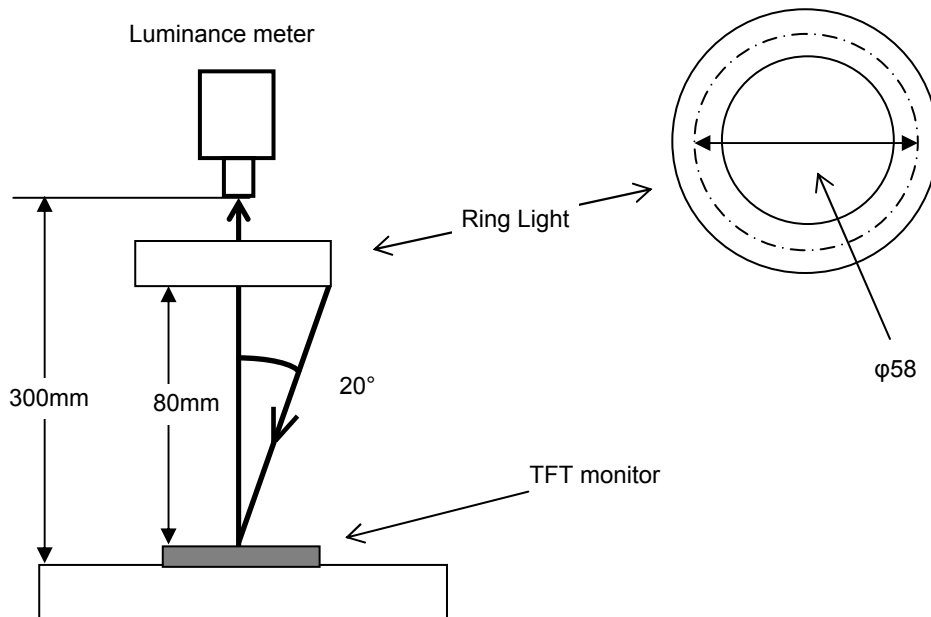
Measuring instruments: LCD7200(OTSUKA ELECTRONICS),Ring Light(40,000 lx, ϕ 58)

Driving condition: Refer to the section "Optical Characteristics"

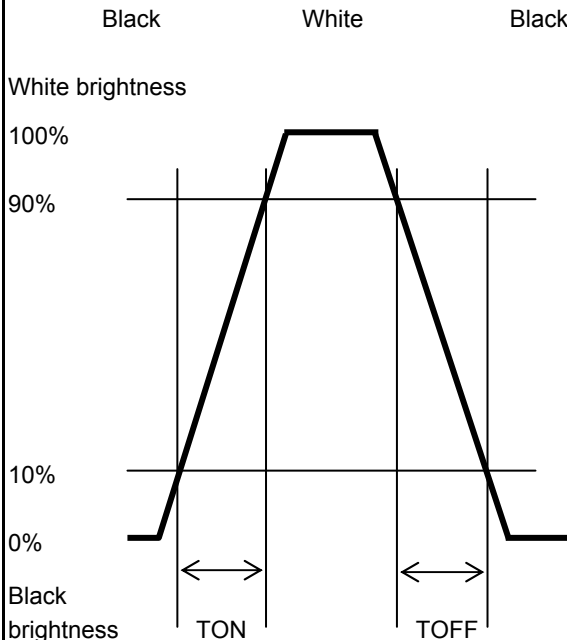
Measured temperature: 25° C unless specified

Measurement system: See the chart below.

Measurement point: At the center of the screen.



2. Test Method

Notice	Item	Test method	Measuring instrument	Remark
1	Response time	<p>Measure output signal waveform by the luminance meter when raster of window pattern is changed from white to black and from black to white.</p>  <p>Black White Black</p> <p>White brightness</p> <p>100%</p> <p>90%</p> <p>10%</p> <p>0%</p> <p>Black brightness</p> <p>TON</p> <p>TOFF</p>	LCD7200	<p>Black display [Data]=00h</p> <p>White display [Data]=FFh</p> <p>TON</p> <p>Rise time</p> <p>TOFF</p> <p>Fall time</p>
2	Contrast ratio	<p>Measure maximum luminance Y1([Data]=FFh) and minimum luminance Y2([Data]=00h) at the center of the screen by displaying raster or window pattern. Then calculate the ratio between these two values.</p> <p>Contrast ratio = Y1/Y2</p> <p>Diameter of measuring point: 8mmφ</p>	CS1000 LCD7200	Backlight ON Backlight OFF
3	Viewing angle Horizontalθ Verticalφ	Move the luminance meter from right to left and up and down and determine the angles where contrast ratio is 10.	EZcontrast160D	
4	White chromaticity	<p>Measure chromaticity coordinates x and y of CIE1931 colorimetric system at [Data] = FFh</p> <p>Color matching faction: 2°view</p>	CS1000	
5	Burn-in	Visually check burn-in image on the screen after 2 hours of "window display" ([Data]=00h/FFh).		
6	Center brightness	Measure the brightness at the center of the screen.	CS1000	
7	Brightness distribution	<p>(Brightness distribution) = 100 x B/A %</p> <p>A : max. brightness of the 9 points</p> <p>B : min. brightness of the 9 points</p>	CS1000	