

# SPECIFICATION

**PART NO. : OEL9M0093-W-E**

**OLED  
Display**  

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**72 X 32**

**0.48"**

This specification may be changed without any notice in order to improve performance or quality etc.

Please contact OLED R&D department TRULY Semiconductors LTD. For updated specification and product status before design for this product or release the order.

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|                 |               |             |  |
|-----------------|---------------|-------------|--|
| <b>TRULY®信利</b> |               | Customer    |  |
| Written by      | ChenYongquan  | Approved by |  |
| Checked by      | Yang Xueyu    |             |  |
| Approved by     | Zhang Weicang |             |  |



**■ PHYSICAL DATA**

| No. | Items:                    | Specification:        | Unit            |
|-----|---------------------------|-----------------------|-----------------|
| 1   | Diagonal Size             | 0.48                  | Inch            |
| 2   | Resolution                | 72(H) x 32(V)         | Dots            |
| 3   | Active Area               | 11.210 (W) x 4.970(H) | mm <sup>2</sup> |
| 4   | Outline Dimension (Panel) | 14.90 (W) x 11.29(H)  | mm <sup>2</sup> |
| 5   | Pixel Pitch               | 0.156 (W) x 0.156(H)  | mm <sup>2</sup> |
| 6   | Pixel Size                | 0.136(W) x 0.136(H)   | mm <sup>2</sup> |
| 7   | Driver IC                 | SSD1309Z              | -               |
| 8   | Display Color             | White                 | -               |
| 9   | Gray scale                | 1                     | Bit             |
| 10  | Interface                 | 4-SPI                 | -               |
| 11  | IC package type           | COG                   | -               |
| 12  | Thickness                 | 1.20±0.1              | mm              |
| 13  | Weight                    | TBD                   | g               |
| 14  | Duty                      | 1/32                  | -               |

**■ ABSOLUTE MAXIMUM RATINGS**

 Unless otherwise specified,  $V_{SS} = 0V$ 

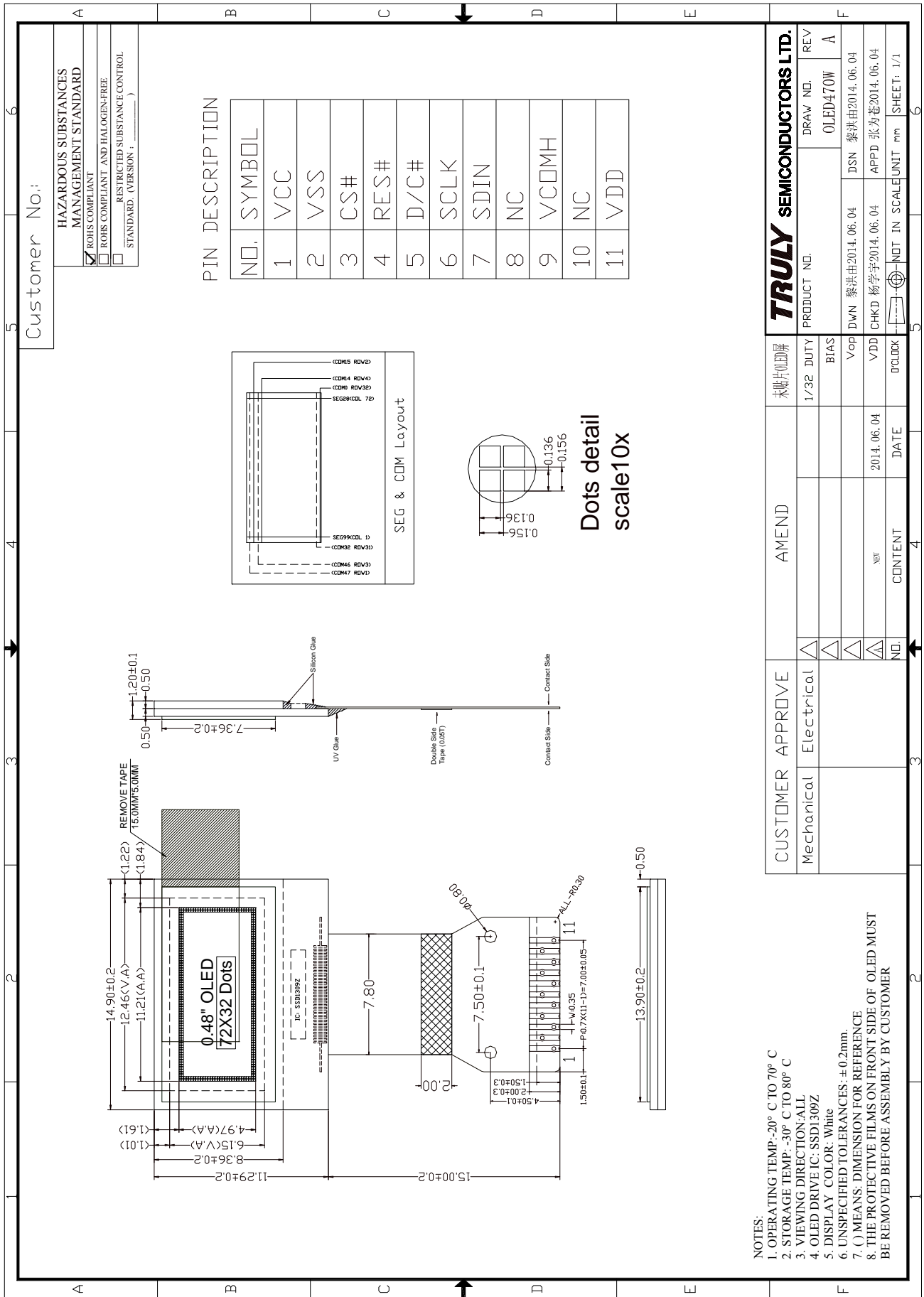
 (  $T_a = 25^{\circ}C$  )

| Items                 |         | Symbol | Min  | Typ. | Max  | Unit |
|-----------------------|---------|--------|------|------|------|------|
| Supply Voltage        | Logic   | VDD    | -0.3 | -    | 4.0  | V    |
|                       | Driving | VCC    | 0    | -    | 17.0 | V    |
| Operating Temperature |         | Top    | -20  | -    | 70   | °C   |
| Storage Temperature   |         | Tst    | -30  | -    | 80   | °C   |
| Humidity              |         | -      | -    | -    | 90   | %RH  |

**Note:**

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

EXTERNAL DIMENSIONS



|                                  |                      |
|----------------------------------|----------------------|
| <b>TRULY SEMICONDUCTORS LTD.</b> |                      |
| PRODUCT NO.                      | OLE470W A            |
| REV                              | A                    |
| 1/32 DUTY                        | BIAS                 |
| Vop                              | VDD                  |
| DWN 黎洪由2014.06.04                | CHKD 杨学宇2014.06.04   |
| DATE                             | 2014.06.04           |
| CONTENT                          | NO. IN SCALE UNIT mm |
| AMEND                            | 未做片阻屏                |
| CUSTOMER APPROVE                 | Electrical           |
| Mechanical                       |                      |

**■ ELECTRICAL CHARACTERISTICS****◆ DC Characteristics**

Unless otherwise specified,  $V_{SS} = 0V$ ,  $V_{DD} = 1.65V$  to  $3.3V$ . (  $T_a = 25^\circ C$  )

| Items          |              | Symbol   | Min                 | Typ. | Max                 | Unit |
|----------------|--------------|----------|---------------------|------|---------------------|------|
| Supply Voltage | Logic        | VDD      | 1.65                | 3    | 3.3                 | V    |
|                | Driving      | VCC      | 7.0                 | 10.0 | 16.0                | V    |
| Input Voltage  | High Voltage | $V_{IH}$ | $0.8 \times V_{DD}$ | -    | -                   | V    |
|                | Low Voltage  | $V_{IL}$ | -                   | -    | $0.2 \times V_{DD}$ | V    |
| Output Voltage | High Voltage | $V_{OH}$ | $0.9 \times V_{DD}$ | -    | -                   | V    |
|                | Low Voltage  | $V_{OL}$ | -                   | -    | $0.1 \times V_{DD}$ | V    |

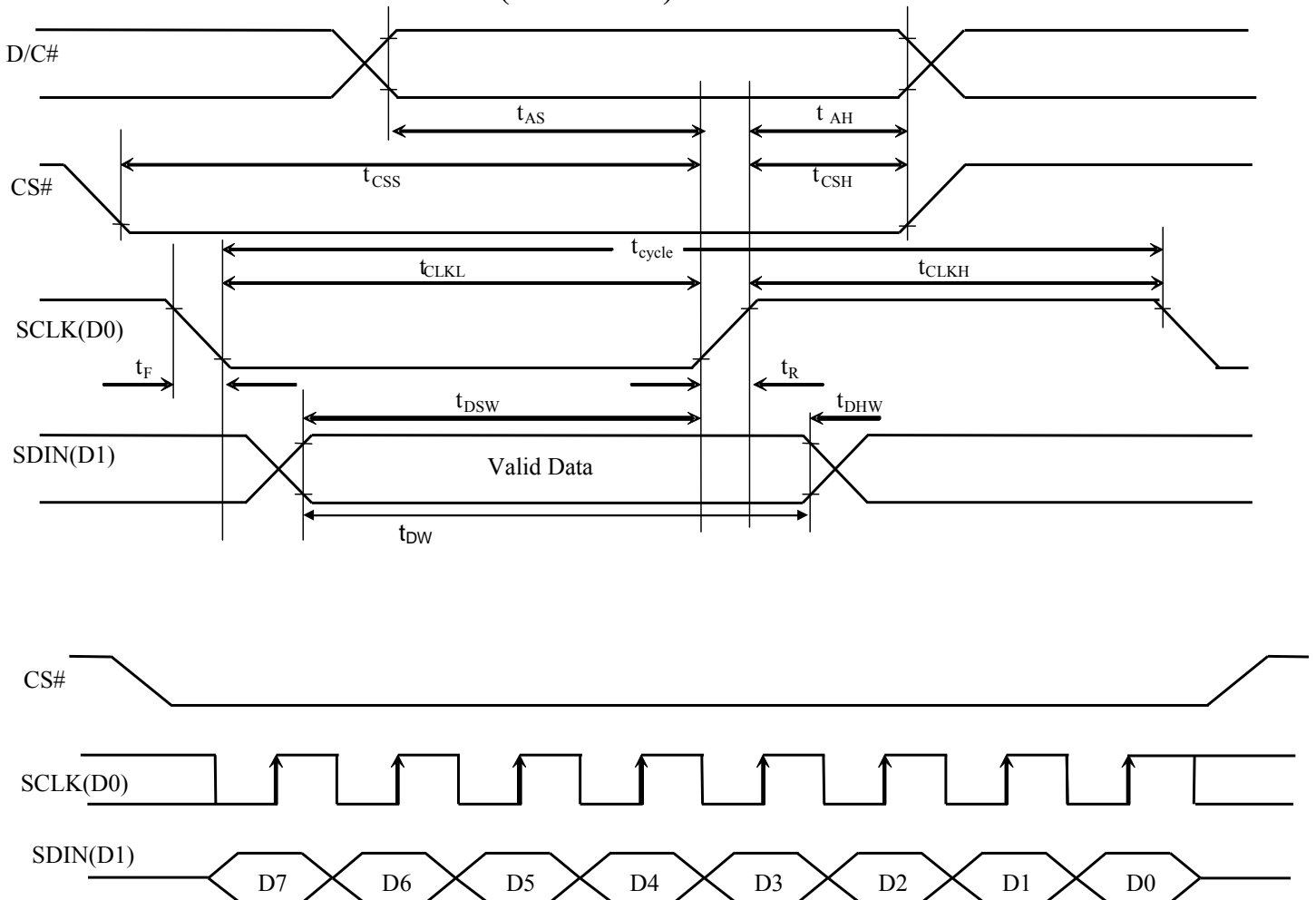
◆ AC Characteristics

Serial Interface Timing Characteristics (4-wire SPI)

(VDD - VSS=1.65~3.3V, TA=+25°C)

| Symbol      | Parameter              | Min | Typ | Max | Unit |
|-------------|------------------------|-----|-----|-----|------|
| $t_{cycle}$ | Clock Cycle Time       | 100 | -   | -   | ns   |
| $t_{AS}$    | Address Setup Time     | 15  | -   | -   | ns   |
| $t_{AH}$    | Address Hold Time      | 15  | -   | -   | ns   |
| $t_{CSS}$   | Chip Select Setup Time | 20  | -   | -   | ns   |
| $t_{CSH}$   | Chip Select Hold Time  | 50  | -   | -   | ns   |
| $t_{DW}$    | Data Write Time        | 55  | -   | -   | ns   |
| $t_{DSW}$   | Write Data Setup Time  | 15  | -   | -   | ns   |
| $t_{DHW}$   | Write Data Hold Time   | 15  | -   | -   | ns   |
| $t_{CLKL}$  | Clock Low Time         | 50  | -   | -   | ns   |
| $t_{CLKH}$  | Clock High Time        | 50  | -   | -   | ns   |
| $t_R$       | Rise Time              | -   | -   | 40  | ns   |
| $t_F$       | Fall Time              | -   | -   | 40  | ns   |

Serial interface characteristics (4-wire SPI)



**■ ELECTRO-OPTICAL CHARACTERISTICS (Ta=25°C)**

| Items                |       | Symbol          | Min.    | Typ.  | Max.  | Unit               | Remark                                  |
|----------------------|-------|-----------------|---------|-------|-------|--------------------|---|
| Operating Luminance  |       | L               | 200     | 250*  | -     | cd /m <sup>2</sup> | White                                   |
| Power Consumption    |       | P               | -       | 15    | 20    | mW                 | 30% pixels ON<br>L=250cd/m <sup>2</sup> |
| Frame Frequency      |       | Fr              | -       | 100   | -     | Hz                 | -                                       |
| Color Coordinate     | White | CIE x           | 0.255   | 0.285 | 0.315 | CIE1931            | Darkroom                                |
|                      |       | CIE y           | 0.300   | 0.330 | 0.360 |                    |   |
| Response Time        | Rise  | Tr              | -       | -     | 0.02  | ms                 | -                                       |
|                      | Decay | Td              | -       | -     | 0.02  | ms                 | -                                       |
| Contrast Ratio*      |       | Cr              | 10000:1 | -     | -     | -                  | Darkroom                                |
| Viewing Angle        |       | $\Delta \theta$ | 160     | -     | -     | Degree             | -                                       |
| Operating Life Time* |       | Top             | 10000   | -     | -     | Hours              | L=250cd/m <sup>2</sup>                  |

**Note:**

1. L=250 cd/m<sup>2</sup> is based on V<sub>DD</sub>=3.0V, V<sub>CC</sub>=10.0V, contrast command setting 0X1A;

2. **Contrast ratio** is defined as follows:

$$\text{Contrast ratio} = \frac{\text{Photo - detector output with OLED being "white"}}{\text{Photo - detector output with OLED being "black"}}$$

3. **Life Time** is defined when the Luminance has decayed to less than 50% of the initial Luminance specification. (Odd and even chess board alternately displayed). (The initial value should be closed to the typical value after adjusting.)



**■ INTERFACE PIN CONNECTIONS**

| No | Symbol | Description  |
|----|--------|--|
| 1  | VCC    | Power supply for panel driving voltage. This is also the most positive power voltage supply pin.   |
| 2  | VSS    | Ground pin. It must be connected to external ground.   |
| 3  | CS#    | This pin is the chip select input connecting to the MCU.<br>The chip is enabled for MCU communication only when CS# is pulled LOW (active LOW).            |
| 4  | RES#   | This pin is reset signal input.<br>When the pin is pulled LOW, initialization of the chip is executed.<br>Keep this pin pull HIGH during normal operation. |
| 5  | D/C#   | This pin is Data/Command control pin connecting to the MCU.  |
| 6  | SCLK   | The serial clock input PIN   |
| 7  | SDIN   | The serial data input PIN  |
| 8  | NC     | No connection.   |
| 9  | VCOMH  | COM signal deselected voltage level.<br>Connected to VCC.  |
| 10 | NC     | No connection.   |
| 11 | VDD    | Power supply pin for core logic operation.   |

■ **COMMAND TABLE**

| 1. Fundamental Command Table |              |         |         |         |         |         |         |         |         |                            |   |
|------------------------------|--------------|---------|---------|---------|---------|---------|---------|---------|---------|----------------------------|---|
| D/C#                         | Hex          | D7      | D6      | D5      | D4      | D3      | D2      | D1      | D0      | Command                    | Description   |
| 0<br>0                       | 81<br>A[7:0] | 1<br>A7 | 0<br>A6 | 0<br>A5 | 0<br>A4 | 0<br>A3 | 0<br>A2 | 0<br>A1 | 1<br>A0 | Set Contrast Control       | Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 7Fh)   |
| 0                            | A4/A5        | 1       | 0       | 1       | 0       | 0       | 1       | 0       | X0      | Entire Display ON          | A4h, X0=0b: Resume to RAM content display (RESET) Output follows RAM content.<br>A5h, X0=1b: Entire display ON Output ignores RAM content.  |
| 0                            | A6/A7        | 1       | 0       | 1       | 0       | 0       | 1       | 1       | X0      | Set Normal/Inverse Display | A6h, X[0]=0b: Normal display (RESET).<br>0 in RAM: OFF in display panel<br>1 in RAM: ON in display panel<br>A7h, X[0]=1b: Inverse display<br>0 in RAM: ON in display panel<br>1 in RAM: OFF in display panel  |
| 0                            | AE/AF        | 1       | 0       | 1       | 0       | 1       | 1       | 1       | X0      | Set Display ON/OFF         | AEh, X[0]=0b: Display OFF (sleep mode) (RESET)<br>AFh X[0]=1b: Display ON in normal mode  |
| 0                            | E3           | 1       | 1       | 1       | 0       | 0       | 0       | 1       | 1       | NOP                        | Command for no operation.   |
| 0<br>0                       | FD<br>A[2]   | 1<br>0  | 1<br>0  | 1<br>0  | 1<br>1  | 1<br>0  | 1<br>A2 | 0<br>1  | 1<br>0  | Set Command Lock           | A[2]: MCU protection status.<br>A[2] = 0b, Unlock OLED driver IC MCU interface from entering command (RESET).<br>A[2] = 1b, Lock OLED driver IC MCU interface from entering command.<br><b>Note:</b><br>The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command |

| 2. Scrolling Command Table |                 |              |    |    |    |    |    |    |    |   |  |                 |                 |                  |                 |                   |                 |                   |                 |  |
|----------------------------|-----------------|--------------|----|----|----|----|----|----|----|---|--|-----------------|-----------------|------------------|-----------------|-------------------|-----------------|-------------------|-----------------|--|
| D/C#                       | Hex             | D7           | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command   | Description  |                 |                 |                  |                 |                   |                 |                   |                 |  |
| 0                          | 26/27           | 0            | 0  | 1  | 0  | 0  | 1  | 1  | X0 | Continuous  | 26h, X[0]=0, Right Horizontal Scroll   |                 |                 |                  |                 |                   |                 |                   |                 |  |
| 0                          | A[7:0]          | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | Horizontal Scroll   | 27h, X[0]=1, Left Horizontal Scroll  |                 |                 |                  |                 |                   |                 |                   |                 |  |
| 0                          | B[2:0]          | *            | *  | *  | *  | *  | B2 | B1 | B0 | Setup   | A[7:0] : Dummy byte (Set as 00h)   |                 |                 |                  |                 |                   |                 |                   |                 |  |
| 0                          | C[2:0]          | *            | *  | *  | *  | *  | C2 | C1 | C0 |   | Horizontal scroll by 1 column  |                 |                 |                  |                 |                   |                 |                   |                 |  |
| 0                          | D[2:0]          | *            | *  | *  | *  | *  | D2 | D1 | D0 |   | B[2:0] : Define start page address   |                 |                 |                  |                 |                   |                 |                   |                 |  |
| 0                          | E[7:0]          | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  |   | <table border="1"> <tr> <td>000b – PAGE0</td> <td>011b – PAGE3</td> <td>110b – PAGE6</td> </tr> <tr> <td>001b – PAGE1</td> <td>100b – PAGE4</td> <td>111b – PAGE7</td> </tr> <tr> <td>010b – PAGE2</td> <td>101b – PAGE5</td> <td></td> </tr> </table>                               | 000b – PAGE0    | 011b – PAGE3    | 110b – PAGE6     | 001b – PAGE1    | 100b – PAGE4      | 111b – PAGE7    | 010b – PAGE2      | 101b – PAGE5    |  |
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| 001b – PAGE1               | 100b – PAGE4    | 111b – PAGE7 |    |    |    |    |    |    |    |   |  |                 |                 |                  |                 |                   |                 |                   |                 |  |
| 010b – PAGE2               | 101b – PAGE5    |              |    |    |    |    |    |    |    |   |  |                 |                 |                  |                 |                   |                 |                   |                 |  |
| 0                          | F[7:0]          | F7           | F6 | F5 | F4 | F3 | F2 | F1 | F0 | C[2:0] : Set time interval between each scroll step in terms of frame frequency |  |                 |                 |                  |                 |                   |                 |                   |                 |  |
| 0                          | G[7:0]          | G7           | G6 | G5 | G4 | G3 | G2 | G1 | G0 |   | <table border="1"> <tr> <td>000b – 5 frames</td> <td>100b – 2 frames</td> </tr> <tr> <td>001b – 64 frames</td> <td>101b – 3 frames</td> </tr> <tr> <td>010b – 128 frames</td> <td>110b – 4 frames</td> </tr> <tr> <td>011b – 256 frames</td> <td>111b – 1 frames</td> </tr> </table> | 000b – 5 frames | 100b – 2 frames | 001b – 64 frames | 101b – 3 frames | 010b – 128 frames | 110b – 4 frames | 011b – 256 frames | 111b – 1 frames |  |
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| 001b – 64 frames           | 101b – 3 frames |              |    |    |    |    |    |    |    |   |  |                 |                 |                  |                 |                   |                 |                   |                 |  |
| 010b – 128 frames          | 110b – 4 frames |              |    |    |    |    |    |    |    |   |  |                 |                 |                  |                 |                   |                 |                   |                 |  |
| 011b – 256 frames          | 111b – 1 frames |              |    |    |    |    |    |    |    |   |  |                 |                 |                  |                 |                   |                 |                   |                 |  |
|                            |                 |              |    |    |    |    |    |    |    | D[2:0] : Define end page address  | <table border="1"> <tr> <td>000b – PAGE0</td> <td>011b – PAGE3</td> <td>110b – PAGE6</td> </tr> <tr> <td>001b – PAGE1</td> <td>100b – PAGE4</td> <td>111b – PAGE7</td> </tr> <tr> <td>010b – PAGE2</td> <td>101b – PAGE5</td> <td></td> </tr> </table>                               | 000b – PAGE0    | 011b – PAGE3    | 110b – PAGE6     | 001b – PAGE1    | 100b – PAGE4      | 111b – PAGE7    | 010b – PAGE2      | 101b – PAGE5    |  |
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| 001b – PAGE1               | 100b – PAGE4    | 111b – PAGE7 |    |    |    |    |    |    |    |   |  |                 |                 |                  |                 |                   |                 |                   |                 |  |
| 010b – PAGE2               | 101b – PAGE5    |              |    |    |    |    |    |    |    |   |  |                 |                 |                  |                 |                   |                 |                   |                 |  |
|                            |                 |              |    |    |    |    |    |    |    | E[7:0] : Dummy byte (Set as 00h)  |  |                 |                 |                  |                 |                   |                 |                   |                 |  |
|                            |                 |              |    |    |    |    |    |    |    | F[7:0] : Define the start column (RESET = 00h)                                  |  |                 |                 |                  |                 |                   |                 |                   |                 |  |
|                            |                 |              |    |    |    |    |    |    |    | G[7:0] : Define the end column address (RESET = 7Fh)                            |  |                 |                 |                  |                 |                   |                 |                   |                 |  |
|                            |                 |              |    |    |    |    |    |    |    | <b>Notes:</b>   |  |                 |                 |                  |                 |                   |                 |                   |                 |  |
|                            |                 |              |    |    |    |    |    |    |    | (1) The value of D[2:0] must be larger than or equal to B[2:0]                  |  |                 |                 |                  |                 |                   |                 |                   |                 |  |
|                            |                 |              |    |    |    |    |    |    |    | (2) The value of G[7:0] must be larger than or equal to F[7:0]                  |  |                 |                 |                  |                 |                   |                 |                   |                 |  |

| 2. Scrolling Command Table |                 |              |    |    |    |    |    |    |    |                   |  |                 |                 |                  |                 |                   |                 |                   |                 |  |
|----------------------------|-----------------|--------------|----|----|----|----|----|----|----|-------------------|--|-----------------|-----------------|------------------|-----------------|-------------------|-----------------|-------------------|-----------------|--|
| D/C#                       | Hex             | D7           | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command           | Description  |                 |                 |                  |                 |                   |                 |                   |                 |  |
| 0                          | 29/2A           | 0            | 0  | 1  | 0  | 1  | 0  | X1 | X0 | Continuous        | 29h, X1X0=01b : Vertical and Right Horizontal Scroll   |                 |                 |                  |                 |                   |                 |                   |                 |  |
| 0                          | A[0]            | *            | *  | *  | *  | *  | *  | *  | A0 | Vertical and      | 2Ah, X1X0=10b : Vertical and Left Horizontal Scroll  |                 |                 |                  |                 |                   |                 |                   |                 |  |
| 0                          | B[2:0]          | *            | *  | *  | *  | *  | B2 | B1 | B0 | Horizontal Scroll | A[0] : Set number of column scroll offset  |                 |                 |                  |                 |                   |                 |                   |                 |  |
| 0                          | C[2:0]          | *            | *  | *  | *  | *  | C2 | C1 | C0 | Setup             | 0b No horizontal scroll  |                 |                 |                  |                 |                   |                 |                   |                 |  |
| 0                          | D[2:0]          | *            | *  | *  | *  | *  | D2 | D1 | D0 |                   | 1b Horizontal scroll by 1 column   |                 |                 |                  |                 |                   |                 |                   |                 |  |
| 0                          | E[5:0]          | *            | *  | E5 | E4 | E3 | E2 | E1 | E0 |                   | B[2:0] : Define start page address   |                 |                 |                  |                 |                   |                 |                   |                 |  |
| 0                          | F[7:0]          | F7           | F6 | F5 | F4 | F3 | F2 | F1 | F0 |                   | <table border="1"> <tr> <td>000b – PAGE0</td> <td>011b – PAGE3</td> <td>110b – PAGE6</td> </tr> <tr> <td>001b – PAGE1</td> <td>100b – PAGE4</td> <td>111b – PAGE7</td> </tr> <tr> <td>010b – PAGE2</td> <td>101b – PAGE5</td> <td></td> </tr> </table>                               | 000b – PAGE0    | 011b – PAGE3    | 110b – PAGE6     | 001b – PAGE1    | 100b – PAGE4      | 111b – PAGE7    | 010b – PAGE2      | 101b – PAGE5    |  |
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| 001b – PAGE1               | 100b – PAGE4    | 111b – PAGE7 |    |    |    |    |    |    |    |                   |  |                 |                 |                  |                 |                   |                 |                   |                 |  |
| 010b – PAGE2               | 101b – PAGE5    |              |    |    |    |    |    |    |    |                   |  |                 |                 |                  |                 |                   |                 |                   |                 |  |
| 0                          | G[7:0]          | G7           | G6 | G5 | G4 | G3 | G2 | G1 | G0 |                   | C[2:0] : Set time interval between each scroll step in terms of frame frequency  |                 |                 |                  |                 |                   |                 |                   |                 |  |
|                            |                 |              |    |    |    |    |    |    |    |                   | <table border="1"> <tr> <td>000b – 5 frames</td> <td>100b – 2 frames</td> </tr> <tr> <td>001b – 64 frames</td> <td>101b – 3 frames</td> </tr> <tr> <td>010b – 128 frames</td> <td>110b – 4 frames</td> </tr> <tr> <td>011b – 256 frames</td> <td>111b – 1 frames</td> </tr> </table> | 000b – 5 frames | 100b – 2 frames | 001b – 64 frames | 101b – 3 frames | 010b – 128 frames | 110b – 4 frames | 011b – 256 frames | 111b – 1 frames |  |
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| 010b – 128 frames          | 110b – 4 frames |              |    |    |    |    |    |    |    |                   |  |                 |                 |                  |                 |                   |                 |                   |                 |  |
| 011b – 256 frames          | 111b – 1 frames |              |    |    |    |    |    |    |    |                   |  |                 |                 |                  |                 |                   |                 |                   |                 |  |
|                            |                 |              |    |    |    |    |    |    |    |                   | D[2:0] : Define end page address   |                 |                 |                  |                 |                   |                 |                   |                 |  |
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| 010b – PAGE2               | 101b – PAGE5    |              |    |    |    |    |    |    |    |                   |  |                 |                 |                  |                 |                   |                 |                   |                 |  |
|                            |                 |              |    |    |    |    |    |    |    |                   | E[5:0] : Vertical scrolling offset<br>e.g. E[5:0]= 01h refer to offset =1 row<br>E[5:0] =3Fh refer to offset =63 rows  |                 |                 |                  |                 |                   |                 |                   |                 |  |
|                            |                 |              |    |    |    |    |    |    |    |                   | F[7:0] : Define the start column (RESET = 00h)   |                 |                 |                  |                 |                   |                 |                   |                 |  |
|                            |                 |              |    |    |    |    |    |    |    |                   | G[7:0] : Define the end column address (RESET = 7Fh)   |                 |                 |                  |                 |                   |                 |                   |                 |  |
|                            |                 |              |    |    |    |    |    |    |    |                   | <b>Note:</b><br>(1) The value of D[2:0] must be larger than or equal to B[2:0]<br>(2) The value of G[7:0] must be larger than or equal to F[7:0]   |                 |                 |                  |                 |                   |                 |                   |                 |  |
| 0                          | 2E              | 0            | 0  | 1  | 0  | 1  | 1  | 1  | 0  | Deactivate scroll | Stop scrolling that is configured by command 26h/27h/29h/2Ah.<br><b>Note:</b><br>After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewrite  |                 |                 |                  |                 |                   |                 |                   |                 |  |

| 2. Scrolling Command Table           |   |  |  |  |  |  |  |  |   |                          |   |              |              |              |              |              |              |              |              |  |              |              |              |              |              |              |              |              |  |
|--------------------------------------|---|--|--|--|--|--|--|--|---|--------------------------|---|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--|
| D/C#                                 | Hex   | D7                                     | D6                                     | D5                                     | D4                                     | D3                                     | D2                                       | D1                                       | D0  | Command                  | Description   |              |              |              |              |              |              |              |              |  |              |              |              |              |              |              |              |              |  |
| 0                                    | 2F  | 0                                      | 0                                      | 1                                      | 0                                      | 1                                      | 1  | 1  | 1   | Activate scroll          | <p>Start scrolling that is configured by the scrolling setup commands :26h/27h/29h/2Ah with the following valid sequences:</p> <p>Valid command sequence 1: 26h; 2Fh.<br/>                     Valid command sequence 2: 27h; 2Fh.<br/>                     Valid command sequence 3: 29h; 2Fh.<br/>                     Valid command sequence 4: 2Ah; 2Fh.</p> <p>For example, if “26h; 2Ah; 2Fh.” commands are issued, the setting in the last scrolling setup command, i.e. 2Ah in this case, will be executed. In other words, setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.</p>  |              |              |              |              |              |              |              |              |  |              |              |              |              |              |              |              |              |  |
| 0<br>0<br>0                          | A3<br>A[5:0]<br>B[6:0]  | 1<br>*<br>*                            | 0<br>*<br>B6                           | 1<br>A5<br>B5                          | 0<br>A4<br>B4                          | 0<br>A3<br>B3                          | 0<br>A2<br>B2                            | 1<br>A1<br>B1                            | 1<br>A0<br>B0                             | Set Vertical Scroll Area | <p>A[5:0] : Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0).[RESET = 0]</p> <p>B[6:0] : Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 64]</p> <p><b>Note:</b></p> <p>(1) A[5:0]+B[6:0] &lt;= MUX ratio<br/>                     (2) B[6:0] &lt;= MUX ratio<br/>                     (3a) Vertical scrolling offset (E[5:0] in 29h/2Ah) &lt; B[6:0]<br/>                     (3b) Set Display Start Line (X5X4X3X2X1X0 of 40h~7Fh) &lt; B[6:0]<br/>                     (4) The last row of the scroll area shifts to the first row of the scroll area.<br/>                     (5) For 64d MUX display<br/>                     A[5:0] = 0, B[6:0]=64 : whole area scrolls<br/>                     A[5:0]=0, B[6:0] &lt; 64 : top area scrolls<br/>                     A[5:0] + B[6:0] &lt; 64 : central area scrolls<br/>                     A[5:0] + B[6:0] = 64 : bottom area scrolls<br/>                     (6) When vertical scrolling is enabled by command 29h / 2Ah, the vertical scroll area is defined by this command</p>  |              |              |              |              |              |              |              |              |  |              |              |              |              |              |              |              |              |  |
| 0<br>0<br>0<br>0<br>0<br>0<br>0<br>0 | 2C/2D<br>A[7:0]<br>B[2:0]<br>C[7:0]<br>D[2:0]<br>E[7:0]<br>F[7:0]<br>G[7:0] | 0<br>0<br>*<br>0<br>*<br>0<br>F7<br>G7 | 0<br>0<br>*<br>0<br>*<br>0<br>F6<br>G6 | 1<br>0<br>*<br>0<br>*<br>0<br>F5<br>G5 | 0<br>0<br>*<br>0<br>*<br>0<br>F4<br>G4 | 1<br>0<br>*<br>0<br>*<br>0<br>F3<br>G3 | 1<br>0<br>B2<br>0<br>D2<br>0<br>F2<br>G2 | 0<br>0<br>B1<br>0<br>D1<br>0<br>F1<br>G1 | X0<br>0<br>B0<br>1<br>D0<br>0<br>F0<br>G0 | Content Scroll Setup     | <p>2Ch, X[0]=0, Right Horizontal Scroll by one column<br/>                     2Dh, X[0]=1, Left Horizontal Scroll by one column</p> <p>A[7:0] : Dummy byte (Set as 00h) Horizontal scroll by 1 column<br/>                     B[2:0] : Define start page address</p> <table border="1"> <tr> <td>000b – PAGE0</td> <td>011b – PAGE3</td> <td>110b – PAGE6</td> </tr> <tr> <td>001b – PAGE1</td> <td>100b – PAGE4</td> <td>111b – PAGE7</td> </tr> <tr> <td>010b – PAGE2</td> <td>101b – PAGE5</td> <td></td> </tr> </table> <p>C[7:0] : Dummy byte (Set as 01h)<br/>                     D[2:0] : Define end page address</p> <table border="1"> <tr> <td>000b – PAGE0</td> <td>011b – PAGE3</td> <td>110b – PAGE6</td> </tr> <tr> <td>001b – PAGE1</td> <td>100b – PAGE4</td> <td>111b – PAGE7</td> </tr> <tr> <td>010b – PAGE2</td> <td>101b – PAGE5</td> <td></td> </tr> </table> <p>E[7:0] : Dummy byte (Set as 00h)<br/>                     F[7:0] : Define the start column (RESET = 00h)<br/>                     G[7:0] : Define the end column address (RESET 7Fh)</p> <p><b>Note:</b></p> <p>(1) The value of D[2:0] must be larger than or equal to B[2:0]<br/>                     (2) The value of G[7:0] must be larger than F[7:0]<br/>                     (3) A delay time of 2 <i>FrameFreq</i> must be set if sending the command of 2Ch / 2Dh consecutively.</p> | 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 | 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 | 010b – PAGE2 | 101b – PAGE5 |  | 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 | 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 | 010b – PAGE2 | 101b – PAGE5 |  |
| 000b – PAGE0                         | 011b – PAGE3  | 110b – PAGE6                           |  |  |  |  |  |  |   |                          |   |              |              |              |              |              |              |              |              |  |              |              |              |              |              |              |              |              |  |
| 001b – PAGE1                         | 100b – PAGE4  | 111b – PAGE7                           |  |  |  |  |  |  |   |                          |   |              |              |              |              |              |              |              |              |  |              |              |              |              |              |              |              |              |  |
| 010b – PAGE2                         | 101b – PAGE5  |  |  |  |  |  |  |  |   |                          |   |              |              |              |              |              |              |              |              |  |              |              |              |              |              |              |              |              |  |
| 000b – PAGE0                         | 011b – PAGE3  | 110b – PAGE6                           |  |  |  |  |  |  |   |                          |   |              |              |              |              |              |              |              |              |  |              |              |              |              |              |              |              |              |  |
| 001b – PAGE1                         | 100b – PAGE4  | 111b – PAGE7                           |  |  |  |  |  |  |   |                          |   |              |              |              |              |              |              |              |              |  |              |              |              |              |              |              |              |              |  |
| 010b – PAGE2                         | 101b – PAGE5  |  |  |  |  |  |  |  |   |                          |   |              |              |              |              |              |              |              |              |  |              |              |              |              |              |              |              |              |  |

| 3. Addressing Setting Command Table |                        |               |               |               |               |               |               |               |               |  |   |
|-------------------------------------|------------------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|--|---|
| D/C#                                | Hex                    | D7            | D6            | D5            | D4            | D3            | D2            | D1            | D0            | Command  | Description   |
| 0                                   | 00~0F                  | 0             | 0             | 0             | 0             | X3            | X2            | X1            | X0            | Set Lower Column Start Address for Page Addressing Mode  | Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET.<br><br><b>Note:</b><br>This command is only for page addressing mode         |
| 0                                   | 10~1F                  | 0             | 0             | 0             | 1             | X3            | X2            | X1            | X0            | Set Higher Column Start Address for Page Addressing Mode | Set the higher nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET.<br><br><b>Note:</b><br>This command is only for page addressing mode        |
| 0<br>0                              | 20<br>A[1:0]           | 0<br>*        | 0<br>*        | 1<br>*        | 0<br>*        | 0<br>*        | 0<br>*        | 0<br>A1       | 0<br>A0       | Set Memory Addressing Mode                               | A[1:0] = 00b, Horizontal Addressing Mode<br>A[1:0] = 01b, Vertical Addressing Mode<br>A[1:0] = 10b, Page Addressing Mode (RESET)<br>A[1:0] = 11b, Invalid   |
| 0<br>0<br>0                         | 21<br>A[7:0]<br>B[7:0] | 0<br>A7<br>B7 | 0<br>A6<br>B6 | 1<br>A5<br>B5 | 0<br>A4<br>B4 | 0<br>A3<br>B3 | 0<br>A2<br>B2 | 0<br>A1<br>B1 | 1<br>A0<br>B0 | Set Column Address                                       | Setup column start and end address<br>A[7:0] : Column start address, range : 0-127d,<br>(RESET=0d)<br>B[7:0] : Column end address, range : 0-127d,<br>(RESET =127d)<br><br><b>Note:</b><br>This command is only for horizontal or vertical addressing mode. |
| 0<br>0<br>0                         | 22<br>A[2:0]<br>B[2:0] | 0<br>*<br>*   | 0<br>*<br>*   | 1<br>*<br>*   | 0<br>*<br>*   | 0<br>*<br>*   | 0<br>A2<br>B2 | 1<br>A1<br>B1 | 0<br>A0<br>B0 | Set Page Address   | Setup page start and end address<br>A[2:0] : Page start Address, range : 0-7d,<br>(RESET = 0d)<br>B[2:0] : Page end Address, range : 0-7d,<br>(RESET = 7d)<br><br><b>Note:</b><br>This command is only for horizontal or vertical addressing mode.          |
| 0                                   | B0~B7                  | 1             | 0             | 1             | 1             | 0             | X2            | X1            | X0            | Set Page Start Address for Page Addressing Mode          | Set GDDRAM Page Start Address (PAGE0~PAGE7) for Page Addressing Mode using X[2:0].<br><br><b>Note :</b><br>This command is only for page addressing mode  |

| 4. Hardware Configuration (Panel resolution & layout related) Command Table |              |        |        |         |         |         |         |         |         |                                     |  |
|---|--------------|--------|--------|---------|---------|---------|---------|---------|---------|-------------------------------------|--|
| D/C#  | Hex          | D7     | D6     | D5      | D4      | D3      | D2      | D1      | D0      | Command                             | Description  |
| 0   | 40~7F        | 0      | 1      | X5      | X4      | X3      | X2      | X1      | X0      | Set Display Start Line              | Set display RAM display start line register from 0-63 using X5X3X2X1X0.<br>Display start line register is reset to 000000b during RESET.   |
| 0   | A0/A1        | 1      | 0      | 1       | 0       | 0       | 0       | 0       | X0      | Set Segment Re-map                  | A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET)<br>A1h, X[0]=1b: column address 127 is mapped to SEG0   |
| 0<br>0  | A8<br>A[5:0] | 1<br>* | 0<br>* | 1<br>A5 | 0<br>A4 | 1<br>A3 | 0<br>A2 | 0<br>A1 | 0<br>A0 | Set Multiplex Ratio                 | Set MUX ratio to N+1 MUX<br>N=A[5:0] : from 16MUX to 64MUX,<br>RESET= 111111b (i.e. 63d, 64MUX)<br>A[5:0] from 0 to 14 are invalid entry.  |
| 0   | C0/C8        | 1      | 1      | 0       | 0       | X3      | 0       | 0       | 0       | Set COM Output Scan Direction       | C0h, X[3]=0b: normal mode (RESET)<br>Scan from COM0 to COM[N-1]<br>C8h, X[3]=1b: remapped mode.<br>Scan from COM[N-1] to COM0<br><br>Where N is the Multiplex ratio.                     |
| 0<br>0  | D3<br>A[5:0] | 1<br>* | 1<br>* | 0<br>A5 | 1<br>A4 | 0<br>A3 | 0<br>A2 | 1<br>A1 | 1<br>A0 | Set Display Offset                  | Set vertical shift by COM from 0d~63d<br>The value is reset to 00h after RESET.  |
| 0<br>0  | DA<br>A[5:4] | 1<br>0 | 1<br>0 | 0<br>A5 | 1<br>A4 | 1<br>0  | 0<br>0  | 1<br>1  | 0<br>0  | Set COM Pins Hardware Configuration | A[4]=0b, Sequential COM pin configuration<br>A[4]=1b (RESET), Alternative COM pin configuration<br>A[5]=0b (RESET), Disable COM Left/Right remap<br>A[5]=1b, Enable COM Left/Right remap |
| 0<br>0  | DC<br>A[1:0] | 1<br>0 | 1<br>0 | 0<br>0  | 1<br>0  | 1<br>0  | 1<br>0  | 0<br>A1 | 0<br>A0 | Set GPIO                            | A[1:0] GPIO : 00 pin HiZ, Input disabled<br>01 pin HiZ, Input enabled<br>10 pin output LOW [RESET]<br>11 pin output HIGH   |

| 5. Timing & Driving Scheme Setting Command Table |              |                      |         |         |         |         |         |         |         |   |  |        |          |                      |       |     |              |       |     |                      |       |     |              |
|--|--------------|----------------------|---------|---------|---------|---------|---------|---------|---------|---|--|--------|----------|----------------------|-------|-----|--------------|-------|-----|----------------------|-------|-----|--------------|
| D/C#   | Hex          | D7                   | D6      | D5      | D4      | D3      | D2      | D1      | D0      | Command   | Description  |        |          |                      |       |     |              |       |     |                      |       |     |              |
| 0<br>0   | D5<br>A[7:0] | 1<br>A7              | 1<br>A6 | 0<br>A5 | 1<br>A4 | 0<br>A3 | 1<br>A2 | 0<br>A1 | 1<br>A0 | Set Display Clock Divide Ratio/Oscillator Frequency | A[3:0] : Define the divide ratio (D) of the display clocks (DCLK):<br>Divide ratio= A[3:0] + 1, RESET is 0000b<br>(divide ratio = 1)<br>A[7:4] : Set the Oscillator Frequency, FOSC.<br>Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 0111b<br><br>Range:0000b~1111b<br>Frequency increases as setting value increases. |        |          |                      |       |     |              |       |     |                      |       |     |              |
| 0<br>0   | D9<br>A[7:0] | 1<br>A7              | 1<br>A6 | 0<br>A5 | 1<br>A4 | 1<br>A3 | 0<br>A2 | 0<br>A1 | 1<br>A0 | Set Pre-charge Period                               | A[3:0] : Phase 1 period of up to 15 DCLK<br>Clock 0 is invalid entry<br>(RESET=2h)<br>A[7:4] : Phase 2 period of up to 15 DCLK<br>Clock 0 is invalid entry<br>(RESET=2h )  |        |          |                      |       |     |              |       |     |                      |       |     |              |
| 0<br>0   | DB<br>A[5:2] | 1<br>0               | 1<br>0  | 0<br>A5 | 1<br>A4 | 1<br>A3 | 0<br>A2 | 1<br>0  | 1<br>0  | Set VCOMH Deselect Level                            | <table border="1"> <thead> <tr> <th>A[5:2]</th> <th>Hex code</th> <th>VCOMH deselect level</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>00h</td> <td>~ 0.64 x VCC</td> </tr> <tr> <td>1101b</td> <td>34h</td> <td>~ 0.78 x VCC (RESET)</td> </tr> <tr> <td>1111b</td> <td>3Ch</td> <td>~ 0.84 x VCC</td> </tr> </tbody> </table>                    | A[5:2] | Hex code | VCOMH deselect level | 0000b | 00h | ~ 0.64 x VCC | 1101b | 34h | ~ 0.78 x VCC (RESET) | 1111b | 3Ch | ~ 0.84 x VCC |
| A[5:2]   | Hex code     | VCOMH deselect level |         |         |         |         |         |         |         |   |  |        |          |                      |       |     |              |       |     |                      |       |     |              |
| 0000b  | 00h          | ~ 0.64 x VCC         |         |         |         |         |         |         |         |   |  |        |          |                      |       |     |              |       |     |                      |       |     |              |
| 1101b  | 34h          | ~ 0.78 x VCC (RESET) |         |         |         |         |         |         |         |   |  |        |          |                      |       |     |              |       |     |                      |       |     |              |
| 1111b  | 3Ch          | ~ 0.84 x VCC         |         |         |         |         |         |         |         |   |  |        |          |                      |       |     |              |       |     |                      |       |     |              |

**Note:** “\*” stands for “Don’t care”.



**■ INITIALIZATION CODE**

```
void InitOLED_MASTER_SSD1309(void)
{
    MainOLED_WCom(0xFD);           //Set Command Lock
    MainOLED_WCom(0x12);
    MainOLED_WCom(0xAE);           //Display OFF(sleep mode)(RESET)
    MainOLED_WCom(0x81);           //Contrast Control(00H-FFH)
    MainOLED_WCom(CONTRAST);
    MainOLED_WCom(0xA4);           //Entire Display ON
    MainOLED_WCom(0xA6);           //Set Normal Display

    MainOLED_WCom(0x8D);           //Set DC-DC (charge Pump)
    MainOLED_WCom(0x14);           //Enable charge Pump
    MainOLED_WCom(0xD8);           //Set low power display mode
    MainOLED_WCom(0x05);           //Lower power display mode

    MainOLED_WCom(0XAD);
    MainOLED_WCom(0X48);

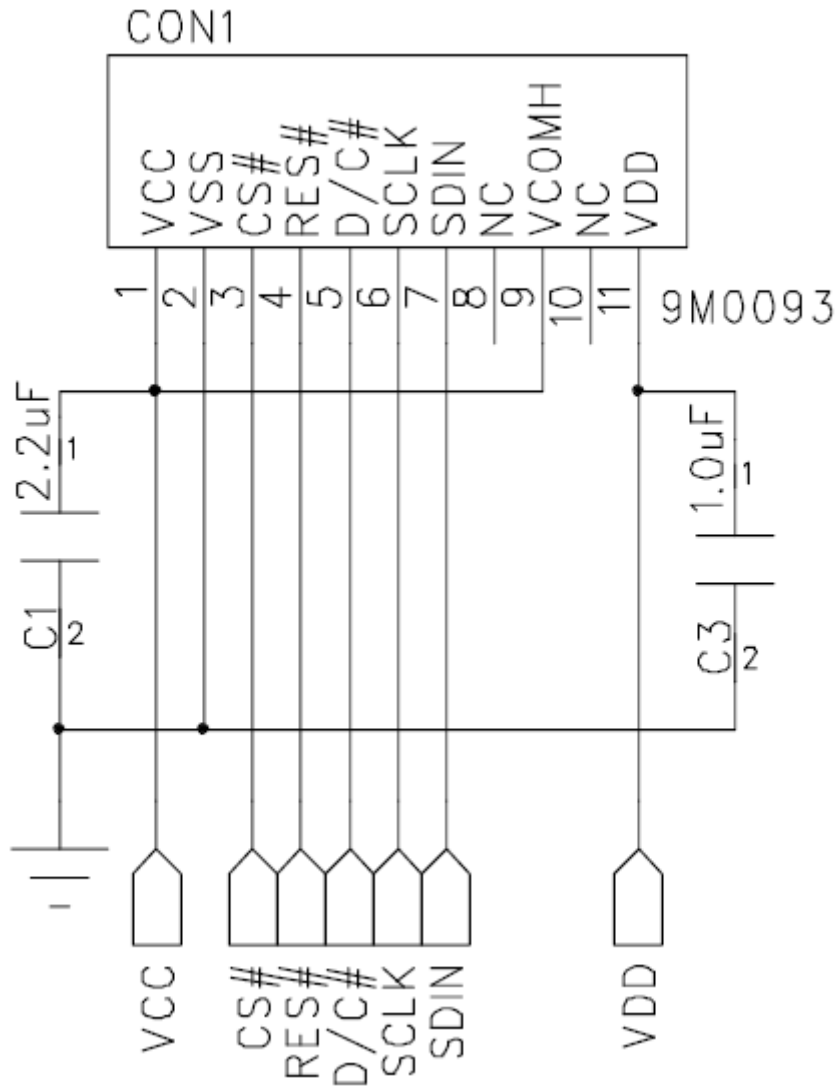
    MainOLED_WCom(0x40);           //Set Display Start Line (040H-07FH)
    MainOLED_WCom(0xA1);           //Set Segment Re-Map
    MainOLED_WCom(0xA8);           //Set Multiplex Ratio 64
    MainOLED_WCom(0x1F);
    MainOLED_WCom(0xC8);           //Com Scan Com1-Com64

    MainOLED_WCom(0xD3);           //Set Display Offset(00H-3FH)
    MainOLED_WCom(0x00);
    MainOLED_WCom(0xDA);           //Com Pin Configuration
    MainOLED_WCom(0x12);
    MainOLED_WCom(0xD5);           //Set Frame Frequency
    MainOLED_WCom(0x80);
    MainOLED_WCom(0xD9);           //Set Pre-Charge Period
    MainOLED_WCom(0xF1);
    MainOLED_WCom(0xDB);           //Set VCOM Deselect Level
    MainOLED_WCom(0x20);

    MainOLED_WCom(0xAF);           //Display ON
}
}
```

■ SCHEMATIC EXAMPLE

◆ Serial Interface Application Circuit:



**■ RELIABILITY TESTS**

| Item  |  | Condition   | Criterion   |
|---|--|---|---|
| High Temperature Storage<br>(HTS)                   |  | 80±2℃, 200 hours  | 1. After testing, the function test is ok.<br>2. After testing, no addition to the defect.<br>3. After testing, the change of luminance should be within +/- 50% of initial value.<br>4. After testing, the change for the mono and area color must be within (+/-0.02, +/- 0.02) and for the full color it must be within (+/-0.04, +/-0.04) of initial value based on 1931 CIE coordinates.<br>5. After testing, the change of total current consumption should be within +/- 50% of initial value. |
| High Temperature Operating<br>(HTO)                 |  | 70±2℃, 96 hours   |   |
| Low Temperature Storage<br>(LTS)                    |  | -30±2℃, 200 hours   |   |
| Low Temperature Operating<br>(LTO)                  |  | -20±2℃, 96 hours  |   |
| High Temperature / High Humidity Storage<br>(HTHHS) |  | 50±3℃, 90%±3%RH, 120 hours  |   |
| Thermal Shock (Non-operation)<br>(TS)               |  | -20±2℃ ~ 25℃ ~ 70±2℃<br>(30min) (5min) (30min)<br>10cycles  |   |
| Vibration<br>(Packing)                              | 10~55~10Hz, amplitude 1.5mm, 1 hour for each direction x, y, z | 1. One box for each test.<br>2. No addition to the cosmetic and the electrical defects.   |   |
| Drop<br>(Packing)                                   | Height : 1 m, each time for 6 sides, 3 edges, 1 angle          |   |   |
| ESD<br>(finished product housing)                   | ±4kV (R: 330Ω C: 150pF, 10times, air discharge)                | 1. After testing, cosmetic and electrical defects should not happen.<br>2. In case of malfunction or defect caused by ESD damage, it would be judged as a good part if it would be recovered to normal state after resetting. |   |

Note: 1) For each reliability test, the sample quantity is 3, and only for one test item.

2) The HTHHS test is requested the Pure Water(Resistance>10MΩ).

3) The test should be done after 2 hours of recovery time in normal environment.

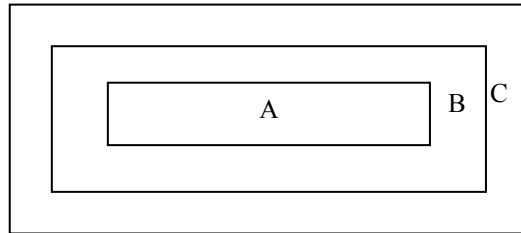
**■ OUTGOING QUALITY CONTROL SPECIFICATION**

**◆ Standard**

According to GB/T2828.1-2003/ISO 2859-1: 1999 and ANSI/ASQC Z1.4-1993, General Inspection Level II.

**◆ Definition**

- 1 Major defect : The defect that greatly affect the usability of product.
- 2 Minor defect : The other defects, such as cosmetic defects, etc.
- 3 Definition of inspection zone:



Zone A: Active Area

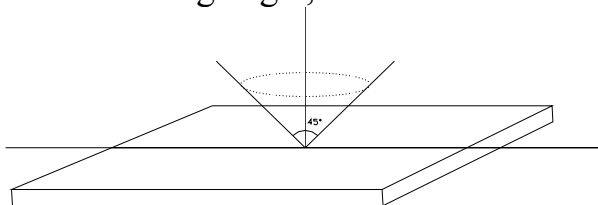
Zone B: Viewing Area except Zone A

Zone C: Outside Viewing Area

Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble of quality and assembly to customer`s product.

**◆ Inspection Methods**

- 1 The general inspection : under 20W x 2 or 40W fluorescent light, about 30cm viewing distance, within 45° viewing angle, under 25±5°C.



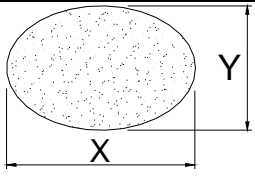
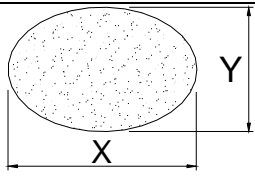
- 2 The luminance and color coordinate inspection : By PR705 or BM-7 or the equal equipments, in the dark room, under 25±5°C.

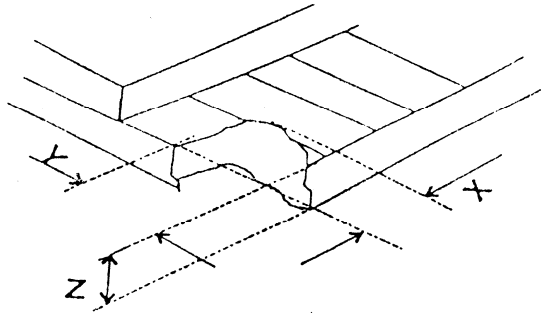
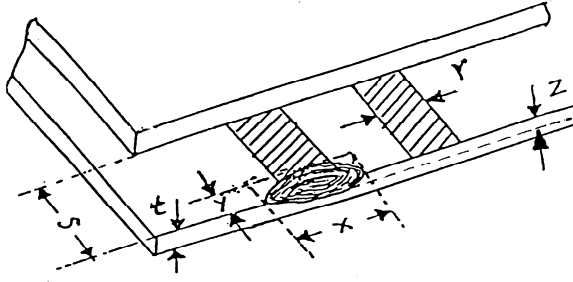
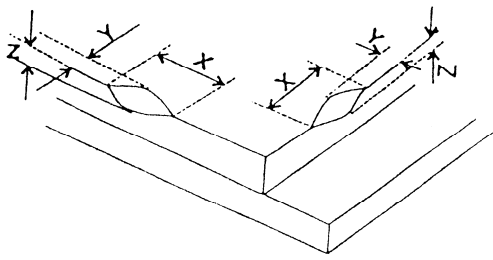
**◆ Inspection Criteria**

- 1 Major defect : AQL= 0.65

| Item              | Criterion  |
|-------------------|--|
| Function Defect   | 1. No display or abnormal display is not accepted        |
|                   | 2. Open or short is not accepted.                        |
|                   | 3. Power consumption exceeding the spec is not accepted. |
| Outline Dimension | Outline dimension exceeding the spec is not accepted.    |
| Glass Crack       | Glass crack tends to enlarge is not accepted.            |

2 Minor Defect : AQL= 1.5

| Item  | Criterion  |                      |                         |         |         |
|---|--|----------------------|-------------------------|---------|---------|
| Spot Defect<br>(dimming and lighting spot)  | Size (mm)  |                      | Accepted Qty            |         |         |
|   |   |                      | Area A + Area B         | Area C  |         |
|   |  |                      | $\Phi \leq 0.07$        | Ignored |         |
|   |  |                      | $0.07 < \Phi \leq 0.10$ | 3       | Ignored |
|   |  |                      | $0.10 < \Phi \leq 0.15$ | 1       |         |
|   |  | $0.15 < \Phi$        | 0                       |         |         |
| Note : $\Phi = (x + y) / 2$   |  |                      |                         |         |         |
| Line Defect<br>(dimming and lighting line)  | L ( Length ) : mm  | W ( Width ) : mm     | Area A + Area B         | Area C  |         |
|   | /  | $W \leq 0.02$        | Ignored                 |         |         |
|   | $L \leq 3.0$   | $0.02 < W \leq 0.03$ | 2                       | Ignored |         |
|   | $L \leq 2.0$   | $0.03 < W \leq 0.05$ | 1                       |         |         |
|   | /  | $0.05 < W$           | As spot defect          |         |         |
| Remarks: The total of spot defect and line defect shall not exceed 4 pcs. The distance between two lines defects must exceed 1 mm |  |                      |                         |         |         |
| Polarizer Stain   | Stain which can be wiped off lightly with a soft cloth or similar cleaning is accepted, otherwise, according to the Spot Defect and the Line Defect. |                      |                         |         |         |
| Polarizer Scratch   | 1. If scratch can be seen during operation, according to the criterions of the Spot Defect and the Line Defect.                                      |                      |                         |         |         |
|   | 2. If scratch can be seen only under non-operation or some special angle, the criterion is as below :  |                      |                         |         |         |
|   | L ( Length ) : mm  | W ( Width ) : mm     | Area A + Area B         | Area C  |         |
|   | /  | $W \leq 0.02$        | Ignore                  |         |         |
|   | $3.0 < L \leq 5.0$   | $0.02 < W \leq 0.04$ | 2                       | Ignore  |         |
|   | $L \leq 3.0$   | $0.04 < W \leq 0.06$ | 1                       |         |         |
| /   | $0.06 < W$   | 0                    |                         |         |         |
| Polarizer Air Bubble  | Size   |                      | Area A + Area B         | Area C  |         |
|   |   |                      | $\Phi \leq 0.20$        |         |         |
|   |  |                      | Ignored                 |         |         |
|   |  |                      | $0.20 < \Phi \leq 0.30$ | 2       |         |
|   |  |                      | $0.30 < \Phi \leq 0.50$ | 1       |         |
|   |  | $0.50 < \Phi$        | 0                       | Ignored |         |

|   |  |              |            |                           |            |          |          |
|---|--|--------------|------------|---------------------------|------------|----------|----------|
| Glass Defect<br>(Glass Chipped)   | <p>1. On the corner</p>  <p>(mm)</p> <table border="1" data-bbox="1061 302 1423 470"> <tr> <td>x</td> <td><math>\leq 1.5</math></td> </tr> <tr> <td>y</td> <td><math>\leq 1.5</math></td> </tr> <tr> <td>z</td> <td><math>\leq t</math></td> </tr> </table> | x            | $\leq 1.5$ | y                         | $\leq 1.5$ | z        | $\leq t$ |
|   | x  | $\leq 1.5$   |            |                           |            |          |          |
|   | y  | $\leq 1.5$   |            |                           |            |          |          |
| z   | $\leq t$   |              |            |                           |            |          |          |
| <p>2. On the bonding edge</p>  <p>(mm)</p> <table border="1" data-bbox="1061 761 1423 929"> <tr> <td>x</td> <td><math>\leq a / 4</math></td> </tr> <tr> <td>y</td> <td><math>\leq s / 3 \ \&amp;\leq 0.7</math></td> </tr> <tr> <td>z</td> <td><math>\leq t</math></td> </tr> </table> | x  | $\leq a / 4$ | y          | $\leq s / 3 \ \&\leq 0.7$ | z          | $\leq t$ |          |
| x   | $\leq a / 4$   |              |            |                           |            |          |          |
| y   | $\leq s / 3 \ \&\leq 0.7$  |              |            |                           |            |          |          |
| z   | $\leq t$   |              |            |                           |            |          |          |
| <p>3. On the other edges</p>  <p>(mm)</p> <table border="1" data-bbox="1061 1187 1423 1355"> <tr> <td>x</td> <td><math>\leq a / 8</math></td> </tr> <tr> <td>y</td> <td><math>\leq 0.7</math></td> </tr> <tr> <td>z</td> <td><math>\leq t</math></td> </tr> </table>                 | x  | $\leq a / 8$ | y          | $\leq 0.7$                | z          | $\leq t$ |          |
| x   | $\leq a / 8$   |              |            |                           |            |          |          |
| y   | $\leq 0.7$   |              |            |                           |            |          |          |
| z   | $\leq t$   |              |            |                           |            |          |          |
| <p>Note: t: glass thickness ; s: pad width ; a: the length of the edge</p>  |  |              |            |                           |            |          |          |
| TCP Defect  | Crack, deep fold and deep pressure mark on the TCP are not accepted  |              |            |                           |            |          |          |
| Pixel Size  | The tolerance of display pixel dimension should be within $\pm 20\%$ of the spec   |              |            |                           |            |          |          |
| Luminance   | Refer to the spec or the reference sample  |              |            |                           |            |          |          |
| Color   | Refer to the spec or the reference sample  |              |            |                           |            |          |          |

**■ CAUTIONS IN USING OLED MODULE****◆ Precautions For Handling OLED Module:**

1. OLED module consists of glass and polarizer. Pay attention to the following items when handling:
  - i. Avoid drop from high, avoid excessive impact and pressure.
  - ii. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead.
  - iii. If the surface becomes dirty, breathe on the surface and gently wipe it off with a soft dry cloth. If it is terrible dirty, moisten the soft cloth with Isopropyl alcohol or Ethyl alcohol. Other solvents may damage the polarizer. Especially water, Ketone and Aromatic solvents.
  - iv. Wipe off saliva or water drops immediately, contact the polarizer with water over a long period of time may cause deformation.
  - v. Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peeling-off may occur with high temperature and high humidity.
  - vi. Condensation on the surface and the terminals due to cold or anything will damage, stain or dirty the polarizer, so make it clean as the way of iii.
2. Do not attempt to disassemble or process the OLED Module.
3. Make sure the TCP or the FPC of the Module is free of twisting, warping and distortion, do not pull or bend them forcefully, especially the soldering pins. On the other side, the SLIT part of the TCP is made to bend in the necessary case.
4. When assembling the module into other equipment, give the glass enough space to avoid excessive pressure on the glass, especially the glass cover which is much more fragile.
5. Be sure to keep the air pressure under 120 kPa, otherwise the glass cover is to be cracked.
6. Be careful to prevent damage by static electricity:
  - i. Be sure to ground the body when handling the OLED Modules.
  - ii. All machines and tools required for assembling, such as soldering irons, must be properly grounded.
  - iii. Do not assemble and do no other work under dry conditions to reduce the amount of static electricity generated. A relative humidity of 50%-60% is recommended.
  - iv. Peel off the protective film slowly to avoid the amount of static electricity generated.
  - v. Avoid to touch the circuit, the soldering pins and the IC on the Module by the body.
  - vi. Be sure to use anti-static package.
7. Contamination on terminals can cause an electrochemical reaction and corrode the terminal circuit, so make it clean anytime.
8. All terminals should be open, do not attach any conductor or semiconductor on the terminals.
9. When the logic circuit power is off, do not apply the input signals.
10. Power on sequence:  $V_{DD} \rightarrow V_{CC}$ , and power off sequence:  $V_{CC} \rightarrow V_{DD}$ .
11. Be sure to keep temperature, humidity and voltage within the ranges of the spec, otherwise shorten Module's life time, even make it damaged.
12. Be sure to drive the OLED Module following the Specification and datasheet of IC controller, otherwise something wrong may be seen.



13. When displaying images, keep them rolling, and avoid one fixed image displaying more than 30 seconds, otherwise the residue image is to be seen. This is the speciality of OLED.

#### ◆ **Precautions For Soldering OLED Module:**

1. Soldering temperature :  $260^{\circ}\text{C} \pm 10^{\circ}\text{C}$ .
2. Soldering time : 3-4 sec.
3. Repeating time : no more than 3 times.
4. If soldering flux is used, be sure to remove any remaining flux after finishing soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended to protect the surface with a cover during soldering to prevent any damage due to flux spatters.

#### ◆ **Precautions For Storing OLED Module:**

1. Be sure to store the OLED Module in the vacuum bag with dessicant.
2. If the Module can not be used up in 1 month after the bag being opened, make sure to seal the Module in the vacuum bag with dessicant again.
3. Store the Module in a dark place, do not expose to sunlight or fluorescent light.
4. The polarizer surface should not touch any other objects. It is recommended to store the Module in the shipping container.
5. It is recommended to keep the temperature between  $0^{\circ}\text{C}$  and  $30^{\circ}\text{C}$  , the relative humidity not over 60%.

#### ◆ **Limited Warranty**

Unless relevant quality agreements signed with customer and law enforcement, for a period of 12 months from date of production, all products (except automotive products) TRULY will replace or repair any of its OLED modules which are found to be functional defect when inspected in accordance with TRULY OLED acceptance standards (copies available upon request). Cosmetic/visual defects must be returned to TRULY within 90 days of shipment. Confirmation of such date should be based on freight documents. The warranty liability of TRULY is limited to repair and/or replacement on the terms above. TRULY will not be responsible for any subsequent or consequential events.

#### ◆ **Return OLED Module Under Warranty:**

1. No warranty in the case that the precautions are disregarded.
2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects.

#### ◆ **PRIOR CONSULT MATTER**

1. For TRULY standard products, we keep the right to change material ,process ... for improving the product property without any notice on our customer.
2. If you have special requirement about reliability condition, please let us know before you start the test on our samples.