smart positioning

Rev. 1.0

Data Sheet

Fastrax IT530M

This document describes the electrical connectivity and functionality of the Fastrax IT530M OEM GNSS Receiver.

August 14, 2012

Fastrax Ltd

Fastrax

TRADEMARKS

Fastrax is a registered trademark of Fastrax Ltd.

All other trademarks are trademarks of MediaTek, Inc. or either of respective holders.

COPYRIGHT

DISCLAIMER

This document is compiled and kept up-to-date as conscientiously as possible. Fastrax Ltd cannot, however, guarantee that the data are free of errors, accurate or complete and, therefore, assumes no liability for loss or damage of any kind incurred directly or indirectly through the use of this document. The information in this document is subject to change without notice and describes only generally the product defined in the introduction of this documentation. Fastrax products are not authorized for use in life-support or safety-critical applications. Use in such applications is done at the sole discretion of the customer. Fastrax will not warrant the use of its devices in such applications.

REFERENCES

Ref. #	Publisher; Reference
(1)	Fastrax; NMEA Manual for Fastrax IT500 Series GPS receivers
(2)	Fastrax; Reflow_soldering_ profile.pdf
(3)	Fastrax; LOCUS manual for Fastrax IT500 Series

CHANGE LOG

Rev.	Notes	Date
1.0	Initial documentation	2012-08-14

1 Contents

2 Overview

2.1 General

The Fastrax IT530M is an OEM GNSS receiver module variant based on Fastrax IT530 with the Mediatek MT3333 chip that supports All-in-One GNSS hybrid navigation. The Fastrax IT530M receiver provides extremely low power and very fast TTFF together with weak signal acquisition and tracking capability to meet even the most stringent performance expectations in navigation with hybrid solution using signals from both GPS + Glonass GNSS systems. Future GNSS systems like Galileo or Beidou can be supported with future firmware upgrade in GPS + Galileo or GPS + Beidou modes. The module has ultra small form factor 9.6x9.6 mm, height is 1.85 mm nominal (2.15 mm max) and can be assembled with SMT reflow soldering.

The IT530M provides complete signal processing from antenna input to host port UART and location data output is in NMEA protocol. The module requires a main and a backup power supply. The host port is configurable to UART during power up. Host data and I/O signal levels are 2.8V CMOS compatible and inputs are 3.6V tolerable. The host interface equals to the IT530 module variant excluding TIMER output signal (open drain), which is now FORCE_ON input signal; the external power switch used with IT530 low power modes is now embedded in to IT530M.

The IT530M supports a new feature called AlwaysLocate™, which is an intelligent controller of the IT530M power saving mode. Depending on the environment and motion conditions, the module can adaptively adjust the navigation activity and fix rate based on measured velocity in order to achieve a balance in positioning accuracy, fix rate and power consumption.

The module is also optionally self-assisted since the EASY™ (Embedded Assist System) ephemeris extension is embedded in the software without any resources required from the host. The EASY™ data is stored on internal flash memory and allows fast TTFF typ. 3 seconds over 3 days. Also EPO™ (Extended Prediction Orbit) server generated extended ephemeris input is also supported, which allows fast TTFF 10 seconds typ. over 7/14 days.

The IT530M contains also an AIC (Active Interference Cancellation), which provides state-of-art narrow band (CW) interference and jamming elimination up to 12 CW jammers < -80dBm.

The module also supports a logging feature called LOCUS, which enables automatic logging of position data to internal flash memory. The logging capacity is >16 hrs typ. @ 15 sec storage interval.

The antenna input supports passive and active antennas with excellent out-of-band blocking rejection and provides also an input for externally generated antenna bias supply.

This document describes the electrical connectivity and main functionality of the Fastrax IT530M OEM GNSS Receiver module.

2.2 Block diagram

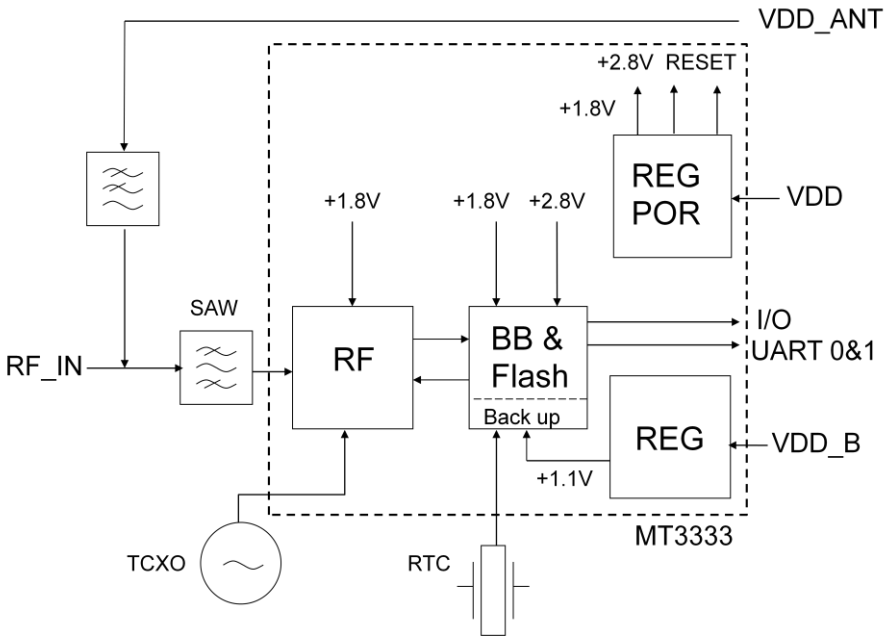

Figure 1 Block diagram

2.3 Frequency Plan

Clock frequencies generated internally in the Fastrax IT530M receiver:

- Switched Mode Power Supply (in PWM and PFM modes)
- 32768 Hz Real Time Clock (RTC)
- 16.368 MHz Master Clock (TCXO)
- 3177.2 MHz Local Oscillator (LO) of the RF down-converter (GPS+Glonass mode)
- LO/2, i.e. 1588.6 MHz of the RF down-converter (GPS+Glonass mode)

2.4 General Specifications

Table 1 General specifications

Receiver	GNSS L1 C/A-code, SPS of GPS + Glonass, Galileo or Beidou
Chip set	Mediatek MT3333
Channels	99/33 (search/track)
Tracking sensitivity	-165 dBm typ. (GPS)
Navigation sensitivity	-165 dBm typ. (GPS)
Navigation sensitivity, re-acq.	-160 dBm typ. (GPS)
Navigation sensitivity, cold acq.	-148 dBm typ. (GPS)
Update rate	1 Hz (configurable up to 10 Hz)
Position accuracy *(note 1)*	3.0 m (67%) typ. Horizontal 5.0 m (67%) typ. Vertical 0.02 m/s (50%) typ. Velocity
Max altitude/velocity	<60,000 ft/<1,000 knots
Differential GPS	SBAS default (WAAS, EGNOS, MSAS, GAGAN, QZSS), RTCM
Time to First Fix, cold acq.	23 s typ. (*note 1*)
Time to First Fix, warm acq.	23 s typ. *(note 1)*
Time to First Fix, hot acq.	1 s typ. *(note 1)*

Supply voltage, main VDD	+3.0 … +4.3 V
Supply voltage, backup VDD_B	+2.0 … +4.3 V
Power consumption, Full Power	57 mW typ. @ 3.3 V *(note 2)*
Power consumption, AlwaysLocate™	tbd mW typ. @ 3.3 V
Power consumption, Backup state	30 µW typ. @ 3.0 V
External RF amplifier net gain range	0… +30 dB
Storage temperature	-40°C…+85°C
Operating temperature	-40°C…+85°C
Host port configuration	UART
Host port protocol	NMEA-0183 rev. 3.01
Serial data format (UART)	8 bits, no parity, 1 stop bit
Serial data speed (UART)	115,200 baud (configurable 4,800... 921,600 baud)
PPS output	200 ms high pulse, rising edge +/-10 ns @ full second GPS epoch

Note 1: With nominal GNSS signal levels -130dBm.

Note 2: @ 1Hz navigation, GPS + Glonass mode, SBAS enabled, average over 24h

3 Operation

3.1 Operating Modes

After power up the IT530M module boots from the internal ROM to Navigation Mode. Modes of operation:

- Navigation Mode (Full Power)
  - Power management system modes
- Standby Mode
- Backup State/Mode
- Reset State

3.2 Full Power Mode

The module will enter Full Power (aka Navigation Mode) after first power up with factory configuration settings. Power consumption will vary depending on the amount of satellite acquisitions and number of satellites in track. This Mode is also referenced as *Full On, Full Power* or *Navigation* Mode.

Navigation is available and any configuration settings are valid as long as the main VDD and backup VDD_B power supplies are active. When the main VDD and backup VDD_B supply is powered off, settings are reset to factory configuration and receiver performs a cold start on next power up.

Suggestion is to keep the backup supply VDD_B active all the time in order to sustain on time, position and ephemeris in the backup RTC and RAM. The main VDD supply can be used to control the module activity, i.e. when VDD is switched off, the module operation is stopped.

Navigation fix rate can be configured by a NMEA command, see chapter 0. Note that baud rate must be set high enough or message payload low enough in order to pass through all messages pending.

3.2.1 Host port configuration

Default host port is configured to UART Port 0 by keeping GPIO9 and GPIO10 floating (not connected) during power up. UART Port1 is reserved for DGPS/RTCM protocol.

Default protocol for host communication is NMEA at 115,200 baud. Details on NMEA protocol can be found in NMEA manual, ref (1). Default NMEA message output configuration: $GPGGA, $GNGSA, $GPGSV, $GPRMC, $GPVTG and $GLGSV rate every second. The module supports also proprietary $PMTK input commands, see ref (1). The message payload consists of $PMTK<cmd_id>,<data_field(s)>*<chk_sum><CR><LF>. Sample command: $PMTK000*32<CR><LF>. For clarity <CR><LF> are not displayed in the following example messages but should be added to the payload at host.

3.3 Power Management Modes

The IT530M module supports also low power operating modes for reduced power consumption:

1. Standby Mode: In this Mode the receiver stops navigation and internal processor enters standby state; current drain at main supply VDD is reduced to 0.4 mA typ. Standby Mode is entered by sending NMEA command: $PMTK161,0*28. Host can wake up the module from Standby Mode to Full Power Mode by sending any byte via host port.

2. Backup Mode: (Support TBD) In this mode the receiver is configured to enter autonomously to Backup State; the main power supply VDD shall be still active but supply is controlled internally on/off. In this mode the receiver stays in Backup state (VDD and backup supply VDD_B active) and VDD current is reduced to tbd mA. Backup Mode is entered by sending NMEA command: $PMTK225,4*2F. Host can wake up the module via host control signal FORCE_ON signal toggle to high state *(t>tbd ms)*.

3. Periodic Mode: (Support TBD) This mode allows autonomous power on/off with reduced fix rate to reduce average power consumption, see figure below; the main power supply VDD is controlled on/off externally by a power switch that is controlled by the TIMER signal output, see reference circuit in chapter 7.1. Periodic Mode is entered by sending the following NMEA command: $PMTK225,**<Type>**,**<Run_time>**,**<Sleep_time>**,<**2nd**_**run_time**>,<**2nd**_**sleep_time**>*<checksum><CR><LF>, where **Type**=1 for Periodic Backup Mode; **Run_time** = Full Power period (ms); **Sleep_time** = Standby/Backup period (ms); **2nd_run_time** = Full Power period (ms) for extended acquisition in case GNSS acquisition fails during the **Run_time**; **2nd_sleep_time** = Standby/Backup period (ms) for extended sleep in case GNSS acquisition fails during the **Run_time**. Example: $PMTK225,1,3000,12000,18000,72000*16 for periodic Mode with 3 sec Navigation and 12 sec sleep in Backup state. Acknowledge response for the command is $PMTK001,225,3*35. The module can exit Periodic Mode by command $PMTK225,0*2B sent just after the module has been wake up from previous sleep cycle.

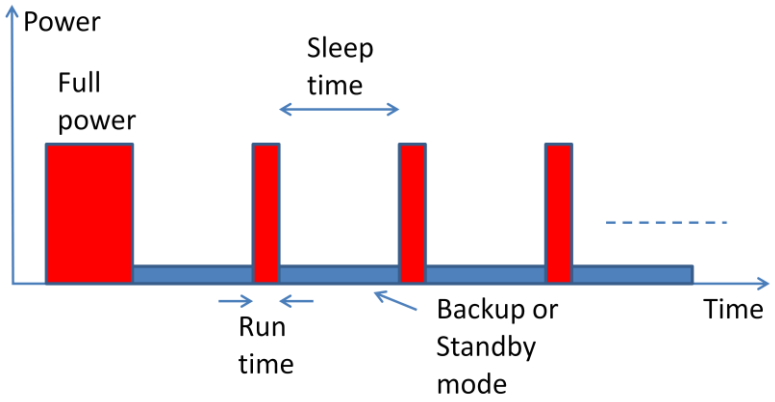

Figure 2 Periodic Mode

4. AlwaysLocate™ (Support TBD) is an intelligent controller of the Periodic Mode; the main power supply VDD is controlled on/off externally by a power switch that is controlled by the TIMER signal output, see reference circuit in chapter 7.1. Depending on the environment and motion conditions, the module can autonomously and adaptively adjust the parameters of the Periodic Mode, e.g. on/off ratio and fix rate to achieve a balance in positioning accuracy and power consumption, see figure below. The average power drain can vary based on conditions; typical average power is 3 mW. Associated profiles are: High and Low Speed, Walking, Outdoor Static and Indoor. AlwaysLocate™ Mode is entered by sending the following NMEA command: $PMTK225,<**Mode**>*<checksum><CR><LF>, where **Mode**=9 for AlwaysLocate™ in Backup Mode. Example: $PMTK225,9*22. Acknowledge response for the command is $PMTK001,225,3*35. The module can exit AlwaysLocate™ Mode by command $PMTK225,0*2B sent just after the module has been wake up from previous sleep cycle.

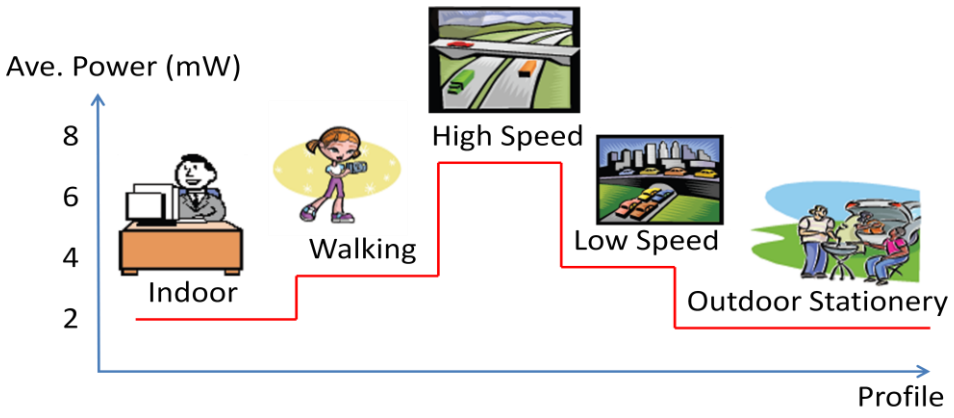

Figure 3 AlwaysLocate™ Mode

The module can control the embedded VDD power switch autonomously only after the IT530M is set to Periodic, Backup or to AlwaysLocate™ mode by a NMEA command.

Note also that first fix position accuracy can be somewhat degraded in Power Management Modes when compared to Full Power operation. User can improve the position accuracy by taking the 2nd or 3rd fix after waking up.

User can exit low power Modes 3… 4 to Full Power by sending NMEA command $PMTK225,0*2B just after the module has woke up from previous sleep cycle.

3.4 Self-Assistance EASY™ usage

The IT530M module self-assistance (Support TBD) uses EASY™ (Embedded Assist System) ephemeris extension, which is embedded in the software without any resources required from the host. The EASY™ data is stored on internal flash memory and allows fast TTFF typ. 3 seconds over 3 days and is enabled by default.

Allow the receiver to navigate at least for 5 minutes with good GNSS satellite visibility in order to collect broadcast ephemeris and to process necessary information.

3.5 Server Assistance EPO™ usage

The IT530M module supports also input from server generated EPO™ file (Extended Prediction Orbit, i.e. ephemeris extension for GPS signals only), which can be transferred from a FTP server and allows fast TTFF with GPS signal typ. 10 seconds over 7/14 days. Contact Fastrax support for details on EPO FTP server usage.

3.6 Logger LOCUS usage

The IT530M module supports (Support TBD) embedded logger function called LOCUS and when enabled it can log position information to internal flash memory; default log interval is 15 seconds that provides typically > 16 h log capacity. The LOCUS can be enabled by NMEA command $PMTK185,0*22. Contact Fastrax support for details on Locus usage, see ref (3).

3.7 DGPS usage

By default DGPS/SBAS navigation mode is enabled. The search for suitable SBAS satellite signal is automatic.

The host may either enable DGPS/RTCM navigation mode by sending command ‘Set DGPS Data Source to RTCM’ $PMTK301,1*2D. The UART Port1 is used for RTCM message input at 9600 baud.

Note that DGPS usage is only supported with GPS system at 1 Hz navigation rate in Full Power mode. Note also that acquiring necessary DGPS correction parameters may take up to 1 minute prior DGPS fix status is achieved, which is indicated in the $GPGGA message, Fix Valid Indicator. Note also that DGPS corrections do not provide corrections against multipath errors that are local; thus accuracy is not necessary improved in urban environments.

3.8 Backup State

Backup State means a low quiescent (10 µA typ. at VDD_B) power state where receiver operation is stopped; only the backup supply VDD_B is powered on while the main supply VDD is switched off by host (or autonomously by IT530M, see also chapter 3.3). Waking up from Backup State to Full Power is controlled by host by switching on the VDD supply.

After waking up the receiver will use all internal aiding like GNSS time, Ephemeris, Last Position etc. resulting to a fastest possible TTFF in either Hot or Warm start modes.

During Backup State the I/O block is powered off; thus suggestion is that host shall force it’s outputs to low state or to high-Z state during Backup state to minimize small leakage currents (<10 µA typ.) at receiver’s input signals.

3.9 Reset State

Reset State stops all internal operations and it is entered internally at power up after which internal reset state is relaxed when 167 ms (typ.) has elapsed and module operations begin. The power on reset level is 2.7 +/- 0.1 V at VDD. Host can also override Reset State via RESET_N input, which is low state active. Normally external reset override is not required and RESET_N signal can be left floating (not connected).

4 Connectivity

4.1 Signal Assignments

The I/O signals are available as soldering (castellated) pads on the bottom side of the module. These pads are also used to attach the module on the motherboard. All digital I/O signal levels are 2.8 V CMOS compatible (except TIMER and 32K/DR_INT that are 1.1 V CMOS) and inputs are 3.6 V tolerable. All unconnected I/O signals can be left unconnected when not used, unless instructed to use external pull up/down resistor.

Table 2 Signal assignment

Contact	Signal	I/O type Full Power, Stanby	I/O type Backup	I/O type Reset	Signal description
1	VDD	P,I	-	P,I	Power supply input +3.3 V nom. *De-couple externally with e.g. 4.7 uF low ESR ceramic capacitor.*
2	VDD_B	P,I	P,I	P,I	Backup power input +3.3 V nom. *De-couple externally with e.g. 1 uF low ESR ceramic capacitor.*
3	VDD_ANT	P,I	P,I	P,I	Antenna bias power supply input up to +/-5.5 V. *Leave floating or connect to GND when not used. When used de-couple signal further externally, see Reference Circuit Diagram.*
4	GND	G	G	G	Ground
5	GND	G	G	G	Ground
6	RF_IN	A,I,P,O	A,I,P,O	A,I,P,O	Analog Antenna input (50 ohm), Antenna bias voltage output (low-pass filtered from VDD_ANT)
7	GND	G	G	G	Ground
8	GND	G	G	G	Ground
9	GND	G	G	G	Ground
10	GND	G	G	G	Ground
11	GPIO9	C,B	HZ	C,B	*Reserved for future usage, leave floating.*
12	RESET_N	C,I,PU	C,I,PU	C,I,PU	External reset input, active low. *Can be left unconnected when not used.*
13	GPIO10	C,B	HZ	C,B	*Reserved for future usage, leave floating.*
14	GND	G	G	G	Ground
15	TX0	C,B	HZ	C,B	UART Port0 TX data transmit (NMEA)
16	RX0	C,B	HZ	C,B	UART Port0 RX data receive (NMEA), PU. *Can be left unconnected when not used.*
17	FORCE_ON	C1V1,I	C1V1,I	C1V1,I	Power control input used to force wake up from low power modes. *When not used connect to Ground externally.*
18	GND	G	G	G	Ground
19	GND	G	G	G	Ground
20	PPS	C,B	HZ	C,B	- PPS Time Mark output signal (default) - GPIO7
21	WAKEUP	P,O	-	P,O	2.8V power output for optional control of external LNA bias switch, active high = LNA bias on. Max load current drain 2 mA. *Can be left*

Contact	Signal	I/O type Full Power, Stanby	I/O type Backup	I/O type Reset	Signal description
					unconnected when not used.
22	32K/DR_INT	C1V1,B	C1V1,B	C1V2,B	- Wake up interrupt (DR_INT default), PD. *Can be left unconnected when not used.* - Optionally 32678 Hz RTC clock output
23	UI_FIX	C,B	HZ	C,B	- Fix indicator output (default). *Can be left unconnected when not used.* - GPIO6
24	GND	G	G	G	Ground
25	TX1	C,B	HZ	C,B	UART Port1 TX data transmit. *Can be left unconnected when not used.*
26	RX1	C,B	HZ	C,B	UART Port1 RX data receive (RTCM), PU. *Can be left unconnected when not used.*
27	EINT1	C,B	HZ	C,B	- Standby Mode control input (not supported). *Can be left unconnected when not used.* - GPIO13
28	GND	G	G	G	Ground

Note (a): Pull Up/down resistor present only shortly after power up.

Legend: A=Analogue, B=Bidirectional, C=CMOS 2.8 V, C1V1=CMOS 1.1 V, G=Ground, HZ=High Impedance, I=Input, O=Output, OD=Output Open Drain, P=Power, PU=Internal Pull Up resistor, PD=Internal Pull Down resistor. Note that with Birectional I/O the firmware has control for input vs. output I/O type depending on the firmware function.

4.2 Power supply

The Fastrax IT530M module requires two separate power supplies: VDD_B for non-volatile back up block (RTC/Backup RAM) and the VDD for digital parts and I/O. VDD can be switched off when navigation is not needed but if possible keep the backup supply VDD_B active all the time in order to keep the non-volatile RTC & RAM active for fastest possible TTFF.

Main power supply VDD current varies according to the VDD level, to the processor load, to the number of satellites is track and to the rate of satellite re-acquisition. Typical VDD peak current is 27 mA (typ.) during GNSS acquisition after power up and typical average 17 mA (VDD 3.3 V) over 24 h during good sky visibility in GPS + Glonass mode. Note that average current drain will also increase during following features:

- 17 mA average (typ.) @1 Hz navigation, GPS + Glonass mode, good sky visibility
- +4 mA @ during first 12.5 minutes after cold start due to receiving broadcast almanac data
- +tbd mA @ 5 Hz navigation rate
- +tbd mA @ 10 Hz navigation rate
- +tbd mA @ Jammer Remover AIC usage

The following picture shows average current and power drain variation vs. VDD supply voltage.

Figure 4 IT530M Power Drain (typ.) vs. VDD (V)

Back up supply VDD_B draws 10 µA typ. current in Backup State. During Full Power Mode VDD_B current typically peaks up to 60 µA and is on the average 40 µA.

NOTE

Backup supply VDD_B has to be active whenever Main supply VDD is active.

By-pass the VDD supply input by a low ESR ceramic de-coupling capacitor (e.g. 4.7 uF) placed nearby VDD pin to ensure low ripple voltage at VDD.

NOTE

De-couple the VDD input externally with e.g. 4.7uF low ESR ceramic capacitor connected to GND. The module has also internal a low ESR (~0.01 ohm) by-pass capacitor at VDD supply input. Ensure that the external regulator providing VDD and VDD_B supply is compatible with low ESR load capacitors.

4.3 Host port configuration

Default host port is UART and selected by leaving GPIO 9 and 10 signals floating (not connected) after power up. Other host port configurations are not supported.

4.4 Host port UART

UART Port 0 is normally used for GNSS data reports and receiver control. Serial data rates are configurable from 4,800 baud to 921,600 baud by $PMTK251,<baud>*<checksum><CR><LF> command. Default baud rate is 115,200 baud; protocol is NMEA. RX signal is pulled up internally and can be left floating (not connected) when not used.

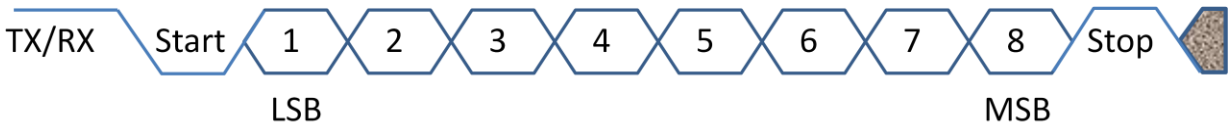

Figure 5 UART timing

Secondary UART Port 1 is configured to RTCM differential GPS data input at 9600 baud.

4.5 Reset input

The RESET_N (active low) signal provides external override of the internally generated power up/down reset. Normally external control of RESET_N is not necessary.

When RESET_N signal is used, it will force volatile RAM data loss. Note that Non-Volatile Backup RAM content is not cleared and thus fast TTFF is possible. The input has internal pull up resistor 85 kohm typ. and the signal can be left floating (not connected) if not used. Non-Volatile Backup RAM content can be cleared with NMEA command 'Factory Reset' $PMTK104*37<CR><LF>.

4.6 FORCE_ON input

The FORCE_ON signal provides input that can be used to force wakeup from low power modes. The signal is active high and shall be at high state at least > tbd ms for wakeup.

4.7 Antenna input

The antenna shall provide simultaneous reception of both GPS 1575 MHz and Glonass bands 1598… 1606 MHz. The module supports both passive and active antennas; the latter gives some advantage in sensitivity and thus suggestion is to use amplified antenna signal. The antenna input RF_IN impedance is 50 ohms and it provides also a bias supply low-pass filtered from VDD_ANT supply. The RF input signal path contains first a SAW band-pass filter before internal LNA, which provides good out-of-band protection against GNSS blocking caused by possible near-by wireless transmitters.

Note that antenna input is ESD sensitive. With passive antennas the ESD performance can be improved by connecting VDD_ANT supply input to GND. Also an external TVS diode with low capacitance (<0.5pF, e.g. Infineon ESD0P2RF) can be used to improve RF-input ESD capability.

NOTE

With Passive antennas leave VDD_ANT not connected or connect to GND.

4.8 Active GNSS antenna

The customer may use an external active GNSS antenna when antenna cable loss exceeds > 1dB. It is suggested the active antenna has a net gain *including cable loss* in the range from +10 dB to +25 dB. Specified sensitivity is measured with external low noise (NF≤1dB, G≥15dB) amplifier, which gives about 3 dB advantage in sensitivity when compared to a passive antenna.

An active antenna requires certain bias voltage, which can be supplied externally via VDD_ANT supply input. De-couple externally the VDD_ANT input; see the application circuit diagram in chapter 6. The external bias supply must provide limitation of the max current below 150mA during e.g. antenna cable short circuit condition.

When the module is in Standby/Backup mode, the antenna bias can be switched off externally by using WAKEUP signal output to switch off VDD_ANT supply, see e.g. Application Circuit Diagram.

NOTE

With an Active GNSS Antenna provide antenna supply externally via VDD_ANT. The VDD_ANT supply must provide also short circuit protection externally, rated current 70mA, abs. max. 150mA.

4.8.1 Jamming Remover

Jamming Remover is an embedded HW block called AIC (Active Interference Cancellation) that tracks and removes up to 12 pcs CW (Carrier Wave) type signals up to -80 dBm (total power signal levels). By default the AIC is disabled and usage requires an NMEA command $PMTK286,1*23<CR><LF> to enable.

Jamming Remover can be used for solving EMI problems in the customer's system and it is effective against e.g. narrow band clock harmonics. When enabled, Jammer Remover will increase current drain by about 1 mA and impact on GNSS performance is low at modest jamming levels; however at high jammer levels -90… -80 dBm the RF signal sampling (ADC) starts to get saturated after which GNSS signal levels start to reduce.

Note that Jamming Remover is not effective against wide band noise (e.g. from host CPU memory bus), which cannot be separated from thermal noise floor. Wide band Jamming signal increases effective noise floor and eventually reduces GNSS signal levels.

4.9 PPS output

The PPS output signal provides pulse-per-second output pulse signal for timing purposes. Pulse length (high state) is 100 ms and it has 1us accuracy synchronized at rising edge to full UTC second with nominal GNSS signal levels. The PPS will output PPS after a few seconds from first fix after the fix epoch is synchronized to full second.

The PPS output is valid when navigation is valid and will also continue 'freewheel' after valid fix is lost by a certain navigation DR timeout, typ. 10 seconds. User can also enable NMEA $GPZDA message that is sent right after the PPS pulse just sent.

4.10 Wakeup output

The WAKEUP output voltage provides indication to e.g. external LNA bias switch that the module is active and navigation. Polarity is active high = LNA bias active.

WAKEUP output is intended to drive only CMOS inputs; do not load WAKEUP signal with current exceeding 2mA. Only loads with steady state current drain is allowed (i.e. loads with ripple currents are prohibited).

NOTE

Do not load WAKEUP output with current exceeding 2mA. Only loads with steady state current drain is allowed, i.e. loads with ripple currents are prohibited.

4.11 Interrupt input EINT1

The default EINT1 function is Standby mode control but the function is not supported; leave signal floating (not connected).

4.12 UI_FIX signal

The default UI_FIX function is valid fix indicator output. Without a valid fix the signal is at low state; during valid fix condition the signal outputs 0.1 s pulses every 1 second.

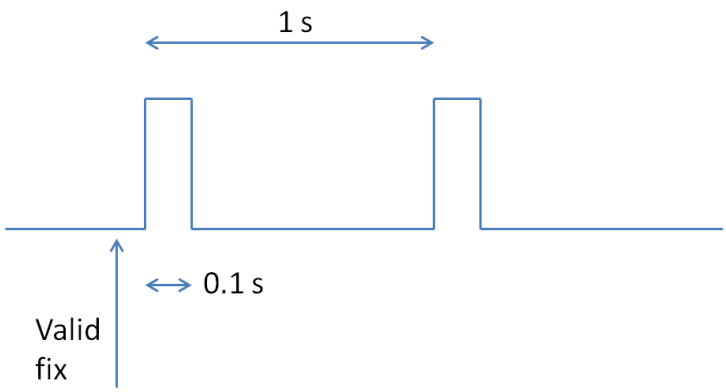

Figure 6 UI_FIX valid fix indicator timing

4.13 32K/DR_INT signal

The default 32K/DR_INT function is wake up interrupting input. The module is able to wake up from Standby and Backup modes to Full Power mode when the signal is toggled by low-high-low state with >10 ms pulse length. While in the DR_INT function the input is pulled low with an internal pull down resistor and the input can be left floating (not connected).

Optionally the signal can be configured to 32768 Hz RTC clock signal output with a custom firmware. The 32K/DR_INT signal has CMOS 1.1V logic levels and when input, the signal is +3.6V tolerable.

4.14 Mechanical Dimensions

Module size is square 9.6 mm (width), 9.6 mm (length) and 1.85 mm (height, 2.15 mm max). General tolerance is ±0.3 mm. Note pin 1 polarity mark on the corner on the shield.

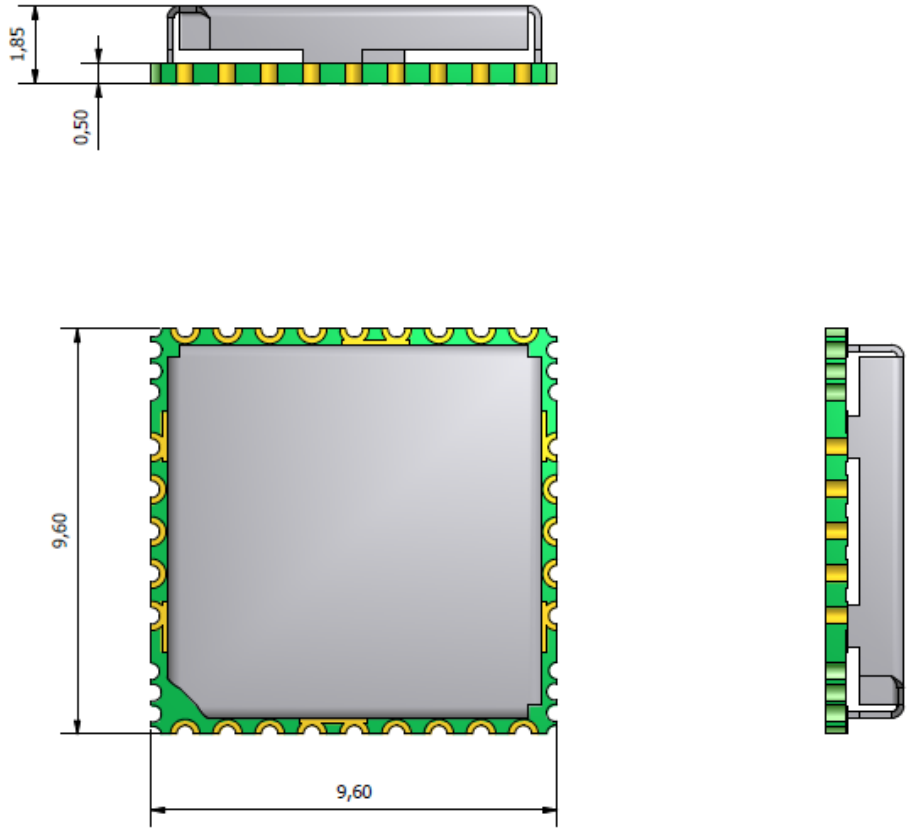

Figure 7 Mechanical Dimensions

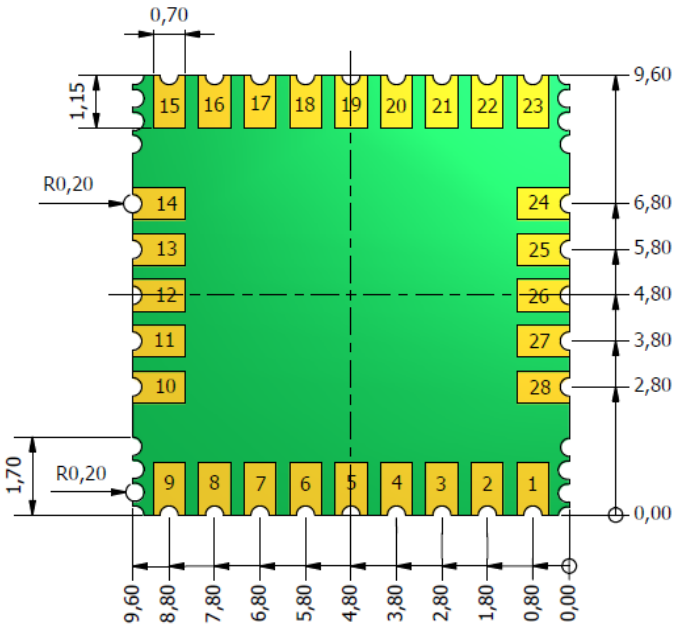

Figure 8 Pin numbering and dimensions, bottom view

4.15 Suggested pad layout

Suggested paste mask openings equal to pad layout. Note the keepout (void area) 4.8x7.2mm for copper & trace & components for all layers under the embedded antenna.

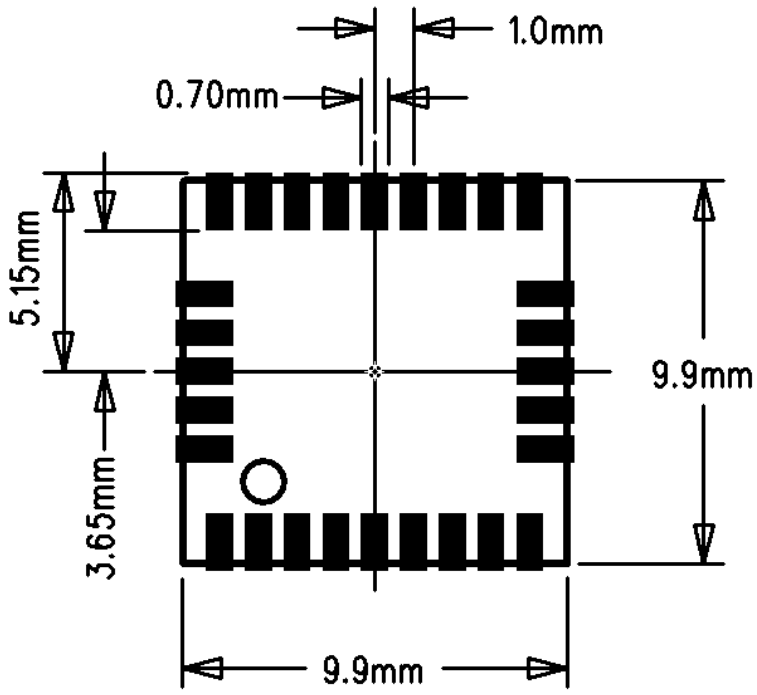

Figure 9 Suggested pad layout and occupied area, top view

5 Electrical Specifications

5.1 Absolute Maximum Ratings

Stressing the device beyond the Absolute Maximum Ratings may cause permanent damage. Operation beyond the DC Electrical Specifications is not recommended and extended exposure beyond the Recommended Operating Conditions can affect device reliability.

Table 3 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
T_{AMB}	Operating and storage temperature	-40	+85	°C
P_{DIS}	Power dissipation	-	200	mW
VDD	Supply voltage input	-0.3	+4.3	V
VDD_B	Supply voltage input, Backup	-0.3	+4.3	V
VDD_ANT	Supply voltage input, Antenna Bias	-5.5	+5.5	V
I_{VDD_ANT}	Antenna Bias Current	-150	+150	mA
V_{IO}(ESD)	IO ESD voltage (only RF_IN, Machine Model)	-50	+50	V
V_{IO}(ESD)	IO ESD voltage (excluding RF_IN, HBM Model)	-1000	+1000	V
P_{RF}	RF_IN input power (in band 1575 +/- 10 MHz)	-	-40	dBm
P_{RF}	RF_IN input power (out of band <1460 MHz or >1710 MHz)	-	+15	dBm

NOTE

Note that module is Electrostatic Sensitive Device (ESD).

5.2 DC Electrical specifications

Operating conditions are T_{AMB} =+25°C, VDD =+3.3 V and VDD_B =+3.0 V unless stated otherwise.

Table 4 DC Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{AMB}	Operating temperature	-40	+25	+85	°C
VDD	Supply voltage input	+3.0	+3.3	+4.3	V
VDD_B	Supply voltage input, Backup	+2.0	+3.0	+4.3	V
I_{VDD} (peak)	Supply current, peak acq.		27		mA
I_{VDD} (ave)	Supply current average, tracking		17		mA
I_{VDD_B} (peak)	Supply current Backup, peak		60		µA
I_{VDD_B} (ave)	Supply current Backup, average		40		µA
I_{VDD_B}	Supply current, Backup state		10		µA
$I_{I(LEAK)}$	Leakage current, Digital Input	-10		+10	µA
V_{OL}	Low level output voltage, I_{OL} 2 mA	-		+0.4	V
V_{OH}	High level output voltage, I_{OH} 2 mA	+2.4	-	-	V
V_{IL}	Low level input voltage	-0.3		+0.7	V
V_{IH}	High level input voltage	+2.1		+3.6	V

R_{PU}	Internal Pull Up resistor	40	85	190	kohm
R_{PD}	Internal Pull Down resistor	40	85	190	kohm

Table 5 DC Electrical characteristics, 1.1 V CMOS domain (FORCE_ON & 32K/DR_INT)

Symbol	Parameter	Min	Typ	Max	Unit
V_{OL}	Low level output voltage, I_{OL} 2 mA	-		+0.165	V
V_{OH}	High level output voltage, I_{OH} 2 mA	+0.78		-	V
V_{IL}	Low level input voltage	-0.3		+0.275	V
V_{IH}	High level input voltage	+0.935		+3.6	V
R_{PU}	Internal Pull Up resistor	130		560	kohm
R_{PD}	Internal Pull Down resistor	130		560	kohm

5.3 AC Electrical characteristics

Operating conditions are T_{AMB} =+25°C and VDD =+1.8 V unless stated otherwise.

Table 6 AC Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{PPS}	PPS cycle time		1		s
$t_{PPS,H}$	PPS, high state pulse length		200		ms
Δt_{PPS}	PPS accuracy, rising edge (*note 1*)	-10		+10	ns TBD
f_{RTC}	RTC output (32K/DR_INT) frequency (*note 2*)		32768		Hz

Note 1: with nominal GPS signal levels -130dBm.

Note 2: when enabled by I/O configuration.

6 Manufacturing

6.1 Assembly and Soldering

The IT530M module is intended for SMT assembly and soldering in a Pb-free reflow process on the top side of the PCB. Suggested solder paste stencil height is 150um minimum to ensure sufficient solder volume. If required paste mask pad openings can be increased to ensure proper soldering and solder wetting over pads.

Use pre-heating at 150… 180°C for 60… 120 sec. Suggested peak reflow temperature is 235… 245°C (for SnAg3.0Cu0.5 alloy). Absolute max reflow temperature is 260°C. For details see Fastrax document 'Soldering Profile' ref (7).

Note that module is Electrostatic Sensitive Device (ESD).

NOTE

Note that module is Electrostatic Sensitive Device (ESD).

Avoid also ultrasonic exposure due to internal crystal and SAW components.

The IT530M module meets the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS). For details contact Fastrax support.

6.2 Moisture sensitivity

IT530M module is moisture sensitive at MSL 3 (see the standard IPC/JEDEC J-STD-020C). The module must be stored in the original moisture barrier bag or if the bag is opened, the module must be repacked or stored in a dry cabin (according to the standard IPC/JEDEC J-STD-033B). Factory floor life in humid conditions is 1 week for MSL 3.

Moisture barrier bag self life is 1 year; thus it is suggested to assemble modules prior self life expiration. If the moisture barrier bad self life is exceeded, the modules must be baked prior usage; contact Fastrax support for details.

6.3 Marking

Module marking includes type code, batch code and serial number.

Type code is e.g. **IT530Mrbbbb** (may vary)**,** where

- **IT530M** is module type code for IT530M
- **r** is incremental firmware revision (e.g. **B,** may vary)
- **bbbb** is BOM (Bill-of-Materials) revision code (e.g. **4341**, may vary)

Batch code is e.g.**120208** (may vary)**,** where

- **1** is factory code
- **2** is last digit of the year (e.g. 201**2**)
- **02** is month (e.g. February)

- **08** is incremental number of the production batch during the month

Serial number is unique for each module having 10 digits including tester code, last two digits of the year, Julian date code and incremental number.

6.4 Tape and reel

Minimum order quantity is 500 pcs. Reel is packed in 500 pcs per reel.

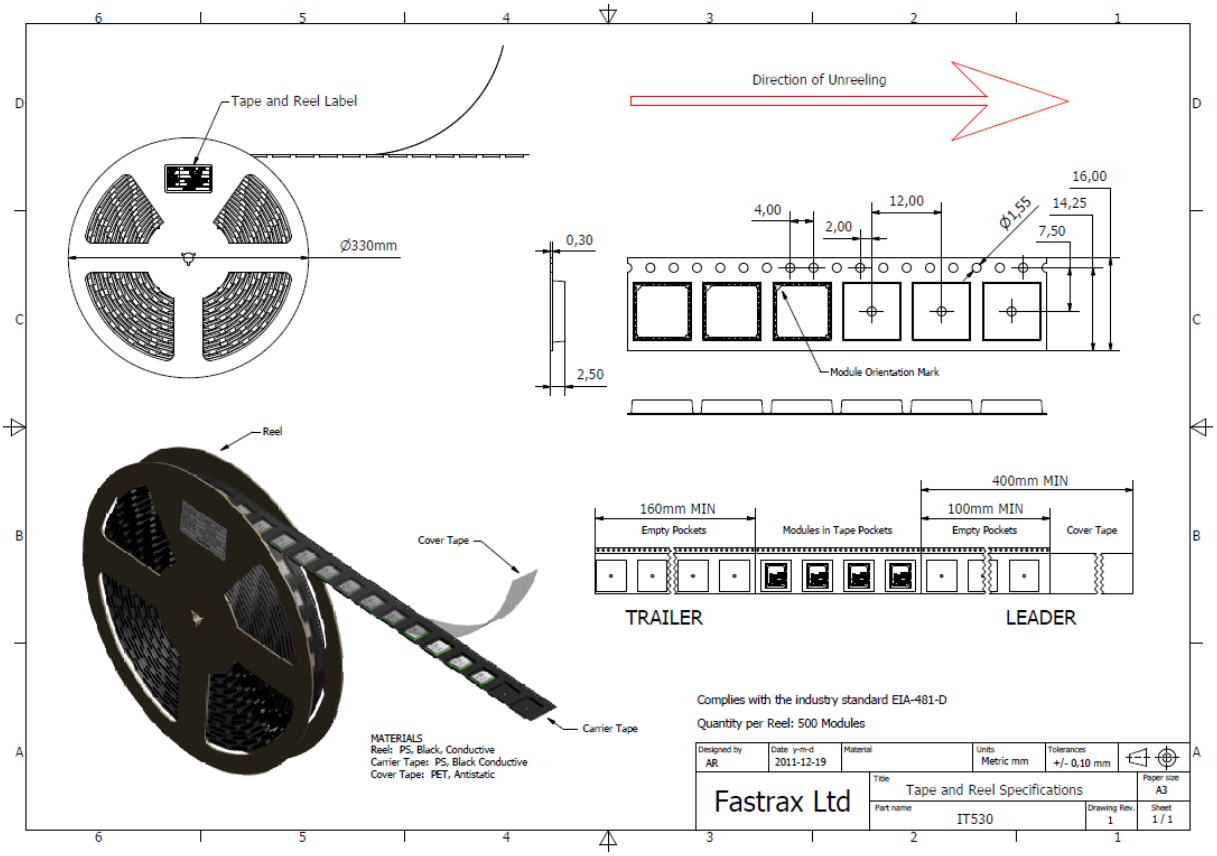

Figure 10 Tape and reel specification

6.5 Environmental Specification

The IT530M module shall be qualified for environmental stresses with the following test series:

Table 7 Environmental tests

Test	Condition	Standard
Temperature Cycle	Test: +85°C (20min) / -40°C (20min), Ramp Slope: 10°C/min, Test Cycles: 300 Cycles	JESD22A104
High Temperature Storage	Temperature +85°C , Test Time: 1,000hr	JESD22A103C
Temperature Humidity Test	Temperature +85°C , 85% R.H., Test Time: 1,000hr	JESD22A101
Vibration Test	10G, 10… 1,000Hz, 1 Octave/min (amplitude 1.0mm max @ <70Hz)	JESD22B103
Shock Test	100G pulse, duration 2ms, 5 Shock 2 directions 3 Axis = 30 Shocks	JESD22B110

7 Reference design

The idea of the reference design is to give a guideline for the applications using the OEM GNSS module. In itself it is not a finished product, but an example that performs correctly.

In the following two chapters the reader is exposed to design rules that he should follow, when designing the GNSS receiver in to the application. By following the rules one end up having an optimal design with no unexpected behavior caused by the PCB layout itself. In fact these guidelines are quite general in nature, and can be utilized in any PCB design related to RF techniques or to high speed logic.

7.1 Reference circuit diagram

The following picture describes a minimum connectivity for a typical autonomous navigation application. It consists of the IT530M module, which is powered by the main VDD supply (+3.3 V typ.) and backup supply VDD_B (+3.0V typ). The external by-pass capacitor C7 is used to de-couple the VDD supply pin close to pin 1.

Suggestion is to keep the backup supply VDD_B active all the time and host may use the VDD supply to control module activity between Full Power and Backup operation modes.

The host port is configured to UART by keeping GPIO 9 & 10 floating. Serial port TX output is connected to host UART input. RX input connection to host UART output is required when sending commands to IT530M.

Optionally WAKEUP signal can be used to drive external antenna bias VDD_ANT (+3.3 V typ.) voltage switch (Q1) during Full Power/Standby/Backup Modes. Transistor Q1 provides also Antenna Bias short circuit protection by limiting bias current to 50 mA typ. L1 and C2 provide additional RF decoupling at VDD_ANT supply.

The reference circuit supports also connectivity to IT530 (GPS only) module variant for optional Backup/Periodic modes of operation: with IT530 the external power switch U1, R8 and D2 shall be assembled while omitting by-pass resistor R9 & R11 (0R). The U1 power switch is controlled autonomously by the TIMER signal from IT530; for details see also IT530 datasheet. This way user may share the same electrical design with both IT530 and IT530M module variants.

Optional connectivity to host includes PPS, UI_FIX, 32K/DR_INT signals. UART Port 1 RX1 signal can be used optionally as input for RTCM differential GPS messages.

Note that all I/O signal levels are CMOS 2.8V compatible (excluding TIMER and 32K/DR_INT signals that have 1.2 V CMOS domain) and inputs are 3.6 V tolerable.

Some I/O signals have series resistors 47… 220 ohm, which are intended for RF-decoupling purposes to improve rejection to internally generated EMI that may leak to nearby GNSS antenna. If GNSS antenna is away > 20cm from module and/or I/O signals are routed under ground plane these series resistor may be omitted.

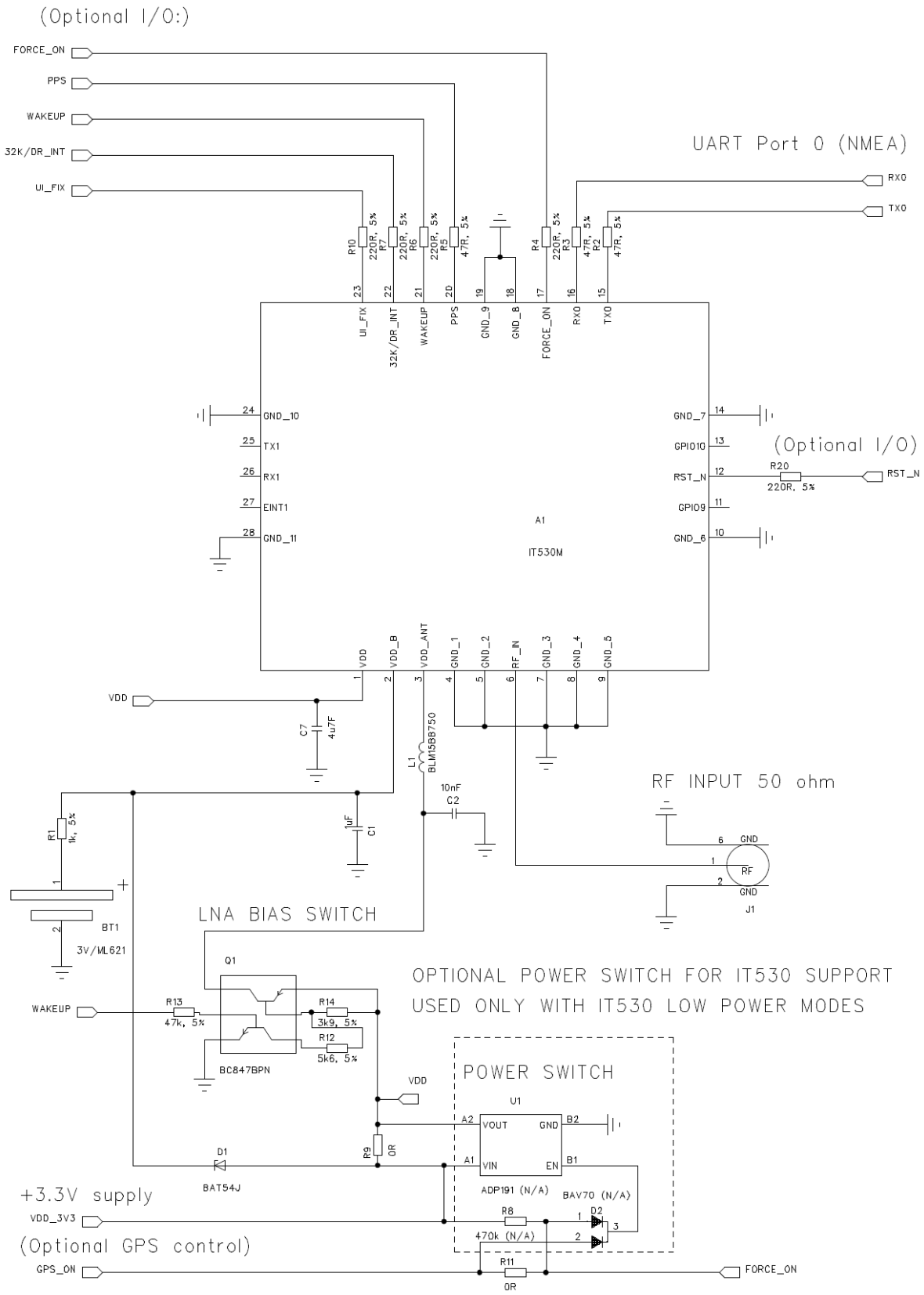

Figure 11 Reference circuit diagram

7.2 PCB layout suggestion

The suggested 4-layer PCB build up is presented in the following table.

Table 8 Suggested PCB build up

Layer	Description
1	Signal + RF trace + Ground plane with solid copper under IT530M
2	Ground plane for signals and for RF trace
3	Signals and power planes
4	Ground plane (also short traces allowed)

For a multi-layer PCB the first inner layer below the IT530M is suggested to be dedicated for the ground plane. Below this ground layer other layers with signal traces are allowed. It is always better to route very long signal traces in the inner layers of the PCB. In this way the trace can be easily shielded with ground areas from above and below.

The serial resistors at the I/O should be placed very near to the IT530M module. In this way the risk for the local oscillator leakage is minimized. For the same reason by-pass capacitors C1 and C2 should be connected very close to the module with short traces to IO contacts and to the ground plane. Place the GND via hole as close as possible to the capacitor.

Connect the GND soldering pads of the IT530M to ground plane with short traces (thermals) to via holes, which are connected to the ground plane. Use preferably one via hole for each GND pad.

The RF input should be routed clearly away from other signals, this minimizes the risk against interference. The proper width for the 50 ohm transmission line impedance depends on the dielectric material of the substrate and on the height between the signal trace and the first ground plane. With FR-4 material the width of the trace shall be two times the substrate height.

A board space free of any traces should be covered with copper areas (GND). In this way, a solid RF ground is achieved throughout the circuit board. Several via holes should be used to connect the ground areas between different layers.

Additionally, it is important that the PCB build-up is symmetrical on both sides of the PCB core. This can be achieved by choosing identical copper content on each layers, and adding copper areas to route-free areas. If the circuit board is heavily asymmetric, the board may bend during the PCB manufacturing or reflow soldering. Bending may cause soldering failures and reduce end product reliability.

The AP530 Application Board layout described in next chapter can be also used as layout reference.

7.2.1 Other electronics on mother board

Signal traces on top and bottom layers should have minimum length. Route signals mainly at inner layers below the top or bottom ground plane. In this way, a solid RF ground is achieved throughout the circuit board on top and bottom sides. Several via holes should be used to connect the ground areas between different layers.

Areas with dense component placing and dense routing requirements should be covered with a metal shield, which should be connected to ground plane with multiple GND via holes. Small ground plane openings for SMT components (length few mm, like LED or push buttons) in the ground plane are OK without a shield.

Dense areas having multiple via holes may open the ground plane for wide areas, thus blind and buried via holes are suggested to be used when changing layers for internal signals and power planes.

Use a power plane layer dedicated solely for power nets. Use wide trace width or even copper plane areas to achieve low impedance for power nets. Dedicate at least one layer as ground planes on adjacent layer above or below power plane layer in order to maximize capacitance to ground plane.

7.2.2 Avoiding EMI

Any GNSS receiver is vulnerable to external spurious EMI signals since GNSS signals are very weak below thermal noise floor. Any man made noise or spurious signals picked up by the nearby GNSS antenna increases the noise floor and reduces GNSS signal levels. Carrier Wave (CW) type spurious signals like clock harmonics on GNSS band may also cause cross correlation products that may interfere with GNSS signal tracking and cause position offsets.

The embedded GNSS antenna may pick up local EMI signals and thus it is essential for good GNSS performance that the following measures against EMI are properly implemented:

- High speed electronics like host CPU & memory bus are enclosed in a 'Faraday shield'. The electrical enclosure is formed by the ground planes on PCB + metal shield over components. Route signals at inner layers as discussed previously. Use preferably a power plane(s) layer for supply nets.
- Any signal that is routed outside the Faraday shield is protected against EMI noise on 1575MHz with a serial RF filter like
    - a serial resistor (> 330ohm, suitable for I/O with low current) or
    - with a dedicated EMI filter (or ferrite bead) suitable for higher current or
    - with suitable by-pass capacitor e.g. 18pF (low impedance due to series resonance at 1575MHz).

The following picture gives a suggestion for e.g. a 6-layer PCB build up, which forms a Faraday shield together with ground planes on PCB and with the shield over high speed electronics. Buried and blind via holes are used to keep EMI signal inside ground planes. I/O signals that are routed outside the Faraday enclosure are filtered with a suitable EMI filter. Power plane layer is used for supply nets with low impedance traces/planes.

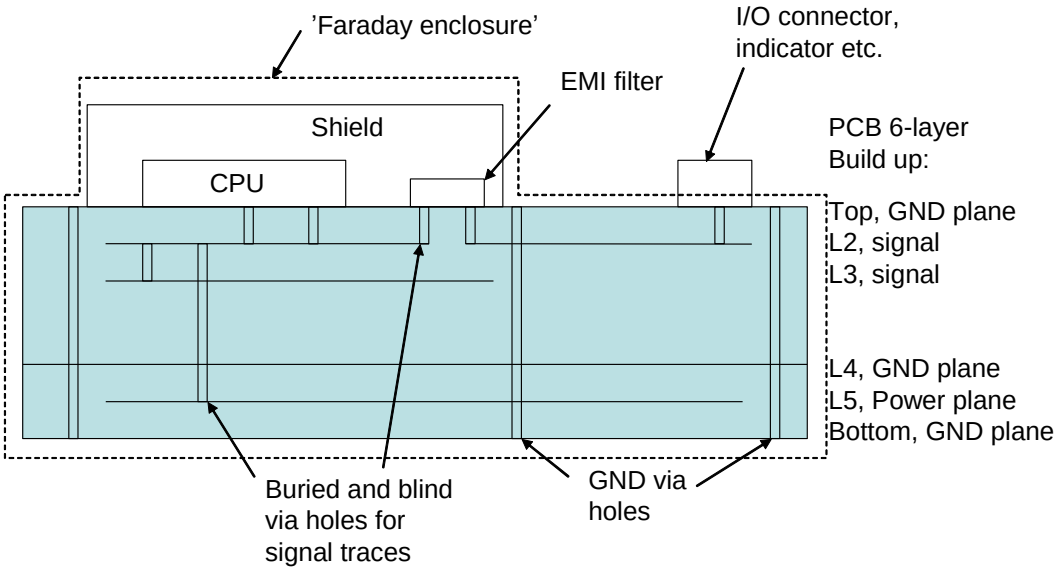

Figure 12 Avoiding EMI with Faraday enclosure

8 AP530 Application board for IT530M

The Fastrax Application Board AP530 provides the IT530M connectivity to the Fastrax Evaluation Kit or to other evaluation purposes. It provides a single PCB board equipped with the IT530M module, MCX antenna connector, Antenna Bias +3.3 V switch, VDD Power Switch, switch for GPS_ON control and 2x20 pin Card Terminal connector.

Default host port configuration is set to UART by switch S4… S6 'ON' and S7 & S8 'OFF'. S3 should be 'ON' for first power up; for successive power up and for low power modes the S3 shall be switched to 'OFF'.

8.1 Board Terminal I/O-connector

The following signals are available at the 40-pin Card Terminal I/O connector J2. The same pin numbering applies also to the Fastrax Evaluation Kit pin header J4. Note that UART Port 0 maps to serial Port 0 at the Fastrax Evaluation Kit. I/O signal levels are CMOS 3.3V compatible unless stated otherwise.

Table 9 Board Terminal signals

Pin	Signal	I/O	Alternative GPIO name	Interface to Fastrax Evaluation Kit
1	TX1	O	-	UART Port 1 async. output
2	GND	-	-	Ground
3	RX1	I	-	UART Port 1 async. input (RTCM)
4	GND	-	-	Ground
5	TX0	O	-	UART Port 0 async. output (NMEA)
6	GND	-	-	Ground
7	RX0	I	-	UART Port 0 async. input (NMEA)
8	GND	-	-	Ground
9	VDD_3V3	I	-	Power supply input +3.3V
10	GND	-	-	Ground
11	PPS	O	-	1PPS signal output
12	GND	-	-	Ground
13	RESET_N	I	-	Active low async. system reset
14	-	-	-	Not connected
15	-	-	-	Not connected
16	-	I	-	Not connected
17	GND	-	-	Ground
18	-	-	-	Not connected
19	-	-	-	Not connected
20	-	-	-	Not connected
21	GND	-	-	Ground
22	-	-	-	Not connected
23	-	-	-	Not connected
24	-	-	-	Not connected
25	GND	-	-	Ground
26	UI_FIX	O	-	UI indicator B output
27	-	-	-	UART CTS signal
28	-	-	-	Not connected
29	-	-	-	UART RTS signal
30	WAKEUP	O	-	UI indicator A output
31	GND	-	-	Ground
32	-	-	-	Not connected
33	GND	-	-	Ground
34	-	I	-	Not connected
35	GND	-	-	Ground

Pin	Signal	I/O	Alternative GPIO name	Interface to Fastrax Evaluation Kit
36	EINT1	I	-	EINT1 (Standby) control input
37	GND	-	-	Ground
38	32K/DR_INT	I/O	-	Default: DR_INT wakeup control input
39	GND	-	-	Ground
40	FORCE_ON_N	I	-	Inverted FORCE_ON control input, pulled up to VDD_3V3

8.2 Bill of materials

A1	IT530M MODULE	IT530M
BT1	PANASONIC ML621/F9D, 3V 5mAh	3V/ML621
C1	Capacitor chip, 1uF 6.3V +20% X5R 0402	1uF
C2	10nF 50V 10% X7R 0402	10nF
C7	4,7uF 6,3V X5R 0805 +20%	4u7F
C11	4,7uF 6,3V X5R 0805 +20%	4u7F
C12	Capacitor chip, 1uF 6.3V +20% X5R 0402	1uF
D1	Diode 40V 225mA, BAT54J	BAT54J
D2	Diode 40V 225mA, BAT54J	N/A
D3	Diode 40V 225mA, BAT54J	N/A
D4	LED Red	TLSU1008
D5	LED Red	TLSU1008
J1	50 Ohm male MCX connector PCB	CON/BNC_90DEG_PCB
J2	EDGE MOUNT SOCKET STRIP 40 PINS	2x20 edge
J3	2x5 pin-header, straight, 2.54mm	2x5P2.54
J4	1x2 pin-header, straight, pitch 2.54mm	1x2P2.54
J5	1x2 pin-header, straight, pitch 2.54mm	1x2P2.54
L1	75R,+25%@100MHz, 0R4@DC, 300mA	BLM15BB750
PCB1	Application board for IT530 rev B	PCB/AP530B00
Q1	NPN/PNP	BC847BPN
R1	Resistor chip, 1k 5% 0402 63mW	1k, 5%
R2	Resistor chip, 47R 0402 63mW 5%	47R, 5%
R3	Resistor chip, 47R 0402 63mW 5%	47R, 5%
R4	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R5	Resistor chip, 47R 0402 63mW 5%	47R, 5%
R6	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R7	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R8	Resistor chip, 1M 5% 0402 63mW	N/A
R9	Resistor chip, 470R 5% 0402 63mW	470R, 5%
R10	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R11	Resistor chip, 47R 0402 63mW 5%	47R, 5%
R12	Resistor chip, 47R 0402 63mW 5%	47R, 5%
R13	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R14	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R15	Resistor chip, 470R 5% 0402 63mW	470R, 5%
R16	Resistor chip, 10k 5% 0402 63mW	N/A
R17	Resistor chip, 10k 5% 0402 63mW	10k, 5%

R18	Resistor chip, 0R 0402	0R
R19	Resistor chip, 0R 0402	0R
R20	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R21	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R22	Resistor chip, 3.9k 5% 0402 63mW	3k9, 5%
R23	Resistor chip, 5k6 5% 0402 63mW	5k6, 5%
R24	Resistor chip, 47k 5% 0402 63mW	47k, 5%
R26	Resistor chip, 10k 5% 0402 63mW	10k, 5%
R27	Resistor chip, 10k 5% 0402 63mW	10k, 5%
R33	Resistor chip, 10k 5% 0402 63mW	N/A
S1	Jumper, Pitch, 2.54mm, Red colour	J4/P1-P2
S2	Label 13x16mm iTrax03s	STICKER13x16
S3	Switch, SMD PUSH BUTTON	SW
S4	Switch, on-off	SW JMP 2P54
S5	Switch, on-off	SW JMP 2P54
S6	Switch, on-off	SW JMP 2P54
S7	Switch, on-off	SW JMP 2P54
S8	Switch, on-off	SW JMP 2P54
S9	Jumper, Pitch, 2.54mm, Red colour	J5/P1-P2
U1	POWER SWITCH 0.1 ohm	N/A
U2	Logic buffer	NC7SZ125
U4	Schmit-Trigger inverter	NC7SZ14M5X

8.3 AP530 Circuit diagram

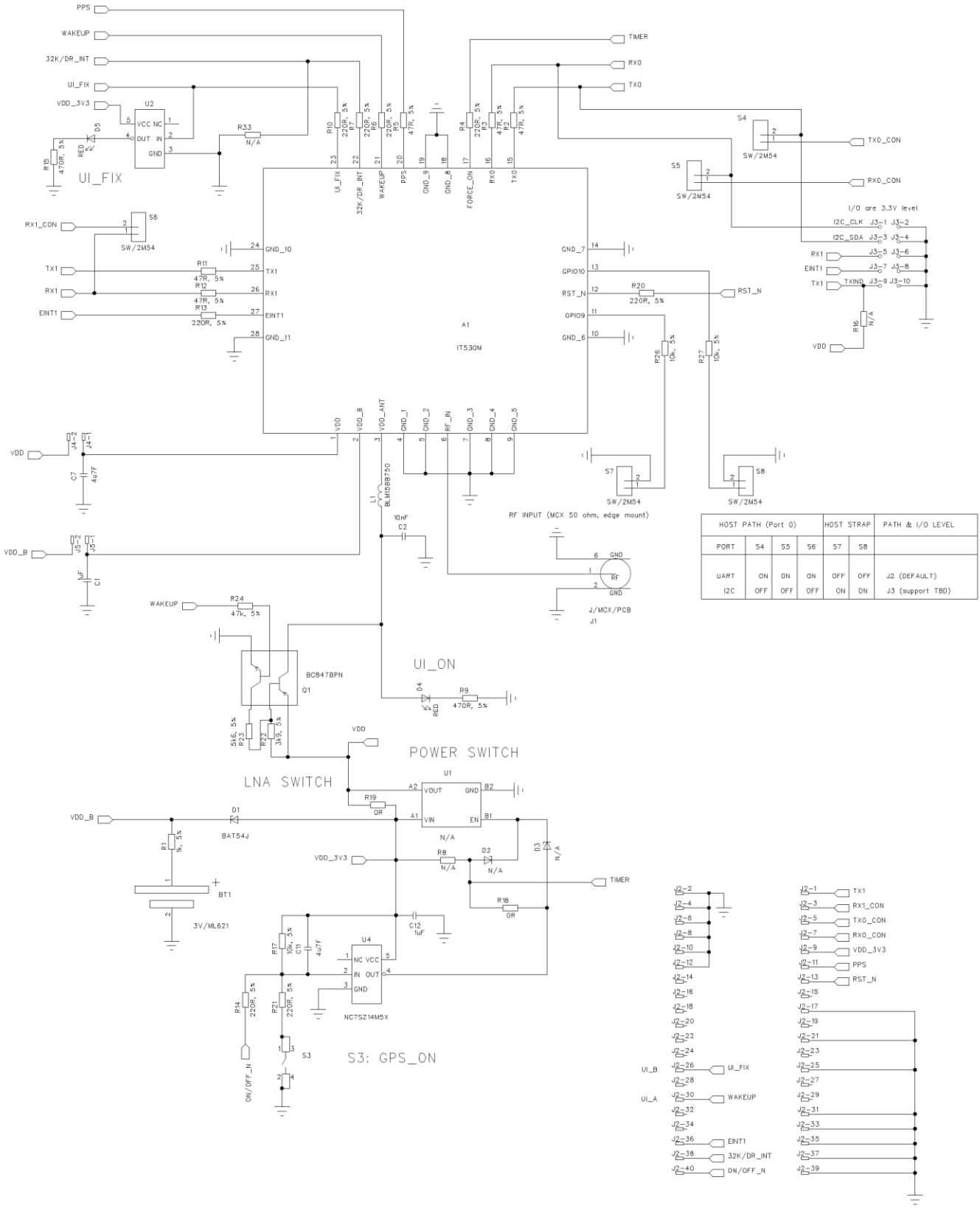

Figure 13 AP530 Circuit diagram

8.4 AP530 layout and assembly

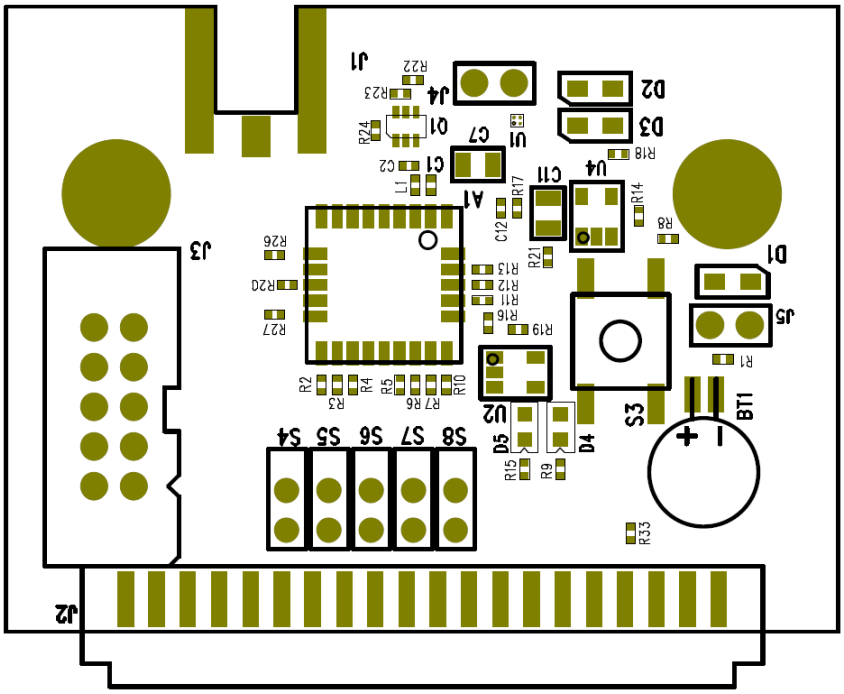

Figure 14 Assembly drawing, top side

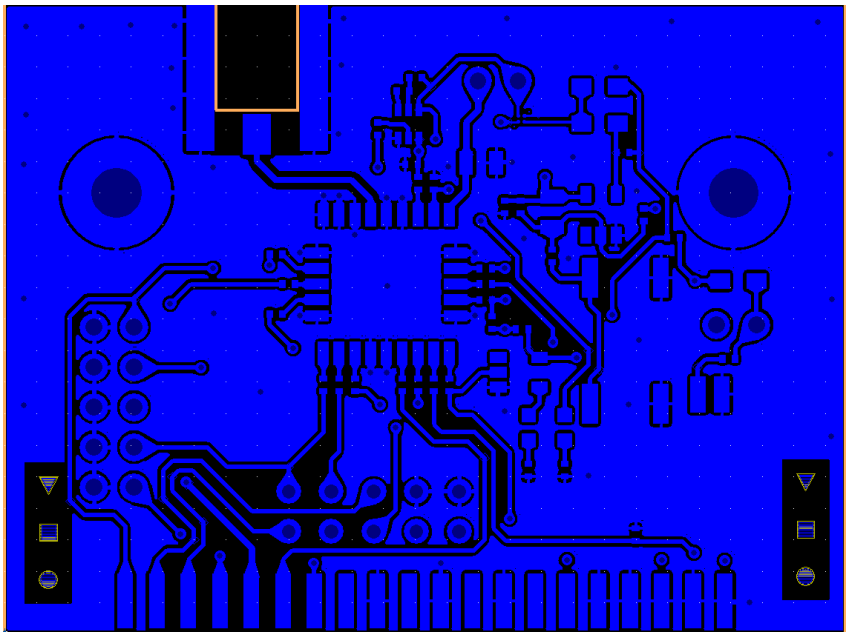

Figure 15 Layer 1, (top)

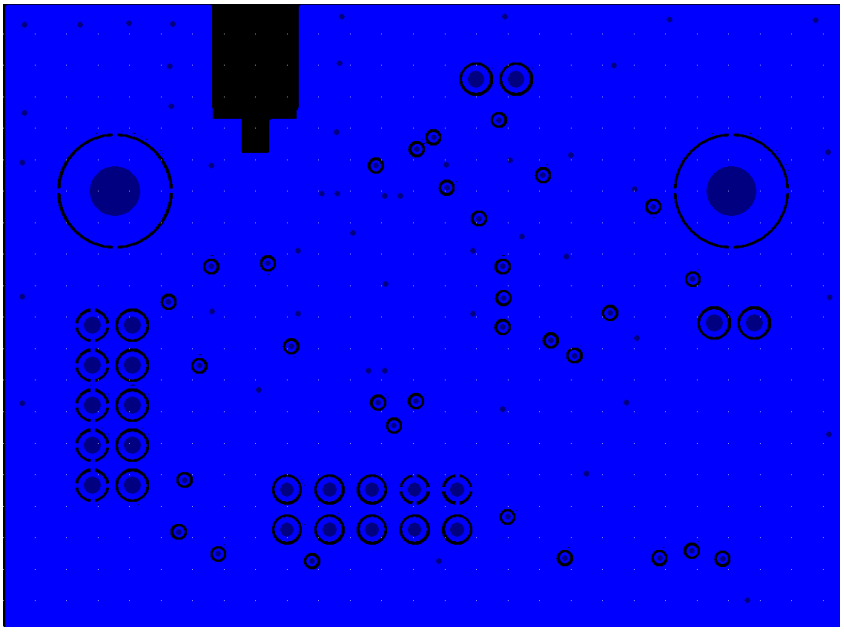

Figure 16 Layer 2

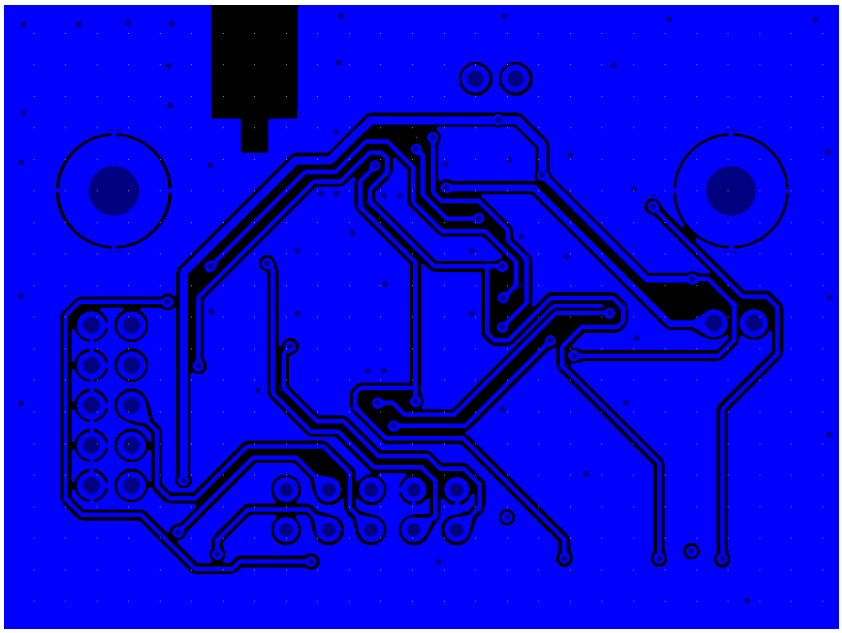

Figure 17 Layer 3

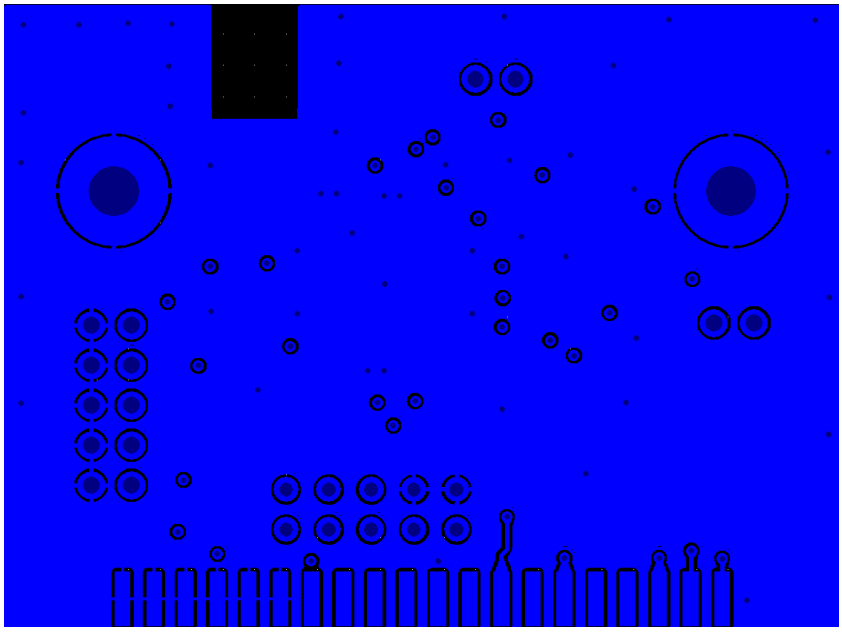

Figure 18 Layer 4 (bottom)

Contact Information

Fastrax Ltd

Street Address: Fastrax Ltd
Polaris Business Park
Itsehallintokuja 6
02600 Espoo

Finland

Tel: +358 (0)424 733 1

Fax: +358 (0)9 8240 9691

http://www.fastraxgps.com

E-mail:

Sales: sales@fastraxgps.com

Support: support@fastraxgps.com