nRF52832 Objective Product Specification v0.6

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1 Revision history

Date	Version	Description
June 2015	0.6	First release.

2 About this document

The nRF52832 is designed to maximize efficiency and performance of the SoC as a whole for ultra-low power wireless applications.

This Product Specification is organized into chapters based on the modules and peripherals that are available in this IC. These chapters include functional descriptions, register tables, and electrical specifications. This document includes a detailed description of each peripheral that can be used on the chip.

The peripherals are broken into separate sections that include the following information:

- A detailed functional description of the peripheral.
- Register configuration for the peripheral
- Electrical specifications tables providing the specified limits of the chip when tested under the conditions defined in the *Recommended operating conditions* on page 30

2.1 Peripheral naming and abbreviations

Every peripheral has a unique name or an abbreviation constructed by a single word, e.g. TIMER. This name is indicated in parentheses in the peripheral chapter heading. This name will be used in the ARM Cortex Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer to identify the peripheral.

The peripheral instance name, which is different from the peripheral name, is constructed using the peripheral name followed by a numbered postfix, starting with 0, for example, TIMER0. A postfix is normally only used if a peripheral can be instantiated more than once. The peripheral instance name is also used in the CMSIS to identify the peripheral instance.

2.2 Register tables

Individual registers are described using register tables.

These tables are built up of two sections. The first three colored rows describe the position and size of the different fields in the register. The following rows describe the fields in more detail.

2.2.1 Fields and values

The **Id (Field Id)** row specifies which bits that belong to the different fields in the register.

A blank space means that the field is reserved and that it is read as undefined and must be written as ‘0’ to secure forward compatibility. If a register is divided into more than one field, a unique field name is specified for each field in the **Field** column.

If a field has enumerated values, then every value will be identified with a unique value Id in the **Value Id** column. Single-bit bit-fields may however omit the “Value Id” when values can be substituted with a Boolean type enumerator range, for example, True, False; Disable, Enable, and On, Off, and so on.

The **Value** column can be populated in the following ways:

- Individual enumerated values, for example, 1, 3, 9.
- Range values, e.g. [0..4], that is, all values from and including 0 and 4.
- Implicit values. If no values are indicated in the **Value** column, all bit combinations are supported, or alternatively the field’s translation and limitations are described in the text instead.

If two or more fields are closely related, the value ID, value, and description may be omitted for all but the first field. Subsequent fields will indicate inheritance with “..”.

When a row in a register table contains the word **Deprecated** it means this is an attribute applied to a feature to indicate that it should not be used for new designs.

2.3 Registers

Table 1: Register Overview

Register	Offset	Description	
DUMMY	0x514	Example of a register controlling a dummy feature	
ANCIENT	0x518	Example of a deprecated register	Deprecated

2.3.1 DUMMY

Address offset: 0x514

Example of a register controlling a dummy feature

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id								D	D	D	D						C	C	C								B							A	A
Reset 0x00050002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**								**Description**																							
A	RW	ENABLE										Example of a field with several enumerated values																							
			Disabled	0								The example feature is disabled																							
			NormalMode	1								The example feature is enabled in normal mode																							
			ExtendedMode	2								The example feature is enabled along with extra functionality																							
B	RW	DONOTUSE										Example of a deprecated field																						Deprecated	
			Disabled	0								The override feature is disabled																							
			Enabled	1								The override feature is enabled																							
C	RW	RANGE										Example of a field with a valid range of values																							
			ValidRange	[2..7]								Example of allowed values for this field																							
D	RW	IMPLICIT										Example of a field with implicit values																							

2.3.2 ANCIENT (Deprecated)

Address offset: 0x518

Example of a deprecated register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**								**Description**																							
A	RW	PTR										Dummy field																							

3 Block diagram

This block diagram illustrates the overall system. Arrows with white heads indicate signals that share physical pins with other signals.

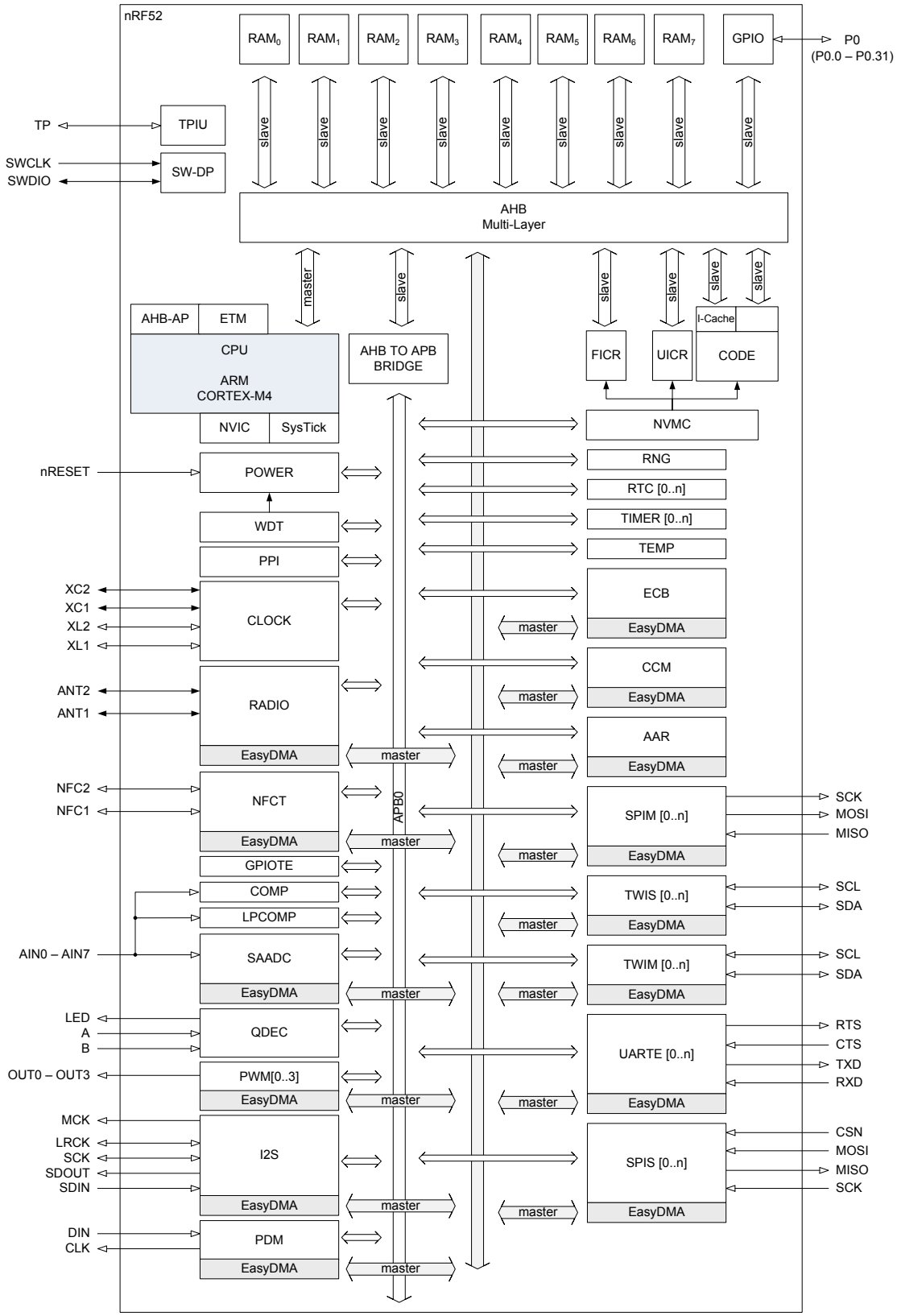

Figure 1: Block diagram

4 Pin assignments

Here we cover the pin assignments on each variant of the chip.

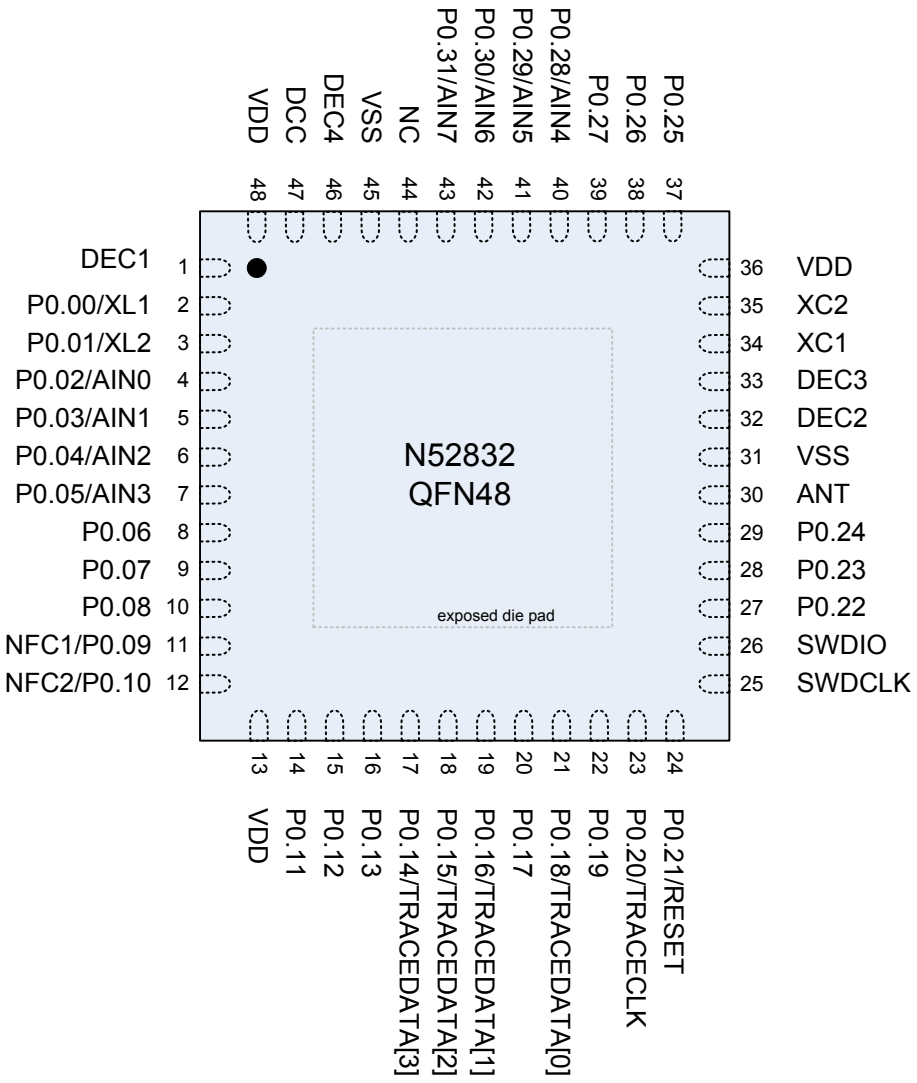

Figure 2: QFN48 Pin assignments, top view

Table 2: Pin assignments

Pin	Name		Description
Left Side of chip			
1	DEC1	Power	0V9 regulator digital supply decoupling.
2	P0.00	Digital I/O	General purpose I/O pin.
	XL1	Analog input	Connection for 32.768 kHz crystal (LFXO).
3	P0.01	Digital I/O	General purpose I/O pin.
	XL2	Analog input	Connection for 32.768 kHz crystal (LFXO).
4	P0.02	Digital I/O	General purpose I/O pin.
	AIN0	Analog input	SAADC/COMP/LPCOMP input.
5	P0.03	Digital I/O	General purpose I/O pin.
	AIN1	Analog input	SAADC/COMP/LPCOMP input.
6	P0.04	Digital I/O	General purpose I/O pin.
	AIN2	Analog input	SAADC/COMP/LPCOMP input.
7	P0.05	Digital I/O	General purpose I/O pin.
	AIN3	Analog input	SAADC/COMP/LPCOMP input.
8	P0.06	Digital I/O	General purpose I/O pin.

Pin	Name		Description
9	P0.07	Digital I/O	General purpose I/O pin.
10	P0.08	Digital I/O	General purpose I/O pin.
11	NFC1	NFC input	NFC antenna connection.
	P0.09	Digital I/O	General purpose I/O pin[1].
12	NFC2	NFC input	NFC antenna connection.
	P0.10	Digital I/O	General purpose I/O pin[1].
Bottom side of chip			
13	VDD	Power	Power-supply pin.
14	P0.11	Digital I/O	General purpose I/O pin.
15	P0.12	Digital I/O	General purpose I/O pin.
16	P0.13	Digital I/O	General purpose I/O pin.
17	P0.14	Digital I/O	General purpose I/O pin.
	TRACEDATA[3]		Trace port output.
18	P0.15	Digital I/O	General purpose I/O pin.
	TRACEDATA[2]		Trace port output.
19	P0.16	Digital I/O	General purpose I/O pin.
	TRACEDATA[1]		Trace port output.
20	P0.17	Digital I/O	General purpose I/O pin.
21	P0.18	Digital I/O	General purpose I/O pin.
	TRACEDATA[0]		Trace port output.
22	P0.19	Digital I/O	General purpose I/O pin.
23	P0.20	Digital I/O	General purpose I/O pin.
	TRACECLK		Trace port clock output.
24	P0.21	Digital I/O	General purpose I/O pin.
	RESET		Configurable as system RESET pin.
Right Side of chip			
25	SWDCLK	Digital input	Serial Wire Debug clock input for debug and programming.
26	SWDIO	Digital I/O	Serial Wire Debug I/O for debug and programming.
27	P0.22	Digital I/O	General purpose I/O pin[2].
28	P0.23	Digital I/O	General purpose I/O pin[2].
29	P0.24	Digital I/O	General purpose I/O pin[2].
30	ANT	RF	Single-ended radio antenna connection.
31	VSS	Power	Ground pin (Radio supply).
32	DEC2	Power	1V3 regulator supply decoupling (Radio supply).
33	DEC3	Power	Power supply decoupling.
34	XC1	Analog input	Connection for 32 MHz crystal.
35	XC2	Analog input	Connection for 32 MHz crystal.
36	VDD	Power	Power-supply pin.
Top side of chip			
37	P0.25	Digital I/O	General purpose I/O pin[2].
38	P0.26	Digital I/O	General purpose I/O pin[2].
39	P0.27	Digital I/O	General purpose I/O pin[2].
40	P0.28	Digital I/O	General purpose I/O pin[2].
	AIN4	Analog input	SAADC/COMP/LPCOMP input.
41	P0.29	Digital I/O	General purpose I/O pin[2].
	AIN5	Analog input	SAADC/COMP/LPCOMP input.
42	P0.30	Digital I/O	General purpose I/O pin[2].
	AIN6	Analog input	SAADC/COMP/LPCOMP input.
43	P0.31	Digital I/O	General purpose I/O pin[2].
	AIN7	Analog input	SAADC/COMP/LPCOMP input.
44	NC		No connect pin. Leave unconnected.
45	VSS	Power	Ground pin.
46	DEC4	Power	1V3 regulator supply decoupling. Input from DC/DC converter. Output from 1.3 V LDO.
47	DCC	Power	DC/DC converter output pin.
48	VDD	Power	Power-supply pin.
Bottom of chip			
Die pad	VSS	Power	Ground pad. Exposed die pad must be connected to ground (VSS) for proper device operation.

[1] See *NFC antenna pins* on page 112 for more information.
[2] See *GPIO located near the radio* on page 112 for more information.

5 Absolute maximum ratings

Maximum ratings are the extreme limits to which nRF52832 can be exposed without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.

Table 3: Absolute maximum ratings

	Note	Min.	Max.	Unit
Supply voltages				
VDD		-0.3	+3.9	V
VSS			0	V
I/O pin voltage				
$V_{I/O}$		-0.3	3.9 V	V
NFC antenna pin current				
$I_{NFC1/2}$			80	mA
Radio				
RF Input Level			10	dBm
Environmental (QFN package)				
Storage temperature		-40	+125	°C
MSL	Moisture Sensitivity Level		2	
ESD HBM	Human Body Model		4	kV
ESD CDM_{QF}	Charged Device Model (QFN48, 6x6 mm package)		750	V
Flash Memory				
Endurance		10 000		Write/erase cycles
Retention		10 years at 40°C		
Number of times a 512 byte block can be written between erase cycles	128 bit writes or 32 bit writes		190	times

6 Recommended operating conditions

The operating conditions are the physical parameters that nRF52832 can operate within.

The nRF52832 operating conditions are defined below in *Table 4: Recommended operating conditions* on page 30.

Table 4: Recommended operating conditions

Symbol	Parameter	Notes	Min.	Nom.	Max.	Units
VDD	Supply voltage, independent of DCDC enable		1.7	3.0	3.6	V
t_{R_VDD}	Supply rise time (0 V to 1.7 V)	[3]			60	ms
TA	Operating temperature		-40	25	85	°C

The on-chip power-on reset circuitry may not function properly for rise times outside the specified interval.

[3] The on-chip power-on reset circuitry may not function properly for rise times outside the specified interval.

7 Mechanical specifications

This chapter covers the mechanical specifications for nRF52832 QFN48 package.

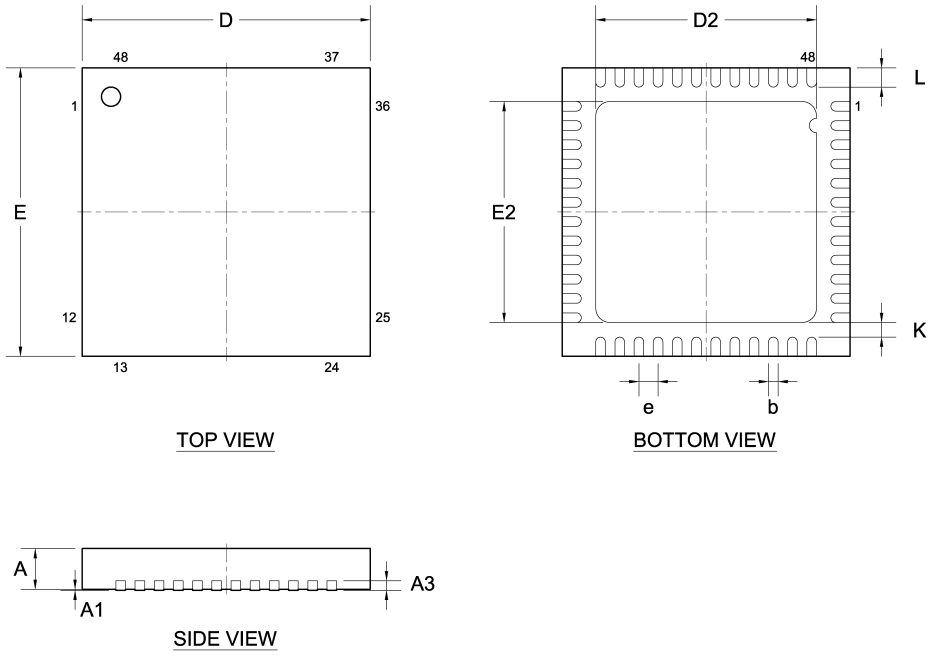

Figure 3: QFN48 6 x 6 mm package

Table 5: QFN48 dimensions in millimeters

Package	A	A1	A3	b	D, E	D2, E2	e	K	L	
	0.80	0.00		0.15		4.50		0.20	0.35	**Min.**
QFN48 (6x6)	0.85	0.02	0.2	0.20	6.0	4.60	0.4		0.40	**Nom.**
	0.90	0.05		0.25		4.70			0.45	**Max.**

8 CPU

The ARM® Cortex™-M4 CPU has a 32-bit instruction set (***Thumb-2***® technology) that implements a superset of 16 and 32-bit instructions to maximize code density and performance.

Key features that enable energy efficient arithmetic and high performance signal processing are:

- Digital signal processing (DSP) instructions
- Single-cycle multiply and accumulate (MAC) instructions
- Hardware divide
- 8 and 16-bit Single instruction multiple data (SIMD) instructions
- Single-precision Floating-point unit (FPU)

The ARM Cortex Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer for the ARM® Cortex™ processor series is implemented and available for M4 CPU.

Real time execution is highly deterministic in thread mode, to and from sleep modes, and when handling events at configurable priority levels via the Nested Vectored Interrupt Controller (NVIC).

Executing code from flash will have a wait state penalty on the nRF52 Series. An instruction cache can be enabled to minimize flash wait states when fetching instructions. For more information on cache, see *Cache* on page 38. The section *Electrical Specification* on page 32 shows CPU performance parameters including wait states in different modes, CPU current and efficiency, and processing power and efficiency based on the CoreMark™ benchmark.

8.1 CPU and support module configuration

The ARM® Cortex™-M4 has a number of CPU options and support modules implemented on the device.

Option / Module	Description	Implemented
Core options		
NVIC	Nested vector interrupt controller	37 vectors
PRIORITIES	Priority bits	3
WIC	Wakeup interrupt controller	NO
Endianness	Memory system endianness	Little Endian
Bit Banding	Bit banded memory	NO
DWT	Data watch point and trace	YES
SysTick	System tick timer	YES
Modules		
MPU	Memory protection unit	YES
FPU	Floating point unit	YES
DAP	Debug access port	YES
ETM	Instruction trace	YES
ITM	Instrumentation trace	YES
TPIU	Trace port	YES
ETB	Embedded trace buffer	NO
FPB	Breakpoint unit	YES
HTM	AHB trace macrocell	NO

8.2 Electrical Specification

8.2.1 CPU performance, HCLK = 64 MHz

Current and efficiency data is taken when in System ON and the CPU is executing the CoreMark™ benchmark. It includes power regulator and clock base currents. All other blocks are IDLE.

Symbol	Description	Min.	Typ.	Max.	Units
$W_{64FLASH}$	CPU wait states, running from flash, cache disabled, 64 MHz			2	
$W_{64FLASHCACHE}$	CPU wait states, running from flash, cache enabled, 64 MHz			3	
W_{64RAM}	CPU wait states, running from RAM, 64 MHz			0	
$I_{DD64FLASH}$	CPU current, running from flash, 64 MHz		5		mA
$I_{DD64FLASHDCDC}$	CPU current, running from flash, 64 MHz, DCDC 3V		2.4		mA

Symbol	Description	Min.	Typ.	Max.	Units
$I_{DD64RAM}$	CPU current, running from RAM, 64 MHz		4.8		mA
$I_{DD64RAMDCDC}$	CPU current, running from RAM, 64 MHz, DCDC 3V		2.2		mA
$I_{DD64FLASH/MHz}$	CPU efficiency, running from flash, 64 MHz		78		µA/ MHz
$I_{DD64FLASHDCDC/MHz}$	CPU efficiency, running from flash, 64 MHz, DCDC 3V		38		µA/ MHz
$CM_{64FLASH}$	CoreMark[4], running from flash, cache enabled, 64 MHz		215		
$CM_{64FLASH/MHz}$	CoreMark per MHz, running from flash, cache enabled, 64 MHz		3.36		
$CM_{64FLASH/mA}$	CoreMark per mA, running from flash, cache enabled, 64 MHz, DCDC 3V		89		

[4] Using IAR v6.50 with flags --endian=little --cpu=Cortex-M4 -e --fpu=None -Ohs --use_c++_inline --no_size_constraints

9 Memory

There are two types of memory: volatile memory (VM) and non-volatile memory (NVM).

Volatile memory is a type of memory that will lose its contents when the chip loses power. This memory type can be read/written an unlimited number of times by the CPU.

Non-volatile memory is a type of memory that can retain stored information even when the chip loses power. This memory type can be read an unlimited number of times by the CPU, but have restrictions on the number of times it can be written and erased[5] and also on how it can be written. Writing to non-volatile memory is managed by the Non Volatile Memory Controller (NVMC).

All memory and registers are found in the same address space as shown in the Device Memory Map, see *Figure 4: Memory map* on page 34.

nRF52832 uses flash based NVM in the code, FICR, and UICR regions.

The VM is SRAM. The physical RAM is mapped to both Code RAM and Data RAM by default to allow RAM regions to be defined in a project as data or code. The Cortex™ M4 can access Instructions and Data for program execution at full speed from Code RAM. Linker tools must be configured to locate code that should run from RAM into Code RAM, and also to re-define the Data RAM region to exclude the RAM used as Code RAM.

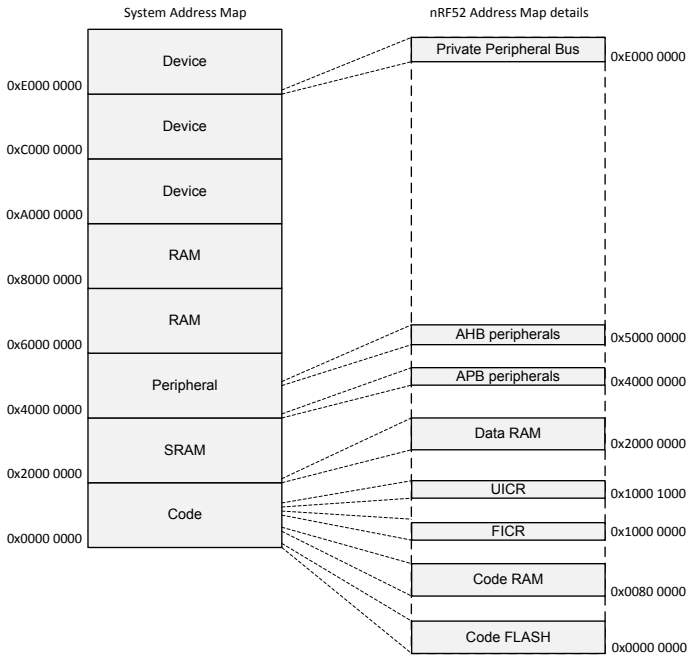

Figure 4: Memory map

9.1 Memory categories

There are three main categories of memory:

- Code memory
- Random Access Memory (RAM)
- Peripheral registers (PER)

[5] See *Table 3: Absolute maximum ratings* on page 29 and *Writing to the NVM* on page 38for more information

In addition, there is one information block (FICR) containing read only parameters describing configuration details of the device and another information block (UICR) that can be configured by the user.

9.1.1 Code memory

The code memory is normally used for storing the program executed by the CPU, but can also be used for storing data constants that are retained when the chip loses power.

9.1.2 Random access memory (RAM)

All RAM is volatile and always loses its content when the chip loses power.

The system includes the following RAM (Random Access Memory) regions:

- Data RAM
- Code RAM

The Data RAM region is located in the SRAM segment of the System Address Map. It is possible to execute code from this region.

The Code RAM region is located in the Code segment of the System Address Map. It is possible to execute code from this region.

The same physical RAM is mapped to both the Data RAM region and the Code RAM region, see *Figure 4: Memory map* on page 34. It is up to the application to partition and use the RAM within these regions so that one does not corrupt the other.

The RAM interface is divided into multiple RAM AHB (AMBA High-performance Bus) slaves.

Each RAM AHB slave is connected to two 4 kbyte RAM sections, see Section 0 and Section 1 in *Figure 5: RAM mapping* on page 35.

Each of the RAM sections have separate power control for System ON and System OFF mode operation, this is configured via POWER->RAM registers.

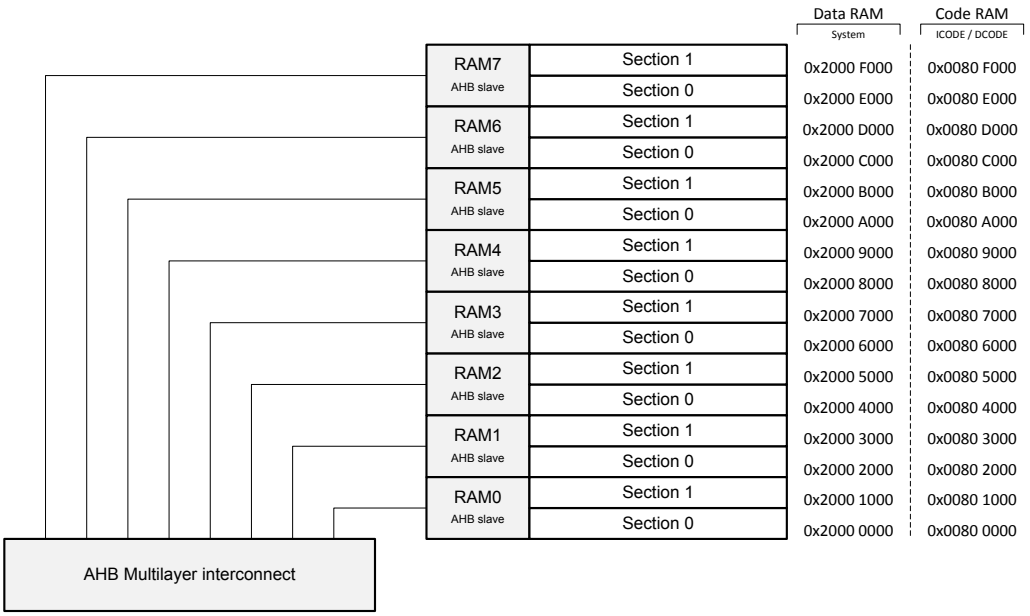

Figure 5: RAM mapping

Table 6: Memory size and organisation

Total flash size	Page Size	No. of Pages	Pre-fetch
512 kB	4 kB	128	128 bits

Table 7: Memory size and organisation

Total RAM Size	Block ID	Size
64 kB	0:15	4 kB

9.1.3 Peripheral registers

The peripheral registers are registers used for interfacing to peripheral units such as timers, the radio, the ADC, and so on.

Most peripherals feature an ENABLE register. Unless otherwise specified in the relevant chapter, the peripheral registers (in particular the PSEL registers) must be configured prior to enabling the peripheral.

When switching from one peripheral to another sharing the same base address (see **Instantiation** below to identify the peripherals that share base addresses), all such peripherals must be disabled before new settings are configured and another peripheral is enabled.

Note that the peripheral must be enabled before tasks and events can be used.

9.2 Non-volatile memory controller (NVMC)

The non-volatile memory controller manages programming and erasing of all flash memory.

See Chapter *Non-volatile memory controller (NVMC)* on page 38 for more detailed information.

9.3 Instantiation

Table 8: Instantiation table

ID	Base Address	Peripheral	Instance	Description	
0	0x40000000	POWER	POWER	Power Control	
0	0x40000000	BPROT	BPROT	Block Protect	
0	0x40000000	CLOCK	CLOCK	Clock control	
1	0x40001000	RADIO	RADIO	2.4 GHz radio	
2	0x40002000	UART	UART0	Universal Asynchronous Receiver/Transmitter	Deprecated
2	0x40002000	UARTE	UARTE0	Universal Asynchronous Receiver/Transmitter with EasyDMA	
3	0x40003000	SPIM	SPIM0	SPI master 0	
3	0x40003000	TWIM	TWIM0	Two-wire interface master 0	
3	0x40003000	SPIS	SPIS0	SPI slave 0.	
3	0x40003000	TWI	TWI0	Two-wire interface master 0	Deprecated
3	0x40003000	SPI	SPI0	SPI master 0	Deprecated
3	0x40003000	TWIS	TWIS0	Two-wire interface slave 0	
4	0x40004000	TWIS	TWIS1	Two-wire interface slave 1	
4	0x40004000	SPI	SPI1	SPI master 1	Deprecated
4	0x40004000	SPIS	SPIS1	SPI slave 1	
4	0x40004000	SPIM	SPIM1	SPI master 1	
4	0x40004000	TWI	TWI1	Two-wire interface master 1	Deprecated
4	0x40004000	TWIM	TWIM1	Two-wire interface master 1	
5	0x40005000	NFCT	NFCT	Near Field Communication Tag	
6	0x40006000	GPIOTE	GPIOTE	GPIO tasks and events	
7	0x40007000	SAADC	SAADC	Analog to digital converter	
8	0x40008000	TIMER	TIMER0	Timer 0	
9	0x40009000	TIMER	TIMER1	Timer 1	
10	0x4000A000	TIMER	TIMER2	Timer 2	
11	0x4000B000	RTC	RTC0	Real time counter 0	
12	0x4000C000	TEMP	TEMP	Temperature Sensor	
13	0x4000D000	RNG	RNG	Random Number Generator	
14	0x4000E000	ECB	ECB	AES ECB Mode Encryption	
15	0x4000F000	CCM	CCM	AES CCM Mode Encryption	
15	0x4000F000	AAR	AAR	Accelerated Address Resolver	

ID	Base Address	Peripheral	Instance	Description	
16	0x40010000	WDT	WDT	Watchdog Timer	
17	0x40011000	RTC	RTC1	Real time counter 1	
18	0x40012000	QDEC	QDEC	Quadrature decoder	
19	0x40013000	LPCOMP	LPCOMP	Low power comparator	
19	0x40013000	COMP	COMP	General Purpose Comparator	
20	0x40014000	EGU	EGU0	Event Generator Unit 0	
20	0x40014000	SWI	SWI0	Software interrupt 0	
21	0x40015000	SWI	SWI1	Software interrupt 1	
21	0x40015000	EGU	EGU1	Event Generator Unit 1	
22	0x40016000	SWI	SWI2	Software interrupt 2	
22	0x40016000	EGU	EGU2	Event Generator Unit 2	
23	0x40017000	EGU	EGU3	Event Generator Unit 3	
23	0x40017000	SWI	SWI3	Software interrupt 3	
24	0x40018000	EGU	EGU4	Event Generator Unit 4	
24	0x40018000	SWI	SWI4	Software interrupt 4	
25	0x40019000	EGU	EGU5	Event Generator Unit 5	
25	0x40019000	SWI	SWI5	Software interrupt 5	
26	0x4001A000	TIMER	TIMER3	Timer 3	
27	0x4001B000	TIMER	TIMER4	Timer 4	
28	0x4001C000	PWM	PWM0	Pulse Width Modulation Unit 0	
29	0x4001D000	PDM	PDM	Pulse Density Modulation (Digital Microphone) Interface	
30	0x4001E000	NVMC	NVMC	Non Volatile Memory Controller	
31	0x4001F000	PPI	PPI	PPI controller	
32	0x40020000	MWU	MWU	Memory Watch Unit	
33	0x40021000	PWM	PWM1	Pulse Width Modulation Unit 1	
34	0x40022000	PWM	PWM2	Pulse Width Modulation Unit 2	
35	0x40023000	SPI	SPI2	SPI master 2.	Deprecated
35	0x40023000	SPIS	SPIS2	SPI slave 2.	
35	0x40023000	SPIM	SPIM2	SPI master 2.	
36	0x40024000	RTC	RTC2	Real time counter 2.	
37	0x40025000	I2S	I2S	Inter-IC Sound interface	
N/A	0x10000000	FICR	FICR	Factory Information Configuration	
N/A	0x10001000	UICR	UICR	User Information Configuration	
N/A	0x50000000	GPIO	P0	General purpose input and output	
N/A	0x50000000	GPIO	GPIO	General purpose input and output	Deprecated

10 Non-volatile memory controller (NVMC)

The Non-volatile memory controller (NVMC) is used for writing and erasing Non-volatile memory (NVM).

Before a write can be performed the NVM must be enabled for writing in CONFIG.WEN. Similarly, before an erase can be performed the NVM must be enabled for erasing in CONFIG.EEN. The user must make sure that writing and erasing are not enabled at the same time. Failing to do so may result in unpredictable behavior.

10.1 Writing to the NVM

When writing is enabled, the NVM is written by writing a word to a word-aligned address in the CODE or UICR. The NVMC is only able to write bits in the NVM that are erased, that is, set to '1'.

The same block address in the NVM can only be written n_{WRITE} number of times before an erase must be performed using PAGEERASE , ERASEUICR, or ERASEALL.

The time it takes to write a word to the NVM is specified by t_{WRITE} . The CPU is halted while the NVMC is writing to the NVM.

Only word-aligned writes are allowed. Byte or half-word-aligned writes will result in a hard fault.

10.2 Writing to user information configuration registers (UICR)

User information configuration registers (UICR) are written as ordinary non-volatile memory. After the UICR has been written, the new UICR configuration will only take effect after a reset.

10.3 Erase all

When erase is enabled, the whole CODE and UICR can be erased in one operation by using the ERASEALL register. ERASEALL will not erase the factory information configuration registers (FICR).

The time it takes to perform an ERASEALL command is specified by $t_{ERASEALL}$. The CPU is halted while the NVMC performs the erase operation.

10.4 Erasing a page in code memory

When erase is enabled, the NVM can be erased page by page using the ERASEPAGE register.

After erasing an NVM page all bits in the page are set to '1'. The time it takes to erase a page is specified by $t_{PAGEERASE}$. The CPU is halted while the NVMC performs the erase operation.

10.5 Cache

An instruction cache can be enabled for the Code FLASH segment of memory.

See the Memory map in *Memory* on page 34 for the location of Code FLASH.

A cache hit is an instruction fetch from the cache, and it has a 0 wait-state delay. The number of wait-states for a cache miss, where the instruction is not available in the cache and needs to be fetched from FLASH, depends on the processor frequency and is shown in the *Flash wait states* table.

Enabling the cache can increase CPU performance and reduce power consumption by reducing the number of wait cycles and the number of flash accesses. This will depend on the cache hit rate. Cache will use some current when enabled. If the reduction in average current due to reduced flash accesses is larger than the cache power requirement, the average current to execute the program code will reduce.

When disabled, the cache does not use current and does not retain its content.

It is possible to enable cache profiling to analyze the performance of the cache for your program using the *ICACHECNF* register. When profiling is enabled, the *IHIT* and *IMISS* registers are incremented for every instruction cache hit or miss respectively. The hit and miss profiling registers do not wrap around after reaching the maximum value. If the maximum value is reached, consider profiling for a shorter duration to get correct numbers.

10.6 Registers

Table 9: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4001E000	NVMC	NVMC	Non Volatile Memory Controller	

Table 10: Register Overview

Register	Offset	Description	
READY	0x400	Ready flag	
CONFIG	0x504	Configuration register	
ERASEPAGE	0x508	Register for erasing a page in Code area	
ERASEPCR1	0x508	Register for erasing a page in Code area. Equivalent to ERASEPAGE.	Deprecated
ERASEALL	0x50C	Register for erasing all non-volatile user memory	
ERASEPCR0	0x510	Register for erasing a page in Code area. Equivalent to ERASEPAGE.	Deprecated
ERASEUICR	0x514	Register for erasing User Information Configuration Registers	
ICACHECNF	0x540	I-Code cache configuration register.	
IHIT	0x548	I-Code cache hit counter.	
IMISS	0x54C	I-Code cache miss counter.	

10.6.1 READY

Address offset: 0x400

Ready flag

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	READY																																	
			Busy	0																															
			Ready	1																															

10.6.2 CONFIG

Address offset: 0x504

Configuration register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	WEN																																	
			Ren	0																															
			Wen	1																															
			Een	2																															

10.6.3 ERASEPAGE

Address offset: 0x508

Register for erasing a page in Code area

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	ERASEPAGE																																	

Register for starting erase of a page in Code area

The value is the address to the page to be erased. (Addresses of first word in page). Note that code erase has to be enabled by CONFIG.EEN before the page can be erased. See product specification for information about the total code size of the device you are using. Attempts to erase pages that are outside the code area may result in undesirable behaviour, e.g. the wrong page may be erased.

10.6.4 ERASEPCR1 (Deprecated)

Address offset: 0x508

Register for erasing a page in Code area. Equivalent to ERASEPAGE.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	ERASEPCR1																																	

Register for erasing a page in Code area. Equivalent to ERASEPAGE.

10.6.5 ERASEALL

Address offset: 0x50C

Register for erasing all non-volatile user memory

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	ERASEALL																																	
			NoOperation	0																															
			Erase	1																															

Erase all non-volatile memory including UICR registers. Note that code erase has to be enabled by CONFIG.EEN before the UICR can be erased.

No operation

Start chip erase

10.6.6 ERASEPCR0 (Deprecated)

Address offset: 0x510

Register for erasing a page in Code area. Equivalent to ERASEPAGE.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	ERASEPCR0																																	

Register for starting erase of a page in Code area. Equivalent to ERASEPAGE.

10.6.7 ERASEUICR

Address offset: 0x514

Register for erasing User Information Configuration Registers

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	ERASEUICR																																	
			NoOperation	0																															
			Erase	1																															

10.6.8 ICACHECNF

Address offset: 0x540

I-Code cache configuration register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																											B								A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	CACHEEN																																	
			Disabled	0																															
			Enabled	1																															
B	RW	CACHEPROFEN																																	
			Disabled	0																															
			Enabled	1																															

10.6.9 IHIT

Address offset: 0x548

I-Code cache hit counter.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	HITS																																	

10.6.10 IMISS

Address offset: 0x54C

I-Code cache miss counter.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	MISSES																																	

10.7 Electrical Specification

10.7.1 Flash programming

Symbol	Description	Min.	Typ.	Max.	Units
n_{WRITE}	Amount of writes between erase	181			

Symbol	Description	Min.	Typ.	Max.	Units
$n_{ENDURANCE}$	Write/erase cycles	10 000			
$n_{RETENTION}$	Retention at 40 degree Celsius	10			Years
t_{WRITE}	Time to write one word	67.5		338	µs
$t_{PAGEERASE}$	Time to erase one page	2.05		89.7	ms
$t_{ERASEALL}$	Time to erase all flash	6.72		295.3	ms

10.7.2 Cache size

Symbol	Description	Min.	Typ.	Max.	Units
$Size_{ICODE}$	I-Code cache size		2048		Bytes

11 Block protection (BPROT)

The mechanism for protecting non-volatile memory can be used to prevent erroneous application code from erasing or writing to protected blocks.

Non-volatile memory can be protected from erases and writes depending on the settings in the CONFIG registers. One bit in a CONFIG register represents one protected block of 4 kB. There are four CONFIG registers of 32 bits, which means there are 128 protectable blocks in total.

> **Important:** If an erase or write to a protected block is detected, the CPU will hard fault. If an ERASEALL operation is attempted from the CPU while any block is protected it will be blocked and the CPU will hard fault.

On reset, all the protection bits are cleared. To ensure safe operation, the first task after reset must be to set the protection bits. The only way of clearing protection bits is by resetting the device from any reset source.

The protection mechanism is turned off when in debug mode (a debugger is connected) and the DISABLEINDEBUG register is set to disable.

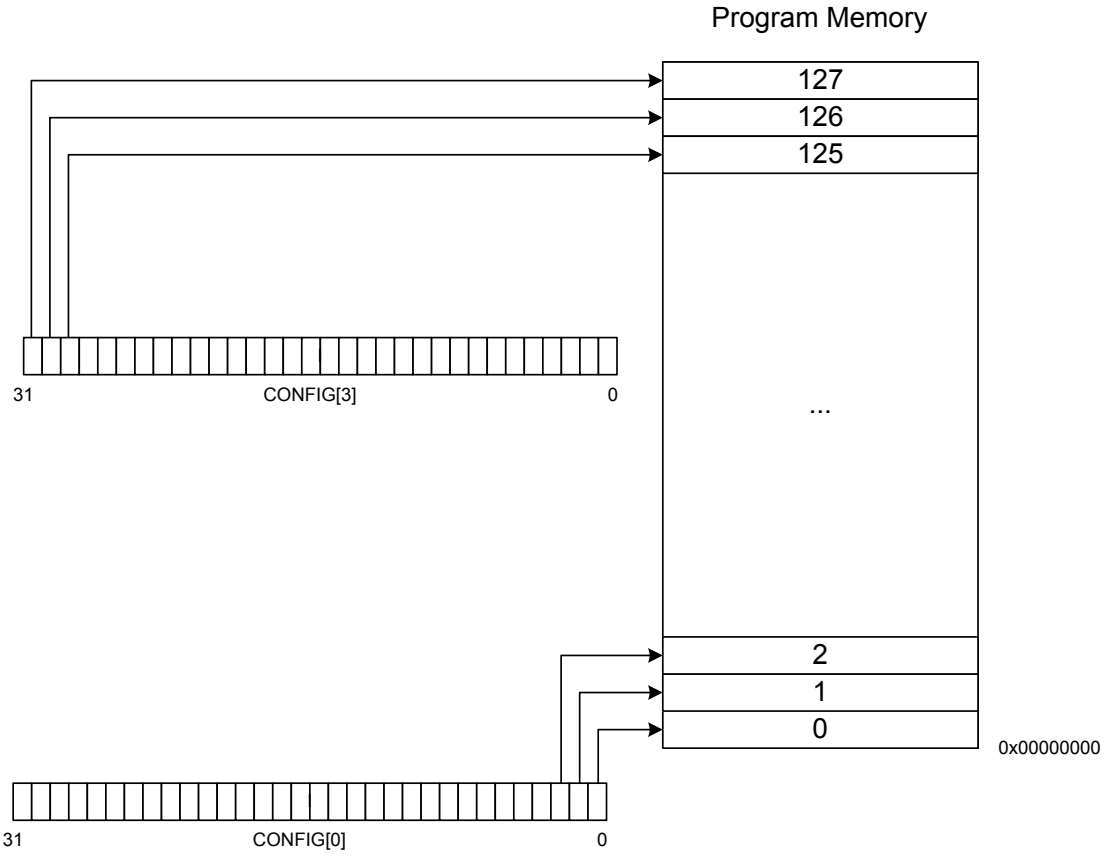

Figure 6: Protected regions of program memory

11.1 Registers

Table 11: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40000000	BPROT	BPROT	Block Protect	

Table 12: Register Overview

Register	Offset	Description
CONFIG0	0x600	Block protect configuration register 0
CONFIG1	0x604	Block protect configuration register 1
DISABLEINDEBUG	0x608	Disable protection mechanism in debug mode
	0x60C	Reserved
CONFIG2	0x610	Block protect configuration register 2
CONFIG3	0x614	Block protect configuration register 3

11.1.1 CONFIG0

Address offset: 0x600

Block protect configuration register 0

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	REGION0			Enable protection for region 0. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
B	RW	REGION1			Enable protection for region 1. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
C	RW	REGION2			Enable protection for region 2. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
D	RW	REGION3			Enable protection for region 3. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
E	RW	REGION4			Enable protection for region 4. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
F	RW	REGION5			Enable protection for region 5. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
G	RW	REGION6			Enable protection for region 6. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
H	RW	REGION7			Enable protection for region 7. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
I	RW	REGION8			Enable protection for region 8. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
J	RW	REGION9			Enable protection for region 9. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
K	RW	REGION10			Enable protection for region 10. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
L	RW	REGION11			Enable protection for region 11. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
M	RW	REGION12			Enable protection for region 12. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
N	RW	REGION13			Enable protection for region 13. Write '0' has no effect.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
O	RW	REGION14			Enable protection for region 14. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
P	RW	REGION15			Enable protection for region 15. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
Q	RW	REGION16			Enable protection for region 16. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
R	RW	REGION17			Enable protection for region 17. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
S	RW	REGION18			Enable protection for region 18. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
T	RW	REGION19			Enable protection for region 19. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
U	RW	REGION20			Enable protection for region 20. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
V	RW	REGION21			Enable protection for region 21. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
W	RW	REGION22			Enable protection for region 22. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
X	RW	REGION23			Enable protection for region 23. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
Y	RW	REGION24			Enable protection for region 24. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
Z	RW	REGION25			Enable protection for region 25. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
a	RW	REGION26			Enable protection for region 26. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
b	RW	REGION27			Enable protection for region 27. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
c	RW	REGION28			Enable protection for region 28. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
d	RW	REGION29			Enable protection for region 29. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
e	RW	REGION30			Enable protection for region 30. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
f	RW	REGION31			Enable protection for region 31. Write '0' has no effect.
			Disabled	0	Protection disabled

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Enabled	1																															
				Protection enable																															

11.1.2 CONFIG1

Address offset: 0x604

Block protect configuration register 1

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	REGION32																																	
			Disabled	0																															
			Enabled	1																															
B	RW	REGION33																																	
			Disabled	0																															
			Enabled	1																															
C	RW	REGION34																																	
			Disabled	0																															
			Enabled	1																															
D	RW	REGION35																																	
			Disabled	0																															
			Enabled	1																															
E	RW	REGION36																																	
			Disabled	0																															
			Enabled	1																															
F	RW	REGION37																																	
			Disabled	0																															
			Enabled	1																															
G	RW	REGION38																																	
			Disabled	0																															
			Enabled	1																															
H	RW	REGION39																																	
			Disabled	0																															
			Enabled	1																															
I	RW	REGION40																																	
			Disabled	0																															
			Enabled	1																															
J	RW	REGION41																																	
			Disabled	0																															
			Enabled	1																															
K	RW	REGION42																																	
			Disabled	0																															
			Enabled	1																															
L	RW	REGION43																																	
			Disabled	0																															
			Enabled	1																															
M	RW	REGION44																																	
			Disabled	0																															
			Enabled	1																															
N	RW	REGION45																																	
			Disabled	0																															
			Enabled	1																															
O	RW	REGION46																																	
			Disabled	0																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Enabled	1																															
P	RW	REGION47																																	
			Disabled	0																															
			Enabled	1																															
Q	RW	REGION48																																	
			Disabled	0																															
			Enabled	1																															
R	RW	REGION49																																	
			Disabled	0																															
			Enabled	1																															
S	RW	REGION50																																	
			Disabled	0																															
			Enabled	1																															
T	RW	REGION51																																	
			Disabled	0																															
			Enabled	1																															
U	RW	REGION52																																	
			Disabled	0																															
			Enabled	1																															
V	RW	REGION53																																	
			Disabled	0																															
			Enabled	1																															
W	RW	REGION54																																	
			Disabled	0																															
			Enabled	1																															
X	RW	REGION55																																	
			Disabled	0																															
			Enabled	1																															
Y	RW	REGION56																																	
			Disabled	0																															
			Enabled	1																															
Z	RW	REGION57																																	
			Disabled	0																															
			Enabled	1																															
a	RW	REGION58																																	
			Disabled	0																															
			Enabled	1																															
b	RW	REGION59																																	
			Disabled	0																															
			Enabled	1																															
c	RW	REGION60																																	
			Disabled	0																															
			Enabled	1																															
d	RW	REGION61																																	
			Disabled	0																															
			Enabled	1																															
e	RW	REGION62																																	
			Disabled	0																															
			Enabled	1																															
f	RW	REGION63																																	
			Disabled	0																															
			Enabled	1																															

11.1.3 DISABLEINDEBUG

Address offset: 0x608

Disable protection mechanism in debug mode

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000001				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DISABLEINDEBUG																																	
			Disabled	1																															
			Enabled	0																															

11.1.4 CONFIG2

Address offset: 0x610

Block protect configuration register 2

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	REGION64																																	Enable protection for region 64. Write '0' has no effect.
			Disabled	0																															Protection disabled
			Enabled	1																															Protection enabled
B	RW	REGION65																																	Enable protection for region 65. Write '0' has no effect.
			Disabled	0																															Protection disabled
			Enabled	1																															Protection enabled
C	RW	REGION66																																	Enable protection for region 66. Write '0' has no effect.
			Disabled	0																															Protection disabled
			Enabled	1																															Protection enabled
D	RW	REGION67																																	Enable protection for region 67. Write '0' has no effect.
			Disabled	0																															Protection disabled
			Enabled	1																															Protection enabled
E	RW	REGION68																																	Enable protection for region 68. Write '0' has no effect.
			Disabled	0																															Protection disabled
			Enabled	1																															Protection enabled
F	RW	REGION69																																	Enable protection for region 69. Write '0' has no effect.
			Disabled	0																															Protection disabled
			Enabled	1																															Protection enabled
G	RW	REGION70																																	Enable protection for region 70. Write '0' has no effect.
			Disabled	0																															Protection disabled
			Enabled	1																															Protection enabled
H	RW	REGION71																																	Enable protection for region 71. Write '0' has no effect.
			Disabled	0																															Protection disabled
			Enabled	1																															Protection enabled
I	RW	REGION72																																	Enable protection for region 72. Write '0' has no effect.
			Disabled	0																															Protection disabled
			Enabled	1																															Protection enabled
J	RW	REGION73																																	Enable protection for region 73. Write '0' has no effect.
			Disabled	0																															Protection disabled
			Enabled	1																															Protection enabled
K	RW	REGION74																																	Enable protection for region 74. Write '0' has no effect.
			Disabled	0																															Protection disabled
			Enabled	1																															Protection enabled
L	RW	REGION75																																	Enable protection for region 75. Write '0' has no effect.
			Disabled	0																															Protection disabled

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Enabled	1																															
M	RW	REGION76																																	
			Disabled	0																															
			Enabled	1																															
N	RW	REGION77																																	
			Disabled	0																															
			Enabled	1																															
O	RW	REGION78																																	
			Disabled	0																															
			Enabled	1																															
P	RW	REGION79																																	
			Disabled	0																															
			Enabled	1																															
Q	RW	REGION80																																	
			Disabled	0																															
			Enabled	1																															
R	RW	REGION81																																	
			Disabled	0																															
			Enabled	1																															
S	RW	REGION82																																	
			Disabled	0																															
			Enabled	1																															
T	RW	REGION83																																	
			Disabled	0																															
			Enabled	1																															
U	RW	REGION84																																	
			Disabled	0																															
			Enabled	1																															
V	RW	REGION85																																	
			Disabled	0																															
			Enabled	1																															
W	RW	REGION86																																	
			Disabled	0																															
			Enabled	1																															
X	RW	REGION87																																	
			Disabled	0																															
			Enabled	1																															
Y	RW	REGION88																																	
			Disabled	0																															
			Enabled	1																															
Z	RW	REGION89																																	
			Disabled	0																															
			Enabled	1																															
a	RW	REGION90																																	
			Disabled	0																															
			Enabled	1																															
b	RW	REGION91																																	
			Disabled	0																															
			Enabled	1																															
c	RW	REGION92																																	
			Disabled	0																															
			Enabled	1																															
d	RW	REGION93																																	
			Disabled	0																															
			Enabled	1																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
e	RW	REGION94																																	
			Disabled	0																															
			Enabled	1																															
f	RW	REGION95																																	
			Disabled	0																															
			Enabled	1																															

11.1.5 CONFIG3

Address offset: 0x614

Block protect configuration register 3

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	REGION96																																	
			Disabled	0																															
			Enabled	1																															
B	RW	REGION97																																	
			Disabled	0																															
			Enabled	1																															
C	RW	REGION98																																	
			Disabled	0																															
			Enabled	1																															
D	RW	REGION99																																	
			Disabled	0																															
			Enabled	1																															
E	RW	REGION100																																	
			Disabled	0																															
			Enabled	1																															
F	RW	REGION101																																	
			Disabled	0																															
			Enabled	1																															
G	RW	REGION102																																	
			Disabled	0																															
			Enabled	1																															
H	RW	REGION103																																	
			Disabled	0																															
			Enabled	1																															
I	RW	REGION104																																	
			Disabled	0																															
			Enabled	1																															
J	RW	REGION105																																	
			Disabled	0																															
			Enabled	1																															
K	RW	REGION106																																	
			Disabled	0																															
			Enabled	1																															
L	RW	REGION107																																	
			Disabled	0																															
			Enabled	1																															
M	RW	REGION108																																	
			Disabled	0																															
			Enabled	1																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
N	RW	REGION109																																	
			Disabled	0																															
			Enabled	1																															
O	RW	REGION110																																	
			Disabled	0																															
			Enabled	1																															
P	RW	REGION111																																	
			Disabled	0																															
			Enabled	1																															
Q	RW	REGION112																																	
			Disabled	0																															
			Enabled	1																															
R	RW	REGION113																																	
			Disabled	0																															
			Enabled	1																															
S	RW	REGION114																																	
			Disabled	0																															
			Enabled	1																															
T	RW	REGION115																																	
			Disabled	0																															
			Enabled	1																															
U	RW	REGION116																																	
			Disabled	0																															
			Enabled	1																															
V	RW	REGION117																																	
			Disabled	0																															
			Enabled	1																															
W	RW	REGION118																																	
			Disabled	0																															
			Enabled	1																															
X	RW	REGION119																																	
			Disabled	0																															
			Enabled	1																															
Y	RW	REGION120																																	
			Disabled	0																															
			Enabled	1																															
Z	RW	REGION121																																	
			Disabled	0																															
			Enabled	1																															
a	RW	REGION122																																	
			Disabled	0																															
			Enabled	1																															
b	RW	REGION123																																	
			Disabled	0																															
			Enabled	1																															
c	RW	REGION124																																	
			Disabled	0																															
			Enabled	1																															
d	RW	REGION125																																	
			Disabled	0																															
			Enabled	1																															
e	RW	REGION126																																	
			Disabled	0																															
			Enabled	1																															
f	RW	REGION127																																	

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled

12 Factory information configuration registers (FICR)

Factory information configuration registers (FICR) are pre-programmed in factory and cannot be erased by the user. These registers contain chip-specific information and configuration.

12.1 Registers

Table 13: Instances

Base address	Peripheral	Instance	Description	Configuration
0x10000000	FICR	FICR	Factory Information Configuration	

Table 14: Register Overview

Register	Offset	Description
CODEPAGESIZE	0x010	Code memory page size
CODESIZE	0x014	Code memory size
CONFIGID	0x05C	Configuration identifier
DEVICEID[0]	0x060	Device identifier
DEVICEID[1]	0x064	Device identifier
ER[0]	0x080	Encryption Root, word 0
ER[1]	0x084	Encryption Root, word 1
ER[2]	0x088	Encryption Root, word 2
ER[3]	0x08C	Encryption Root, word 3
IR[0]	0x090	Identity Root, word 0
IR[1]	0x094	Identity Root, word 1
IR[2]	0x098	Identity Root, word 2
IR[3]	0x09C	Identity Root, word 3
DEVICEADDRTYPE	0x0A0	Device address type
DEVICEADDR[0]	0x0A4	Device address 0
DEVICEADDR[1]	0x0A8	Device address 1
INFO.PART	0x100	Part code
INFO.VARIANT	0x104	Part variant
INFO.PACKAGE	0x108	Package option
INFO.RAM	0x10C	RAM variant
INFO.FLASH	0x110	Flash variant
	0x114	Reserved
	0x118	Reserved
	0x11C	Reserved
NFC.TAGHEADER0	0x450	Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.
NFC.TAGHEADER1	0x454	Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.
NFC.TAGHEADER2	0x458	Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.
NFC.TAGHEADER3	0x45C	Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.

12.1.1 CODEPAGESIZE

Address offset: 0x010

Code memory page size

Bit number																															
Id																															
Reset 0xFFFFFFFF																															
Id	RW	Field	Value Id	Value	Description																										
A	R	CODEPAGESIZE			Code memory page size																										

12.1.2 CODESIZE

Address offset: 0x014

Code memory size

Bit number																															
Id																															
Reset 0xFFFFFFFF																															
Id	RW	Field	Value Id	Value	Description																										
A	R	CODESIZE			Code memory size in number of pages Total code space is: CODEPAGESIZE * CODESIZE																										

12.1.3 CONFIGID

Address offset: 0x05C

Configuration identifier

Bit number																															
Id																															
Reset 0xFFFFFFFF																															
Id	RW	Field	Value Id	Value	Description																										
A	R	HWID			Identification number for the HW																										
B	R	FWID			Identification number for the FW that is pre-loaded into the chip																									Deprecated	

12.1.4 DEVICEID[0]

Address offset: 0x060

Device identifier

Bit number																															
Id																															
Reset 0xFFFFFFFF																															
Id	RW	Field	Value Id	Value	Description																										
A	R	DEVICEID			64 bit unique device identifier DEVICEID[0] contains the least significant bits of the device identifier. DEVICEID[1] contains the most significant bits of the device identifier.																										

12.1.5 DEVICEID[1]

Address offset: 0x064

Device identifier

Bit number																															
Id																															
Reset 0xFFFFFFFF																															
Id	RW	Field	Value Id	Value	Description																										
A	R	DEVICEID			64 bit unique device identifier DEVICEID[0] contains the least significant bits of the device identifier. DEVICEID[1] contains the most significant bits of the device identifier.																										

12.1.6 ER[0]

Address offset: 0x080

Encryption Root, word 0

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	R	ER			Encryption Root, word n

12.1.7 ER[1]

Address offset: 0x084

Encryption Root, word 1

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	R	ER			Encryption Root, word n

12.1.8 ER[2]

Address offset: 0x088

Encryption Root, word 2

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	R	ER			Encryption Root, word n

12.1.9 ER[3]

Address offset: 0x08C

Encryption Root, word 3

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	R	ER			Encryption Root, word n

12.1.10 IR[0]

Address offset: 0x090

Identity Root, word 0

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	R	IR			Identity Root, word n

12.1.11 IR[1]

Address offset: 0x094

Identity Root, word 1

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFFF				**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	R	IR			Identity Root, word n

12.1.12 IR[2]

Address offset: 0x098

Identity Root, word 2

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFFF				**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	R	IR			Identity Root, word n

12.1.13 IR[3]

Address offset: 0x09C

Identity Root, word 3

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFFF				**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	R	IR			Identity Root, word n

12.1.14 DEVICEADDRTYPE

Address offset: 0x0A0

Device address type

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A
Reset 0xFFFFFFFF				**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	R	DEVICEADDRTYPE			Device address type
			Public	0	Public address
			Random	1	Random address

12.1.15 DEVICEADDR[0]

Address offset: 0x0A4

Device address 0

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFFF				**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Reset 0xFFFFFFFF				**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	R	DEVICEADDR			48 bit device address
					DEVICEADDR[0] contains the least significant bits of the device address. DEVICEADDR[1] contains the most significant bits of the device address. Only bits [15:0] of DEVICEADDR[1] are used.

12.1.16 DEVICEADDR[1]

Address offset: 0x0A8

Device address 1

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFFF				**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Reset 0xFFFFFFFF				**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	R	DEVICEADDR			48 bit device address DEVICEADDR[0] contains the least significant bits of the device address. DEVICEADDR[1] contains the most significant bits of the device address. Only bits [15:0] of DEVICEADDR[1] are used.

12.1.17 INFO.PART

Address offset: 0x100

Part code

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00052000				**0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	R	PART			Part code
			N51822	0x51822	nRF51822
			N51422	0x51422	nRF51422
			N52000	0x52000	nRF52000
			Unspecified	0xFFFFFFFF	Unspecified

12.1.18 INFO.VARIANT

Address offset: 0x104

Part variant

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFFF				**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	R	VARIANT			Part variant
			nRF51C	0x1002	nRF51-C
			nRF51D	0x1003	nRF51-D
			nRF51E	0x1004	nRF51-E
			Unspecified	0xFFFFFFFF	Unspecified

12.1.19 INFO.PACKAGE

Address offset: 0x108

Package option

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	R	PACKAGE			Package option
			QFN48	0x0000	48-pin QFN with 31 GPIO
			nRF51CSP56A	0x1000	nRF51x22 CDxx - WLCSP 56 balls
			nRF51CSP62A	0x1001	nRF51x22 CExx - WLCSP 62 balls
			nRF51CSP62B	0x1002	nRF51x22 CFxx - WLCSP 62 balls
			nRF51CSP62C	0x1003	nRF51x22 CTxx - WLCSP 62 balls
			Unspecified	0xFFFFFFFF	Unspecified

12.1.20 INFO.RAM

Address offset: 0x10C

RAM variant

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000040				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	RAM																																	
			K16	16																															
			K32	32																															
			K64	64																															
			Unspecified	0xFFFFFFFF																															

12.1.21 INFO.FLASH

Address offset: 0x110

Flash variant

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000200				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	FLASH																																	
			K128	128																															
			K256	256																															
			K512	512																															
			Unspecified	0xFFFFFFFF																															

12.1.22 NFC.TAGHEADER0

Address offset: 0x450

Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				D	D	D	D	D	D	D	D	C	C	C	C	C	C	C	C	B	B	B	B	B	B	B	B	A	A	A	A	A	A	A	A
Reset 0xFFFFFF5F				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	MFGID																																	
B	R	UD1																																	
C	R	UD2																																	
D	R	UD3																																	

12.1.23 NFC.TAGHEADER1

Address offset: 0x454

Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				D	D	D	D	D	D	D	D	C	C	C	C	C	C	C	C	B	B	B	B	B	B	B	B	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	UD4																																	
B	R	UD5																																	
C	R	UD6																																	
D	R	UD7																																	

12.1.24 NFC.TAGHEADER2

Address offset: 0x458

Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.

Bit number																																
Id																																
Reset 0xFFFFFFFF																																
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																											
A	R	UD8			Unique identifier byte 8																											
B	R	UD9			Unique identifier byte 9																											
C	R	UD10			Unique identifier byte 10																											
D	R	UD11			Unique identifier byte 11																											

12.1.25 NFC.TAGHEADER3

Address offset: 0x45C

Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.

Bit number																																
Id																																
Reset 0xFFFFFFFF																																
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																											
A	R	UD12			Unique identifier byte 12																											
B	R	UD13			Unique identifier byte 13																											
C	R	UD14			Unique identifier byte 14																											
D	R	UD15			Unique identifier byte 15																											

13 User information configuration registers (UICR)

The user information configuration registers (UICRs) are non-volatile memory (NVM) registers for configuring user specific settings.

For information on writing UICR registers, see the *Non-volatile memory controller (NVMC)* on page 38 and *Memory* on page 34 chapters.

13.1 Registers

Table 15: Instances

Base address	Peripheral	Instance	Description	Configuration
0x10001000	UICR	UICR	User Information Configuration	

Table 16: Register Overview

Register	Offset	Description	
	0x000		Reserved
	0x004		Reserved
	0x008		Reserved
	0x010		Reserved
NRFFW[0]	0x014	Reserved for Nordic firmware design	
NRFFW[1]	0x018	Reserved for Nordic firmware design	
NRFFW[2]	0x01C	Reserved for Nordic firmware design	
NRFFW[3]	0x020	Reserved for Nordic firmware design	
NRFFW[4]	0x024	Reserved for Nordic firmware design	
NRFFW[5]	0x028	Reserved for Nordic firmware design	
NRFFW[6]	0x02C	Reserved for Nordic firmware design	
NRFFW[7]	0x030	Reserved for Nordic firmware design	
NRFFW[8]	0x034	Reserved for Nordic firmware design	
NRFFW[9]	0x038	Reserved for Nordic firmware design	
NRFFW[10]	0x03C	Reserved for Nordic firmware design	
NRFFW[11]	0x040	Reserved for Nordic firmware design	
NRFFW[12]	0x044	Reserved for Nordic firmware design	
NRFFW[13]	0x048	Reserved for Nordic firmware design	
NRFFW[14]	0x04C	Reserved for Nordic firmware design	
NRFHW[0]	0x050	Reserved for Nordic hardware design	
NRFHW[1]	0x054	Reserved for Nordic hardware design	
NRFHW[2]	0x058	Reserved for Nordic hardware design	
NRFHW[3]	0x05C	Reserved for Nordic hardware design	
NRFHW[4]	0x060	Reserved for Nordic hardware design	
NRFHW[5]	0x064	Reserved for Nordic hardware design	
NRFHW[6]	0x068	Reserved for Nordic hardware design	
NRFHW[7]	0x06C	Reserved for Nordic hardware design	
NRFHW[8]	0x070	Reserved for Nordic hardware design	
NRFHW[9]	0x074	Reserved for Nordic hardware design	
NRFHW[10]	0x078	Reserved for Nordic hardware design	
NRFHW[11]	0x07C	Reserved for Nordic hardware design	
CUSTOMER[0]	0x080	Reserved for customer	
CUSTOMER[1]	0x084	Reserved for customer	
CUSTOMER[2]	0x088	Reserved for customer	
CUSTOMER[3]	0x08C	Reserved for customer	
CUSTOMER[4]	0x090	Reserved for customer	
CUSTOMER[5]	0x094	Reserved for customer	
CUSTOMER[6]	0x098	Reserved for customer	

Register	Offset	Description
CUSTOMER[7]	0x09C	Reserved for customer
CUSTOMER[8]	0x0A0	Reserved for customer
CUSTOMER[9]	0x0A4	Reserved for customer
CUSTOMER[10]	0x0A8	Reserved for customer
CUSTOMER[11]	0x0AC	Reserved for customer
CUSTOMER[12]	0x0B0	Reserved for customer
CUSTOMER[13]	0x0B4	Reserved for customer
CUSTOMER[14]	0x0B8	Reserved for customer
CUSTOMER[15]	0x0BC	Reserved for customer
CUSTOMER[16]	0x0C0	Reserved for customer
CUSTOMER[17]	0x0C4	Reserved for customer
CUSTOMER[18]	0x0C8	Reserved for customer
CUSTOMER[19]	0x0CC	Reserved for customer
CUSTOMER[20]	0x0D0	Reserved for customer
CUSTOMER[21]	0x0D4	Reserved for customer
CUSTOMER[22]	0x0D8	Reserved for customer
CUSTOMER[23]	0x0DC	Reserved for customer
CUSTOMER[24]	0x0E0	Reserved for customer
CUSTOMER[25]	0x0E4	Reserved for customer
CUSTOMER[26]	0x0E8	Reserved for customer
CUSTOMER[27]	0x0EC	Reserved for customer
CUSTOMER[28]	0x0F0	Reserved for customer
CUSTOMER[29]	0x0F4	Reserved for customer
CUSTOMER[30]	0x0F8	Reserved for customer
CUSTOMER[31]	0x0FC	Reserved for customer
PSELRESET[0]	0x200	Mapping of the nRESET function (see POWER chapter for details)
PSELRESET[1]	0x204	Mapping of the nRESET function (see POWER chapter for details)
APPROTECT	0x208	Access port protection
NFCPINS	0x20C	Setting of pins dedicated to NFC functionality: NFC antenna or GPIO

13.1.1 NRFFW[0]

Address offset: 0x014

Reserved for Nordic firmware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFFW			Reserved for Nordic firmware design

13.1.2 NRFFW[1]

Address offset: 0x018

Reserved for Nordic firmware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFFW			Reserved for Nordic firmware design

13.1.3 NRFFW[2]

Address offset: 0x01C

Reserved for Nordic firmware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFFW			Reserved for Nordic firmware design

13.1.4 NRFFW[3]

Address offset: 0x020

Reserved for Nordic firmware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFFW			Reserved for Nordic firmware design

13.1.5 NRFFW[4]

Address offset: 0x024

Reserved for Nordic firmware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFFW			Reserved for Nordic firmware design

13.1.6 NRFFW[5]

Address offset: 0x028

Reserved for Nordic firmware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFFW			Reserved for Nordic firmware design

13.1.7 NRFFW[6]

Address offset: 0x02C

Reserved for Nordic firmware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFFW			Reserved for Nordic firmware design

13.1.8 NRFFW[7]

Address offset: 0x030

Reserved for Nordic firmware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFFW			Reserved for Nordic firmware design

13.1.9 NRFFW[8]

Address offset: 0x034

Reserved for Nordic firmware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFFW			Reserved for Nordic firmware design

13.1.10 NRFFW[9]

Address offset: 0x038

Reserved for Nordic firmware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFFW			Reserved for Nordic firmware design

13.1.11 NRFFW[10]

Address offset: 0x03C

Reserved for Nordic firmware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFFW			Reserved for Nordic firmware design

13.1.12 NRFFW[11]

Address offset: 0x040

Reserved for Nordic firmware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFFW			Reserved for Nordic firmware design

13.1.13 NRFFW[12]

Address offset: 0x044

Reserved for Nordic firmware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFFW			Reserved for Nordic firmware design

13.1.14 NRFFW[13]

Address offset: 0x048

Reserved for Nordic firmware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFFW			Reserved for Nordic firmware design

13.1.15 NRFFW[14]

Address offset: 0x04C

Reserved for Nordic firmware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFFW			Reserved for Nordic firmware design

13.1.16 NRFHW[0]

Address offset: 0x050

Reserved for Nordic hardware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFHW			Reserved for Nordic hardware design

13.1.17 NRFHW[1]

Address offset: 0x054

Reserved for Nordic hardware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFHW			Reserved for Nordic hardware design

13.1.18 NRFHW[2]

Address offset: 0x058

Reserved for Nordic hardware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFHW			Reserved for Nordic hardware design

13.1.19 NRFHW[3]

Address offset: 0x05C

Reserved for Nordic hardware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFHW			Reserved for Nordic hardware design

13.1.20 NRFHW[4]

Address offset: 0x060

Reserved for Nordic hardware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFHW			Reserved for Nordic hardware design

13.1.21 NRFHW[5]

Address offset: 0x064

Reserved for Nordic hardware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFHW			Reserved for Nordic hardware design

13.1.22 NRFHW[6]

Address offset: 0x068

Reserved for Nordic hardware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFHW			Reserved for Nordic hardware design

13.1.23 NRFHW[7]

Address offset: 0x06C

Reserved for Nordic hardware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFHW			Reserved for Nordic hardware design

13.1.24 NRFHW[8]

Address offset: 0x070

Reserved for Nordic hardware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFHW			Reserved for Nordic hardware design

13.1.25 NRFHW[9]

Address offset: 0x074

Reserved for Nordic hardware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFHW			Reserved for Nordic hardware design

13.1.26 NRFHW[10]

Address offset: 0x078

Reserved for Nordic hardware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFHW			Reserved for Nordic hardware design

13.1.27 NRFHW[11]

Address offset: 0x07C

Reserved for Nordic hardware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	NRFHW			Reserved for Nordic hardware design

13.1.28 CUSTOMER[0]

Address offset: 0x080

Reserved for customer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	CUSTOMER			Reserved for customer

13.1.29 CUSTOMER[1]

Address offset: 0x084

Reserved for customer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	CUSTOMER			Reserved for customer

13.1.30 CUSTOMER[2]

Address offset: 0x088

Reserved for customer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	CUSTOMER			Reserved for customer

13.1.31 CUSTOMER[3]

Address offset: 0x08C

Reserved for customer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	CUSTOMER			Reserved for customer

13.1.32 CUSTOMER[4]

Address offset: 0x090

Reserved for customer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	CUSTOMER			Reserved for customer

13.1.33 CUSTOMER[5]

Address offset: 0x094

Reserved for customer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	CUSTOMER			Reserved for customer

13.1.34 CUSTOMER[6]

Address offset: 0x098

Reserved for customer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	CUSTOMER			Reserved for customer

13.1.35 CUSTOMER[7]

Address offset: 0x09C

Reserved for customer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	CUSTOMER			Reserved for customer

13.1.36 CUSTOMER[8]

Address offset: 0x0A0

Reserved for customer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	CUSTOMER			Reserved for customer

13.1.37 CUSTOMER[9]

Address offset: 0x0A4

Reserved for customer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	CUSTOMER			Reserved for customer

13.1.38 CUSTOMER[10]

Address offset: 0x0A8

Reserved for customer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	CUSTOMER			Reserved for customer

13.1.39 CUSTOMER[11]

Address offset: 0x0AC

Reserved for customer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	CUSTOMER			Reserved for customer

13.1.40 CUSTOMER[12]

Address offset: 0x0B0

Reserved for customer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	CUSTOMER			Reserved for customer

13.1.41 CUSTOMER[13]

Address offset: 0x0B4

Reserved for customer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	CUSTOMER			Reserved for customer

13.1.42 CUSTOMER[14]

Address offset: 0x0B8

Reserved for customer

Bit number																																
Id																																
Reset 0xFFFFFFFF																																
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																											
A	RW	CUSTOMER			Reserved for customer																											

13.1.43 CUSTOMER[15]

Address offset: 0x0BC

Reserved for customer

Bit number																																
Id																																
Reset 0xFFFFFFFF																																
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																											
A	RW	CUSTOMER			Reserved for customer																											

13.1.44 CUSTOMER[16]

Address offset: 0x0C0

Reserved for customer

Bit number																																
Id																																
Reset 0xFFFFFFFF																																
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																											
A	RW	CUSTOMER			Reserved for customer																											

13.1.45 CUSTOMER[17]

Address offset: 0x0C4

Reserved for customer

Bit number																																
Id																																
Reset 0xFFFFFFFF																																
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																											
A	RW	CUSTOMER			Reserved for customer																											

13.1.46 CUSTOMER[18]

Address offset: 0x0C8

Reserved for customer

Bit number																																
Id																																
Reset 0xFFFFFFFF																																
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																											
A	RW	CUSTOMER			Reserved for customer																											

13.1.47 CUSTOMER[19]

Address offset: 0x0CC

Reserved for customer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	CUSTOMER			Reserved for customer

13.1.48 CUSTOMER[20]

Address offset: 0x0D0

Reserved for customer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	CUSTOMER			Reserved for customer

13.1.49 CUSTOMER[21]

Address offset: 0x0D4

Reserved for customer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	CUSTOMER			Reserved for customer

13.1.50 CUSTOMER[22]

Address offset: 0x0D8

Reserved for customer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	CUSTOMER			Reserved for customer

13.1.51 CUSTOMER[23]

Address offset: 0x0DC

Reserved for customer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	CUSTOMER			Reserved for customer

13.1.52 CUSTOMER[24]

Address offset: 0x0E0

Reserved for customer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Id	RW	Field	Value Id	Value	Description
A	RW	CUSTOMER			Reserved for customer

13.1.53 CUSTOMER[25]

Address offset: 0x0E4

Reserved for customer

Bit number																															
Id																															
Reset 0xFFFFFFFF																															
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	CUSTOMER			Reserved for customer

13.1.54 CUSTOMER[26]

Address offset: 0x0E8

Reserved for customer

Bit number																															
Id																															
Reset 0xFFFFFFFF																															
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	CUSTOMER			Reserved for customer

13.1.55 CUSTOMER[27]

Address offset: 0x0EC

Reserved for customer

Bit number																															
Id																															
Reset 0xFFFFFFFF																															
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	CUSTOMER			Reserved for customer

13.1.56 CUSTOMER[28]

Address offset: 0x0F0

Reserved for customer

Bit number																															
Id																															
Reset 0xFFFFFFFF																															
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	CUSTOMER			Reserved for customer

13.1.57 CUSTOMER[29]

Address offset: 0x0F4

Reserved for customer

Bit number																															
Id																															
Reset 0xFFFFFFFF																															
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	CUSTOMER			Reserved for customer

13.1.58 CUSTOMER[30]

Address offset: 0x0F8

Reserved for customer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	CUSTOMER																																	
				Reserved for customer																															

13.1.59 CUSTOMER[31]

Address offset: 0x0FC

Reserved for customer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	CUSTOMER																																	
				Reserved for customer																															

13.1.60 PSELRESET[0]

Address offset: 0x200

Mapping of the nRESET function (see POWER chapter for details)

All PSELRESET registers have to contain the same value for a pin mapping to be valid. If they don't, there will be no nRESET function exposed on a GPIO, and the device will always start independently of the levels present on any of the GPIOs.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				B																															
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PIN		21																															
				GPIO number P0.n onto which Reset is exposed																															
B	RW	CONNECT																																	
				Connection																															
			Disconnected	1																															
				Disconnect																															
			Connected	0																															
				Connect																															

13.1.61 PSELRESET[1]

Address offset: 0x204

Mapping of the nRESET function (see POWER chapter for details)

All PSELRESET registers have to contain the same value for a pin mapping to be valid. If they don't, there will be no nRESET function exposed on a GPIO, and the device will always start independently of the levels present on any of the GPIOs.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				B																															
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PIN		21																															
				GPIO number P0.n onto which Reset is exposed																															
B	RW	CONNECT																																	
				Connection																															
			Disconnected	1																															
				Disconnect																															
			Connected	0																															
				Connect																															

13.1.62 APPROTECT

Address offset: 0x208

Access port protection

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																											A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF			**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	RW	PALL																									Blocks debugger read/write access to all CPU registers and memory mapped addresses							
			Disabled								0xFF																Disable							
			Enabled								0x00																Enable							

13.1.63 NFCPINS

Address offset: 0x20C

Setting of pins dedicated to NFC functionality: NFC antenna or GPIO

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		A
Reset 0xFFFFFFFF			**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	RW	PROTECT																									Setting of pins dedicated to NFC functionality							
			Disabled								0																Operation as GPIO pins. Same protection as normal GPIO pins							
			NFC								1																Operation as NFC antenna pins. Configures the protection for NFC operation							

14 Peripheral interface

Peripherals can be accessed through the standard ARM® Cortex Advanced Peripheral Bus (APB) or AMBA High-performance Bus (AHB) registers as well as through task, event, and interrupt registers.

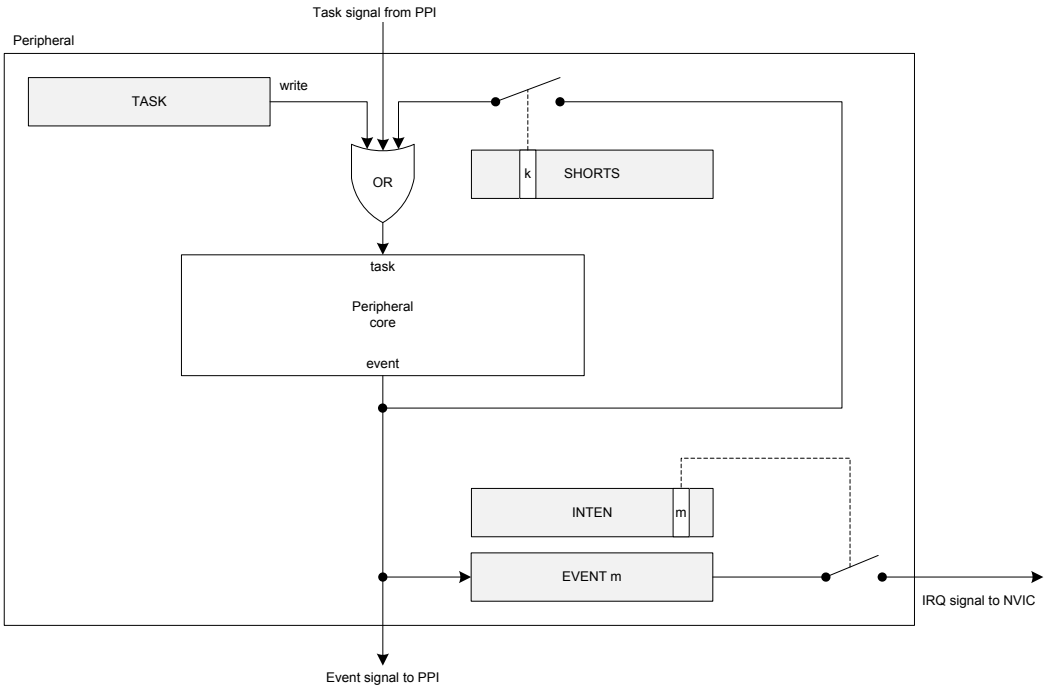

Figure 7: Tasks, events, shortcuts, and interrupts

14.1 Peripheral ID

Every peripheral is assigned a fixed block of 0x1000 bytes of address space, which is equal to 1024 x 32 bit registers. This pattern is applied to all peripherals located on the APB bus and on the AHB bus.

See *Instantiation* on page 36 for more information about which peripherals are available and where they are located in the address map.

For peripherals on the APB bus there is a direct relationship between its ID and its base address. A peripheral with base address 0x40000000 is therefore assigned ID=0, and a peripheral with base address 0x40001000 is assigned ID=1. The peripheral with base address 0x4001F000 is assigned ID=31.

Peripherals may share the same ID, which may impose one or more of the following limitations:

- Some peripherals share some registers or other common resources.
- Operation is mutually exclusive. Only one of the peripherals can be used at a time.
- Switching from one peripheral to another must follow a specific pattern (disable the first, then enable the second peripheral).

When switching between two mutually exclusive peripherals that share the same ID the user should do the following to prevent unwanted behavior:

- Disable the previously used peripheral
- Remove any PPI connections set up for the peripheral that is being disabled
- Clear all bits in the INTEN register, i.e. INTENCLR = 0xFFFFFFFF.
- Explicitly configure the peripheral that you enable and do not rely on configuration values that may be inherited from the peripheral that was disabled.

- Enable the now configured peripheral.

14.2 Bit set and clear

Registers with multiple single-bit bit fields may implement the "set-and-clear" pattern. This pattern enables firmware to set and clear individual bits in a register without having to perform a read-modify-write operation on the main register.

This pattern is implemented using three consecutive addresses in the register map where the main register is followed by a dedicated SET and CLR register in that order.

The SET register is used to set individual bits in the main register while the CLR register is used to clear individual bits in the main register. Writing a '1' to a bit in the SET or CLR register will set or clear the same bit in the main register respectively. Writing a '0' to a bit in the SET or CLR register has no effect. Reading the SET or CLR registers returns the value of the main register.

Restriction: The main register may not be visible and hence not directly accessible in all cases.

14.3 Tasks

Tasks are used to trigger actions in a peripheral, for example, to start a particular behavior. A peripheral can implement multiple tasks with each task having a separate register in that peripheral's task register group.

A task is triggered when firmware writes a '1' to the task register or when the peripheral itself or another peripheral toggles the corresponding task signal. See *Figure 7: Tasks, events, shortcuts, and interrupts* on page 74.

14.4 Events

Events are used to notify peripherals and the CPU about events that have happened, for example, a state change in a peripheral. A peripheral may generate multiple events with each event having a separate register in that peripheral's event register group.

An event is generated when the peripheral itself toggles the corresponding event signal, whereupon the event register is updated to reflect that the event has been generated. See *Figure 7: Tasks, events, shortcuts, and interrupts* on page 74. An event register is only cleared when firmware writes a '0' to it.

Events can be generated by the peripheral even when the event register is set to '1'.

14.5 Shortcuts

A shortcut is a direct connection between an event and a task within the same peripheral. If a shortcut is enabled, its associated task is automatically triggered when its associated event is generated.

Using a shortcut is the equivalent to making the same connection outside the peripheral and through the PPI. However, the propagation delay through the shortcut is usually shorter than the propagation delay through the PPI.

Shortcuts are predefined, which means their connections cannot be configured by firmware. Each shortcut can be individually enabled or disabled through the shortcut register, one bit per shortcut, giving a maximum of 32 shortcuts for each peripheral.

14.6 Interrupts

An interrupt is an exception that is generated by an event and can interrupt the program flow of the CPU.

All peripherals on the APB bus support interrupts. A peripheral only occupies one interrupt, and the interrupt number follows the peripheral ID, for example, the peripheral with ID=4 is connected to interrupt number 4 in the Nested Vector Interrupt Controller (NVIC).

Using the INTEN, INTENSET and INTENCLR registers, you can configure every event in a peripheral to generate that peripheral's interrupt. You can enable multiple events to generate interrupts simultaneously. To resolve the correct interrupt's source, firmware can query the event registers found in the event group in the peripherals register map.

Some peripherals implement only INTENSET and INTENCLR, the INTEN register is not available on those peripherals. Refer to the individual chapters for details. In all cases, however, reading back the INTENSET or INTENCLR register returns the same information as in INTEN.

Each event implemented in the peripheral is associated with a specific bit position in the INTEN, INTENSET and INTENCLR registers. The correct bit position can be derived from the event's address. The event on address 0x100 is associated with bit 0 in the INTEN register, the event at address 0x104 is associated with bit 1, and so on. The event at address 0x17C is identified with bit 31 in the INTEN register. This pattern effectively limits the maximum number of events in a peripheral to 32.

The relationship between tasks, events, shortcuts, and interrupts is shown in *Figure 7: Tasks, events, shortcuts, and interrupts* on page 74.

14.6.1 Interrupt clearing

Clearing an IRQ signal from a peripheral may not take immediate effect seen from the processor. When clearing an event register or setting the INTENCLR register, the processor may delay the write onto the bus, or the bus itself may insert a delay. In some cases firmware needs to take this into account, e.g. when clearing the IRQ signal right before exiting the interrupt handler. Since the effect on the IRQ signal can be delayed, the NVIC may detect it as a new interrupt and the interrupt handler is called again. To avoid this, it is recommended to perform a read from any register in the peripheral (e.g. event or INTENCLR register). Reading from a register on the same peripheral will ensure that the write operation is completed before the read occurs.

15 Debugger interface (DIF)

The Debugger interface (DIF) module provides access to the on-chip debug functionality. The debug interface to the device is a standard two-pin serial wire debug (SWD) interface as defined by ARM™.

Listed here are the main features for DIF:

- Standard ARM Debug Access Port (DAP)
- Flash Patch and Breakpoint Unit (FPB) supports:
  - Two literal comparators
  - Six instruction comparators
- Data Watchpoint and Trace Unit (DWT)
  - Four comparators
- Instrumentation Trace Macrocell (ITM)
- Embedded Trace Macrocell (ETM)
- Trace Port Interface Unit (TPIU)
  - ITM and ETM trace
  - Parallel Trace Port (4-bit) and Single Wire Output (SWO)

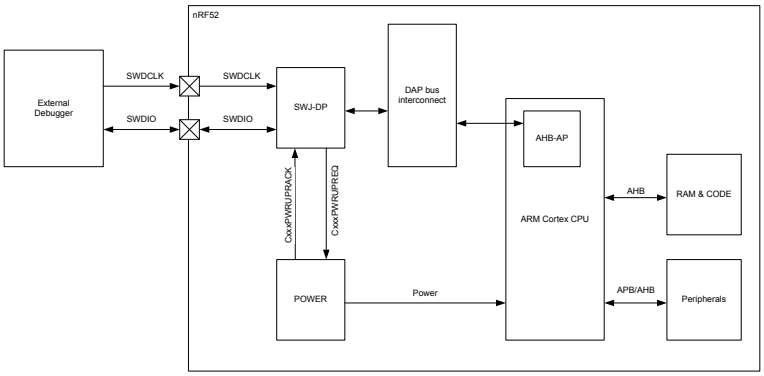

Figure 8: Debugger interface

The debug feature set offers a flexible and powerful mechanism for non-intrusive debugging of program code. Breakpoints, single stepping, and instruction trace capture of code execution flow are part of this support.

Also supported is a real-time debug mechanism to allow interrupts to execute to completion in real time when breakpoints are set in Thread mode or lower priority interrupts. This enables the developer to set a breakpoint and single step through their code without a failure of the real-time event driven threads running at higher priority. For example, this enables the device to continue to service the high priority interrupts of an external controller or sensor without failure or loss of state synchronization while the developer steps through code in a low priority thread. In this way, it is possible to continue.

- SW or HW triggered capture and dump of resource status from within an application
- SW or HW triggered continuous capture of changes in status of resources from active to inactive over time

Before the external debugger can access the CPU it must first request and make sure that the appropriate power domains are powered up. This is handled using the built in CxxxPWRUPREQ and CxxxPWRUPACK feature found in the ARM CoreSight DAP.

As long as the debugger is requesting the debug domain or the complete system to be powered up, the device will be in debug interface mode. Some peripherals will behave differently in debug interface mode compared to normal operation mode where the debugger is not requesting any of the power domains to be powered up. More information about these differences is described in the chapters of the peripherals that are affected.

Important:

- The SWDIO line has an internal pull-up resistor.
- The SWDCLK line has an internal pull-down resistor.

15.1 Trace pin multiplexing

There are two ways of getting trace data out from the chip, through the Single Wire Output (SWO) pin or the parallel trace port pins.

For ITM tracing, the single SWO trace port is sufficient. When using ETM the parallel trace port must be used, to ensure enough throughput. For details of how to use the debug and trace capabilities, please read the debug documentation of your IDE.

When serial tracing is enabled the SWO signal is multiplexed onto P0.18. When parallel trace is enabled, the TRACEDATA[0..3] and TRACECLK signals are multiplexed onto P0.18, P0.16, P0.15, P0.14 and P0.20 respectively. When tracing is disabled, GPIOs are multiplexed onto the multi-function pins. The trace pin multiplexing is configurable through the *TRACECONFIG* on page 108 register, see *Clock management (CLOCK)* on page 101.

Note that the speed of these GPIOs depends on the DRIVE setting in their respective PIN_CNF register. Only S0S1 and H0H1 drives are suitable for debugging. S0S1 is the default DRIVE at reset. If parallel or serial trace port signals are not fast enough in the debugging conditions, all GPIOs in use for tracing should be set to high drive (H0H1). The user shall make sure that these GPIOs' DRIVE is not overwritten by software during the debugging session.

Refer to *PIN_CNF[14]* on page 138, *PIN_CNF[15]* on page 139, *PIN_CNF[16]* on page 139, *PIN_CNF[18]* on page 141 and *PIN_CNF[20]* on page 142.

Trace mechanism	Unavailable GPIOs
Parallel trace	TRACEDATA[3..0]: P0.18, P0.16, P0.15, P0.14 TRACECLK: P0.20
Serial trace (SWO)	P0.18

16 Power management (POWER)

Power management architecture gives you unique flexibility through individual power control of all system blocks on the device.

The power management system is highly flexible with functional blocks such as the CPU, radio transceiver, and peripherals having separate power state control in addition to the global System ON and OFF modes.

Power management and supply has the following features:

- On-chip LDO regulator
- On-chip DC/DC regulator
- Global System ON/OFF modes
- RAM block power control for retention in System OFF mode and to power down unused blocks in System ON mode
- Analog or digital pin wakeup from System OFF
- Independent and auto-controlled peripheral block RUN/IDLE in System ON mode
- Supervisor HW to manage power on reset, brownout, and power fail
- Auto-controlled refresh modes for LDO and DC/DC regulators to maximize efficiency
- Automatic switching between LDO and DC/DC regulator based on load to maximize efficiency

Note: Two additional external passive components are required to use the DC/DC converter.

16.1 Power supply

The following power supply alternatives are supported:

- Internal DC/DC converter setup
- Internal LDO setup

16.2 Main regulators

The default power supply option is the on-chip low drop out (LDO) linear voltage regulator. This regulator takes the input 1.7 to 3.6 V supply and provides 1.3 V regulated supply for device function blocks. The LDO regulator automatically switches to a refresh mode to minimize current consumption in the power supply system itself when load current is low.

A DC/DC buck converter is placed in parallel with the LDO and is optionally enabled by an application. The DC/DC converter offers up to 50% lower current consumption, and is especially efficient for applications using battery technologies with higher nominal cell voltages. The DC/DC converter, like the LDO, has a refresh mode which is automatically engaged to minimize current consumption.

The main regulators are requested by on-chip peripherals as needed and will be switched off when not requested. The main regulator can also be forced to remain on using constant latency sub power mode to reduce event latencies and CPU startup time if required by the application.

Regulator refresh mode switches regulator output on and off with a variable duty cycle based on output load. The regulator self-current is reduced on average for low load currents which increases power efficiency.

The external device I/Os are always supplied directly from the external supply to ensure I/O signal compatibility with other devices on the PCB.

16.3 LDO regulator setup

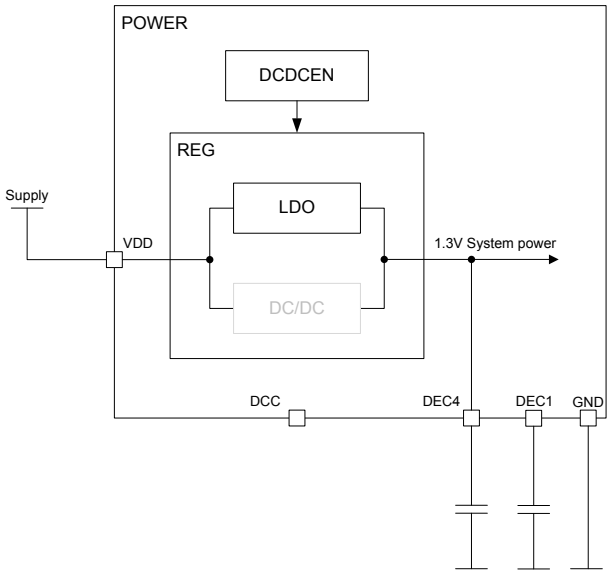

Figure 9: LDO regulator setup

16.4 DC/DC converter setup

The DC/DC converter setup can be used as an alternative to using the internal LDO regulator. Using the DC/DC converter will, in general, give reduced power consumption compared to using the LDO regulator.

The DC/DC converter requires an external LC filter as shown in *Figure 10: DC/DC converter setup* on page 80 and is enabled through the *DCDCEN* on page 89 register.

The required component values for the external LC-filter are:

- C = 1 uF
- L = 10 uH

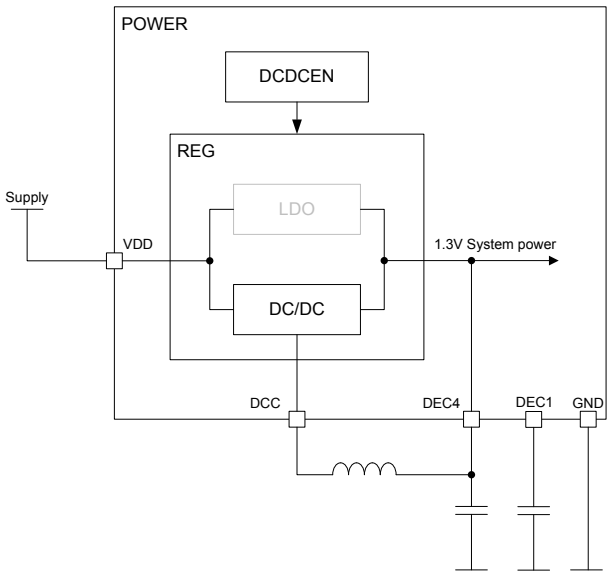

Figure 10: DC/DC converter setup

16.5 System OFF mode

System OFF is the deepest power saving mode the system can enter. In this mode, the system's core functionality is powered down and all ongoing tasks are terminated. The only mechanism that is functional and responsive in this mode is the reset and the wakeup mechanism.

The device can be put into System OFF mode using the POWER register interface. When in System OFF mode the device can be woken up through one of the following signals:

1. The DETECT signal, optionally generated by the GPIO peripheral
2. The ANADETECT signal, optionally generated by the LPCOMP module
3. The SENSE signal, optionally generated by the NFC module to "wake-on-field"
4. A reset

When the system wakes up from System OFF mode, a system reset is performed.

One or more 4k RAM blocks of RAM can be retained in System OFF mode depending on the settings in the RAM[n].POWER registers.

RAM[n].POWER are retained registers, see *Reset behavior*. Note that these registers are usually overwritten by the startup code provided with the nRF application examples.

Before entering System OFF mode the user must make sure that all on-going EasyDMA transactions have been completed. This is usually accomplished by making sure that the EasyDMA enabled peripheral is not active when entering System OFF.

16.5.1 Emulated System OFF mode

If the device is in debug interface mode, System OFF will be emulated to secure that all required resources needed for debugging are available during System OFF, see *DIF* chapter for more information. Required resources needed for debugging include the following key components: DIF, CLOCK, POWER, NVMC, CPU, CODE, and RAM. Since the CPU is kept on in emulated System OFF mode, it is recommended to add an infinite loop directly after entering System OFF, to prevent the CPU from executing code that normally should not be executed.

16.6 System ON mode

System ON is the default state after power-on reset. In System ON, all functional blocks will independently be in IDLE or RUN mode depending on the functionality needed by the application.

System ON is the default state after power-on reset. In System ON all functional blocks, such as the CPU or peripherals, can independently be in IDLE or RUN mode, depending on the functionality needed by the application.

The system can switch on and off the appropriate internal power sources depending on how much power is needed at any given time. The power requirement of a peripheral is directly related to its activity level, and the activity level of a peripheral is usually raised and lowered when specific tasks are triggered or events are generated.

16.6.1 Sub power modes

In System ON mode, when both the CPU and all the peripherals are in IDLE mode, the system can reside in one of the following two sub power modes:

- Constant latency
- Low power

In constant latency mode the CPU wakeup latency and the PPI task response will be constant and kept at a minimum. This is secured by forcing a set of base resources on while in sleep. The advantage of having a constant and predictable latency will be at the cost of having increased power consumption. The constant latency mode is selected by triggering the CONSTLAT task.

In low power mode the automatic power management system, described in *System ON mode* on page 81, ensures the most efficient supply option is chosen to save the most power. The advantage of having the lowest power possible will be at the cost of having varying CPU wakeup latency and PPI task response. The low power mode is selected by triggering the LOWPWR task.

When the system enters System ON mode, it will, by default, reside in the low power sub-power mode.

16.7 Power supply supervisor

The power supply supervisor initializes the system at power-on and provides an early warning of impending power failure. In addition the power supply supervisor puts the system in a reset state if the supply voltage is too low for safe operation (brownout). The power supply supervisor is illustrated in *Figure 11: Power supply supervisor* on page 82.

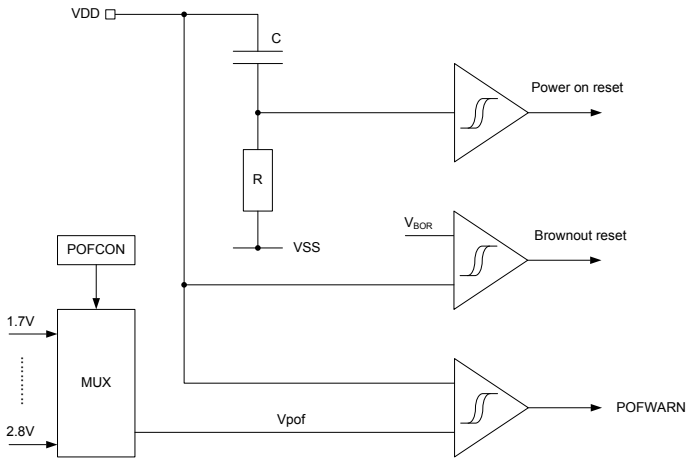

Figure 11: Power supply supervisor

16.8 Power-fail comparator

The power-fail comparator provides the CPU with an early warning of impending power failure. It will not reset the system, but give the CPU time to prepare for an orderly power-down.

The comparator features a hysteresis of $V_{POFHYST}$ (refer to the Product Specification for the exact value), as illustrated in *Figure 12: Power-fail comparator (BOR = Brownout reset)* on page 83. The threshold V_{POF} is set in the POFCON register.

If power fail warning is enabled and the supply voltage is below V_{POF} the power fail comparator will prevent the NVMC from performing write operations to the NVM. See *NVMC* chapter for more information about the NVMC.

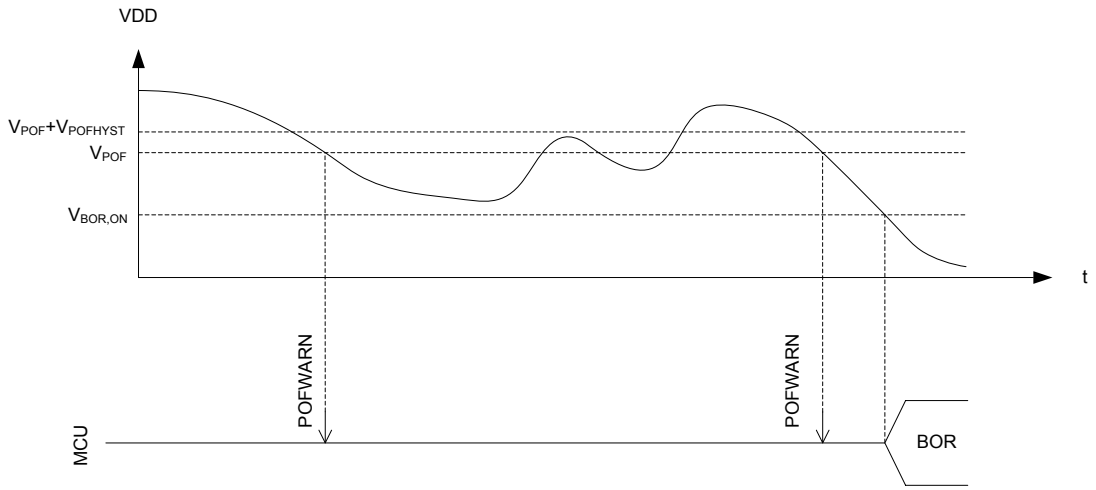

Figure 12: Power-fail comparator (BOR = Brownout reset)

To save power the power-fail comparator is not active in System OFF or in System ON when HFLKC is not running.

16.9 RAM blocks

Each of the available RAM blocks, which each may contain multiple RAM sections, can power up and down independently in both System ON and System OFF mode, using the RAM[n] registers. See *Memory* chapter for more information about RAM blocks and sections.

16.10 Reset

There are multiple reset sources that may trigger a reset of the system. After a reset the CPU can query the RESETREAS (reset reason register) to find out which source generated the reset.

A sub-set of the available GPIOs can be configured as pin reset, see UICR->PSELRESET[0] and UICR->PSELRESET[1] registers for more information on how to configure a GPIO as pin reset.

16.11 Power-on reset

The power-on reset generator initializes the system at power-on. The system is held in reset state until the supply has reached the minimum operating voltage and the internal voltage regulators have started.

16.12 Pin reset

A pin reset is generated when the physical reset pin on the device is asserted.

Pin reset is configured via the *PSELRESET[0]* and *PSELRESET[1]* registers.

16.13 Wakeup from System OFF mode reset

The device is reset when it wakes up from System OFF mode.

The DAP is not reset following a wake up from System OFF mode if the device is in debug interface mode, see *DIF* chapter for more information.

16.14 Soft reset

A soft reset is generated when the SYSRESETREQ bit of the Application Interrupt and Reset Control Register (AIRCR register) in the ARM® core is set.

16.15 Watchdog reset

A Watchdog reset is generated when the watchdog times out. See *WDT* chapter for more information.

16.16 Brown-out reset

The brown-out reset generator puts the system in reset state if the supply voltage drops below the brownout reset threshold.

16.17 Retained registers

A retained register is a register that will retain its value in System OFF mode, and through a reset depending on reset source. See individual peripheral chapters for information of which registers are retained for the different peripherals.

16.18 Reset behavior

Reset source	Reset target CPU	Peripherals	GPIO	Debug[a]	SWJ-DP	RAM	WDT	Retained registers	RESETREAS
CPU lockup [6]	x	x	x						
Soft reset	x	x	x						
Wakeup from System OFF mode reset	x	x		x [7]		x [8]			
Watchdog reset [9]	x	x	x	x		x	x	x	
Pin reset	x	x	x	x		x	x	x	
Brownout reset	x	x	x	x	x	x	x	x	x
Power on reset	x	x	x	x	x	x	x	x	x

Note: The RAM is never reset, but depending on reset source, RAM content may be corrupted.

16.19 Registers

Table 17: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40000000	POWER	POWER	Power Control	

[a] All debug components excluding SWJ-DP, see DIF chapter for more information about the different debug components in the system.

[6] Reset from CPU lockup is disabled if the device is in debug interface mode. CPU lockup is not possible in System OFF.

[7] The Debug components will not be reset if the device is in debug interface mode.

[8] RAM is not reset on wakeup from OFF mode, but depending on settings in the RAM registers parts, or the whole RAM, may not be retained after the device has entered System OFF mode.

[9] Watchdog reset is not available in System OFF.

Table 18: Register Overview

Register	Offset	Description	
TASKS_CONSTLAT	0x078	Enable constant latency mode	
TASKS_LOWPWR	0x07C	Enable low power mode (variable latency)	
EVENTS_POFWARN	0x108	Power failure warning	
EVENTS_SLEEPENTER	0x114	CPU entered WFI/WFE sleep	
EVENTS_SLEEPEXIT	0x118	CPU exited WFI/WFE sleep	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
RESETREAS	0x400	Reset reason	
RAMSTATUS	0x428	RAM status register	Deprecated
SYSTEMOFF	0x500	System OFF register	
POFCON	0x510	Power failure comparator configuration	
GPREGRET	0x51C	General purpose retention register	
GPREGRET2	0x520	General purpose retention register	
RAMON	0x524	RAM on/off register (this register is retained)	Deprecated
RAMONB	0x554	RAM on/off register (this register is retained)	Deprecated
DCDCEN	0x578	DC/DC enable register	
RAM[0].POWER	0x900	RAM0 power control register	
RAM[0].POWERSET	0x904	RAM0 power control set register	
RAM[0].POWERCLR	0x908	RAM0 power control clear register	
RAM[1].POWER	0x910	RAM1 power control register	
RAM[1].POWERSET	0x914	RAM1 power control set register	
RAM[1].POWERCLR	0x918	RAM1 power control clear register	
RAM[2].POWER	0x920	RAM2 power control register	
RAM[2].POWERSET	0x924	RAM2 power control set register	
RAM[2].POWERCLR	0x928	RAM2 power control clear register	
RAM[3].POWER	0x930	RAM3 power control register	
RAM[3].POWERSET	0x934	RAM3 power control set register	
RAM[3].POWERCLR	0x938	RAM3 power control clear register	
RAM[4].POWER	0x940	RAM4 power control register	
RAM[4].POWERSET	0x944	RAM4 power control set register	
RAM[4].POWERCLR	0x948	RAM4 power control clear register	
RAM[5].POWER	0x950	RAM5 power control register	
RAM[5].POWERSET	0x954	RAM5 power control set register	
RAM[5].POWERCLR	0x958	RAM5 power control clear register	
RAM[6].POWER	0x960	RAM6 power control register	
RAM[6].POWERSET	0x964	RAM6 power control set register	
RAM[6].POWERCLR	0x968	RAM6 power control clear register	
RAM[7].POWER	0x970	RAM7 power control register	
RAM[7].POWERSET	0x974	RAM7 power control set register	
RAM[7].POWERCLR	0x978	RAM7 power control clear register	

16.19.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit number																															
Id																										C	B			A		
Reset 0x00000000																										**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	POFWARN			Write '1' to Enable interrupt on *EVENTS_POFWARN* event
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
B	RW	SLEEPENTER			Write '1' to Enable interrupt on *EVENTS_SLEEPENTER* event
			Set	1	Enable

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																													C	B			A		
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Disabled	0																															
			Enabled	1																															
C	RW	SLEEPEXIT																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															

16.19.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																													C	B			A		
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	POFWARN																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	SLEEPENTER																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	SLEEPEXIT																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															

16.19.3 RESETREAS

Address offset: 0x400

Reset reason

Unless cleared, the RESETREAS register will be cumulative. A field is cleared by writing '1' to it. If none of the reset sources are flagged, this indicates that the chip was reset from the on-chip reset generator, which will indicate a power-on-reset or a brownout reset.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																H	G	F	E												D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	RESETPIN																																	
			NotDetected	0																															
			Detected	1																															
B	RW	DOG																																	
			NotDetected	0																															
			Detected	1																															
C	RW	SREQ																																	
			NotDetected	0																															
			Detected	1																															
D	RW	LOCKUP																																	
			NotDetected	0																															
			Detected	1																															
E	RW	OFF																																	

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																H	G	F	E														D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			NotDetected	0																															
			Detected	1																															
F	RW	LPCOMP																																	
			NotDetected	0																															
			Detected	1																															
G	RW	DIF																																	
			NotDetected	0																															
			Detected	1																															
H	RW	NFC																																	
			NotDetected	0																															
			Detected	1																															

16.19.4 RAMSTATUS (Deprecated)

Address offset: 0x428

RAM status register

Since this register is deprecated the following substitutions have been made: RAM block 0 is equivalent to a block comprising RAM0.S0 and RAM1.S0, RAM block 1 is equivalent to a block comprising RAM2.S0 and RAM3.S0, RAM block 2 is equivalent to a block comprising RAM4.S0 and RAM5.S0 and RAM block 3 is equivalent to a block comprising RAM6.S0 and RAM7.S0. A RAM block field will indicate ON as long as any of the RAM sections associated with a block are on.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	RAMBLOCK0																																	
			Off	0																															
			On	1																															
B	R	RAMBLOCK1																																	
			Off	0																															
			On	1																															
C	R	RAMBLOCK2																																	
			Off	0																															
			On	1																															
D	R	RAMBLOCK3																																	
			Off	0																															
			On	1																															

16.19.5 SYSTEMOFF

Address offset: 0x500

System OFF register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	W	SYSTEMOFF																																	
			Enter	1																															

16.19.6 POFCON

Address offset: 0x510

Power failure comparator configuration

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																B	B	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	POF																																	
			Disabled	0																															
			Enabled	1																															
B	RW	THRESHOLD																																	
			V19	6																															
			V20	7																															
			V21	8																															
			V22	9																															
			V23	10																															
			V24	11																															
			V27	14																															
			V28	15																															

16.19.7 GPREGRET

Address offset: 0x51C

General purpose retention register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	GPREGRET																																	

General purpose retention register

This register is a retained register

16.19.8 GPREGRET2

Address offset: 0x520

General purpose retention register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	GPREGRET																																	

General purpose retention register

This register is a retained register

16.19.9 RAMON (Deprecated)

Address offset: 0x524

RAM on/off register (this register is retained)

Since this register is deprecated the following substitutions have been made: RAM block 0 is equivalent to a block comprising RAM0.S0 and RAM1.S0 and RAM block 1 is equivalent to a block comprising RAM2.S0 and RAM3.S0. For new designs it is recommended to use the *RAM[0].POWER* on page 89 and its sibling registers instead.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C																B	A
Reset 0x00000003				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	ONRAM0																																	
			RAM0Off	0																															
			RAM0On	1																															
B	RW	ONRAM1																																	
			RAM1Off	0																															
			RAM1On	1																															
C	RW	OFFRAM0																																	
			RAM0Off	0																															
			RAM0On	1																															
D	RW	OFFRAM1																																	
			RAM1Off	0																															
			RAM1On	1																															

16.19.10 RAMONB (Deprecated)

Address offset: 0x554

RAM on/off register (this register is retained)

Since this register is deprecated the following substitutions have been made: RAM block 2 is equivalent to a block comprising RAM4.S0 and RAM5.S0 and RAM block 3 is equivalent to a block comprising RAM6.S0 and RAM7.S0. For new designs it is recommended to use the *RAM[0].POWER* on page 89 and its sibling registers instead.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C																B	A
Reset 0x00000003				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	ONRAM2																																	
			RAM2Off	0																															
			RAM2On	1																															
B	RW	ONRAM3																																	
			RAM3Off	0																															
			RAM3On	1																															
C	RW	OFFRAM2																																	
			RAM2Off	0																															
			RAM2On	1																															
D	RW	OFFRAM3																																	
			RAM3Off	0																															
			RAM3On	1																															

16.19.11 DCDCEN

Address offset: 0x578

DC/DC enable register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DCDCEN																																	
			Disabled	0																															
			Enabled	1																															

16.19.12 RAM[0].POWER

Address offset: 0x900

RAM0 power control register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C															B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	S0POWER																																	
			Off	0																															
			On	1																															
B	RW	S1POWER																																	
			Off	0																															
			On	1																															
C	RW	S0RETENTION																																	
			Off	0																															
			On	1																															
D	RW	S1RETENTION																																	
			Off	0																															
			On	1																															

16.19.13 RAM[0].POWERSET

Address offset: 0x904

RAM0 power control set register

When read, this register will return the value of the POWER register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C															B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	W	S0POWER																																	
			On	1																															
B	W	S1POWER																																	
			On	1																															
C	W	S0RETENTION																																	
			On	1																															
D	W	S1RETENTION																																	
			On	1																															

16.19.14 RAM[0].POWERCLR

Address offset: 0x908

RAM0 power control clear register

When read, this register will return the value of the POWER register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C															B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	W	S0POWER																																	
			Off	1																															
B	W	S1POWER																																	
			Off	1																															

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				D C B A
Reset 0x0000FFFF				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
C	W	S0RETENTION			Keep retention on RAM section S0 when RAM section is switched off
			Off	1	Off
D	W	S1RETENTION			Keep retention on RAM section S1 when RAM section is switched off
			Off	1	Off

16.19.15 RAM[1].POWER

Address offset: 0x910

RAM1 power control register

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				D C B A
Reset 0x0000FFFF				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	S0POWER			Keep RAM section S0 of RAMm on or off in System ON mode All RAM sections will be switched off in System OFF mode
			Off	0	Off
			On	1	On
B	RW	S1POWER			Keep RAM section S1 of RAMm on or off in System ON mode All RAM sections will be switched off in System OFF mode
			Off	0	Off
			On	1	On
C	RW	S0RETENTION			Keep retention on RAM section S0 when RAM section is switched off
			Off	0	Off
			On	1	On
D	RW	S1RETENTION			Keep retention on RAM section S1 when RAM section is switched off
			Off	0	Off
			On	1	On

16.19.16 RAM[1].POWERSET

Address offset: 0x914

RAM1 power control set register

When read, this register will return the value of the POWER register.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				D C B A
Reset 0x0000FFFF				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	W	S0POWER			Keep RAM section S0 of RAMm on or off in System ON mode
			On	1	On
B	W	S1POWER			Keep RAM section S1 of RAMm on or off in System ON mode
			On	1	On
C	W	S0RETENTION			Keep retention on RAM section S0 when RAM section is switched off
			On	1	On
D	W	S1RETENTION			Keep retention on RAM section S1 when RAM section is switched off
			On	1	On

16.19.17 RAM[1].POWERCLR

Address offset: 0x918

RAM1 power control clear register

When read, this register will return the value of the POWER register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C															B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
				Description																															
A	W	S0POWER																																	
				Keep RAM section S0 of RAMm on or off in System ON mode																															
			Off	1																															
				Off																															
B	W	S1POWER																																	
				Keep RAM section S1 of RAMm on or off in System ON mode																															
			Off	1																															
				Off																															
C	W	S0RETENTION																																	
				Keep retention on RAM section S0 when RAM section is switched off																															
			Off	1																															
				Off																															
D	W	S1RETENTION																																	
				Keep retention on RAM section S1 when RAM section is switched off																															
			Off	1																															
				Off																															

16.19.18 RAM[2].POWER

Address offset: 0x920

RAM2 power control register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C															B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
				Description																															
A	RW	S0POWER																																	
				Keep RAM section S0 of RAMm on or off in System ON mode All RAM sections will be switched off in System OFF mode																															
			Off	0																															
				Off																															
			On	1																															
				On																															
B	RW	S1POWER																																	
				Keep RAM section S1 of RAMm on or off in System ON mode All RAM sections will be switched off in System OFF mode																															
			Off	0																															
				Off																															
			On	1																															
				On																															
C	RW	S0RETENTION																																	
				Keep retention on RAM section S0 when RAM section is switched off																															
			Off	0																															
				Off																															
			On	1																															
				On																															
D	RW	S1RETENTION																																	
				Keep retention on RAM section S1 when RAM section is switched off																															
			Off	0																															
				Off																															
			On	1																															
				On																															

16.19.19 RAM[2].POWERSET

Address offset: 0x924

RAM2 power control set register

When read, this register will return the value of the POWER register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C															B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
				Description																															
A	W	S0POWER																																	
				Keep RAM section S0 of RAMm on or off in System ON mode																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C																B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			On	1																															
B	W	S1POWER																																	
			On	1																															
C	W	S0RETENTION																																	
			On	1																															
D	W	S1RETENTION																																	
			On	1																															

16.19.20 RAM[2].POWERCLR

Address offset: 0x928

RAM2 power control clear register

When read, this register will return the value of the POWER register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C																B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	W	S0POWER																																	
			Off	1																															
B	W	S1POWER																																	
			Off	1																															
C	W	S0RETENTION																																	
			Off	1																															
D	W	S1RETENTION																																	
			Off	1																															

16.19.21 RAM[3].POWER

Address offset: 0x930

RAM3 power control register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C																B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	S0POWER																																	
				All RAM sections will be switched off in System OFF mode																															
			Off	0																															
			On	1																															
B	RW	S1POWER																																	
				All RAM sections will be switched off in System OFF mode																															
			Off	0																															
			On	1																															
C	RW	S0RETENTION																																	
			Off	0																															
			On	1																															
D	RW	S1RETENTION																																	

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C																B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Off	0																															
			On	1																															

16.19.22 RAM[3].POWERSET

Address offset: 0x934

RAM3 power control set register

When read, this register will return the value of the POWER register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C																B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	W	S0POWER																																	
			On	1																															
B	W	S1POWER																																	
			On	1																															
C	W	S0RETENTION																																	
			On	1																															
D	W	S1RETENTION																																	
			On	1																															

16.19.23 RAM[3].POWERCLR

Address offset: 0x938

RAM3 power control clear register

When read, this register will return the value of the POWER register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C																B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	W	S0POWER																																	
			Off	1																															
B	W	S1POWER																																	
			Off	1																															
C	W	S0RETENTION																																	
			Off	1																															
D	W	S1RETENTION																																	
			Off	1																															

16.19.24 RAM[4].POWER

Address offset: 0x940

RAM4 power control register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C																B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	S0POWER																																	
			Off	0																															
			On	1																															
B	RW	S1POWER																																	
			Off	0																															
			On	1																															
C	RW	S0RETENTION																																	
			Off	0																															
			On	1																															
D	RW	S1RETENTION																																	
			Off	0																															
			On	1																															

16.19.25 RAM[4].POWERSET

Address offset: 0x944

RAM4 power control set register

When read, this register will return the value of the POWER register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C																B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	W	S0POWER																																	
			On	1																															
B	W	S1POWER																																	
			On	1																															
C	W	S0RETENTION																																	
			On	1																															
D	W	S1RETENTION																																	
			On	1																															

16.19.26 RAM[4].POWERCLR

Address offset: 0x948

RAM4 power control clear register

When read, this register will return the value of the POWER register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C																B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	W	S0POWER																																	
			Off	1																															
B	W	S1POWER																																	
			Off	1																															

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				D C B A
Reset 0x0000FFFF				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Id	**RW**	**Field**	**Value Id**	**Value** **Description**
C	W	S0RETENTION		Keep retention on RAM section S0 when RAM section is switched off
			Off	1 Off
D	W	S1RETENTION		Keep retention on RAM section S1 when RAM section is switched off
			Off	1 Off

16.19.27 RAM[5].POWER

Address offset: 0x950

RAM5 power control register

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				D C B A
Reset 0x0000FFFF				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Id	**RW**	**Field**	**Value Id**	**Value** **Description**
A	RW	S0POWER		Keep RAM section S0 of RAMm on or off in System ON mode All RAM sections will be switched off in System OFF mode
			Off	0 Off
			On	1 On
B	RW	S1POWER		Keep RAM section S1 of RAMm on or off in System ON mode All RAM sections will be switched off in System OFF mode
			Off	0 Off
			On	1 On
C	RW	S0RETENTION		Keep retention on RAM section S0 when RAM section is switched off
			Off	0 Off
			On	1 On
D	RW	S1RETENTION		Keep retention on RAM section S1 when RAM section is switched off
			Off	0 Off
			On	1 On

16.19.28 RAM[5].POWERSET

Address offset: 0x954

RAM5 power control set register

When read, this register will return the value of the POWER register.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				D C B A
Reset 0x0000FFFF				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Id	**RW**	**Field**	**Value Id**	**Value** **Description**
A	W	S0POWER		Keep RAM section S0 of RAMm on or off in System ON mode
			On	1 On
B	W	S1POWER		Keep RAM section S1 of RAMm on or off in System ON mode
			On	1 On
C	W	S0RETENTION		Keep retention on RAM section S0 when RAM section is switched off
			On	1 On
D	W	S1RETENTION		Keep retention on RAM section S1 when RAM section is switched off
			On	1 On

16.19.29 RAM[5].POWERCLR

Address offset: 0x958

RAM5 power control clear register

When read, this register will return the value of the POWER register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C															B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
				Description																															
A	W	S0POWER																																	
				Keep RAM section S0 of RAMm on or off in System ON mode																															
			Off	1																															
				Off																															
B	W	S1POWER																																	
				Keep RAM section S1 of RAMm on or off in System ON mode																															
			Off	1																															
				Off																															
C	W	S0RETENTION																																	
				Keep retention on RAM section S0 when RAM section is switched off																															
			Off	1																															
				Off																															
D	W	S1RETENTION																																	
				Keep retention on RAM section S1 when RAM section is switched off																															
			Off	1																															
				Off																															

16.19.30 RAM[6].POWER

Address offset: 0x960

RAM6 power control register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C															B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
				Description																															
A	RW	S0POWER																																	
				Keep RAM section S0 of RAMm on or off in System ON mode All RAM sections will be switched off in System OFF mode																															
			Off	0																															
				Off																															
			On	1																															
				On																															
B	RW	S1POWER																																	
				Keep RAM section S1 of RAMm on or off in System ON mode All RAM sections will be switched off in System OFF mode																															
			Off	0																															
				Off																															
			On	1																															
				On																															
C	RW	S0RETENTION																																	
				Keep retention on RAM section S0 when RAM section is switched off																															
			Off	0																															
				Off																															
			On	1																															
				On																															
D	RW	S1RETENTION																																	
				Keep retention on RAM section S1 when RAM section is switched off																															
			Off	0																															
				Off																															
			On	1																															
				On																															

16.19.31 RAM[6].POWERSET

Address offset: 0x964

RAM6 power control set register

When read, this register will return the value of the POWER register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C															B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
				Description																															
A	W	S0POWER																																	
				Keep RAM section S0 of RAMm on or off in System ON mode																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C																B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			On	1																															
B	W	S1POWER																																	
			On	1																															
C	W	S0RETENTION																																	
			On	1																															
D	W	S1RETENTION																																	
			On	1																															

16.19.32 RAM[6].POWERCLR

Address offset: 0x968

RAM6 power control clear register

When read, this register will return the value of the POWER register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C																B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	W	S0POWER																																	
			Off	1																															
B	W	S1POWER																																	
			Off	1																															
C	W	S0RETENTION																																	
			Off	1																															
D	W	S1RETENTION																																	
			Off	1																															

16.19.33 RAM[7].POWER

Address offset: 0x970

RAM7 power control register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C																B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	S0POWER																																	
				All RAM sections will be switched off in System OFF mode																															
			Off	0																															
			On	1																															
B	RW	S1POWER																																	
				All RAM sections will be switched off in System OFF mode																															
			Off	0																															
			On	1																															
C	RW	S0RETENTION																																	
			Off	0																															
			On	1																															
D	RW	S1RETENTION																																	

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C																B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Off	0																															
			On	1																															

16.19.34 RAM[7].POWERSET

Address offset: 0x974

RAM7 power control set register

When read, this register will return the value of the POWER register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C																B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	W	S0POWER																																	
			On	1																															
B	W	S1POWER																																	
			On	1																															
C	W	S0RETENTION																																	
			On	1																															
D	W	S1RETENTION																																	
			On	1																															

16.19.35 RAM[7].POWERCLR

Address offset: 0x978

RAM7 power control clear register

When read, this register will return the value of the POWER register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	C																B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	W	S0POWER																																	
			Off	1																															
B	W	S1POWER																																	
			Off	1																															
C	W	S0RETENTION																																	
			Off	1																															
D	W	S1RETENTION																																	
			Off	1																															

16.20 Electrical Specification

16.20.1 Current consumption, sleep

Symbol	Description	Min.	Typ.	Max.	Units
I_{OFF}	System OFF current, no RAM retention		0.4		µA
I_{ON}	System ON base current, no RAM retention		1.2		µA
I_{RAM}	Additional RAM retention current per 4 KB RAM block		40		nA

16.20.2 Device startup times and transition currents

Symbol	Description	Min.	Typ.	Max.	Units
t_{POR}	Time in Power on Reset after VDD reaches 1.7 V for all supply voltages and temperatures. Dependent on supply rise time.				
$t_{POR,10us}$	VDD rise time 10us		1		ms
$t_{POR,10ms}$	VDD rise time 10ms		9		ms
$t_{POR,60ms}$	VDD rise time 60ms		23		ms
t_{PINR}	If a GPIO pin is configured as reset, the maximum time taken to pull up the pin and release reset after power on reset. Dependent on the pin capacitive load (C)[10]: t=5RC, R = 13kOhm				
$t_{PINR,500nF}$	C = 500nF			32.5	ms
$t_{PINR,10uF}$	C = 10uF			650	ms
t_{R2ON}	Time from reset to ON (CPU execute)				
$t_{R2ON,NOTCONF}$	If reset pin not configured	tPOR			ms
$t_{R2ON,CONF}$	If reset pin configured	tPOR + tPINR			ms
t_{OFF2ON}	Time from OFF to CPU execute		14.65		µs
$t_{IDLE2CPU}$	Time from IDLE to CPU execute		10		µs
$t_{EVTSET,CL1}$	Time from HW event to PPI event in Constant Latency System ON mode				µs
$t_{EVTSET,CL0}$	Time from HW event to PPI event in Low Power System ON mode				µs

16.20.3 Power fail comparator

Symbol	Description	Min.	Typ.	Max.	Units
V_{POF}	Nominal power level warning thresholds (falling supply voltage). Levels are configurable between Min. and Max. in 100mV increments.	1.7		2.8	V
V_{POFTOL}	Threshold voltage tolerance	-1.5		0.6	%
$V_{POFHYST}$	Threshold voltage hysteresis		50		mV
$V_{BOR,OFF}$	Brown out reset voltage range SYSTEM OFF mode	1.2		1.7	V
$V_{BOR,ON}$	Brown out reset voltage range SYSTEM ON mode	1.46		1.58	V

[10] To decrease maximum time a device could hold in reset, a strong external pullup resistor can be used.

17 Clock management (CLOCK)

The advanced clock management system can source the system clocks from a range of internal or external high and low frequency oscillators and distribute them to modules based upon a module's individual requirements. Clock distribution is automated and grouped independently by module to limit current consumption in unused branches of the clock tree.

Listed here are the main features for CLOCK:

- 64 MHz on-chip oscillator
- 64 MHz crystal oscillator, using external 32 MHz crystal
- 32.768 kHz +/-250 ppm RC oscillator
- 32.768 kHz crystal oscillator
- 32.768 kHz synthesized from high frequency oscillator
- FW override control of oscillator activity for low latency start up
- Automatic oscillator and clock control, and distribution for ultra-low power

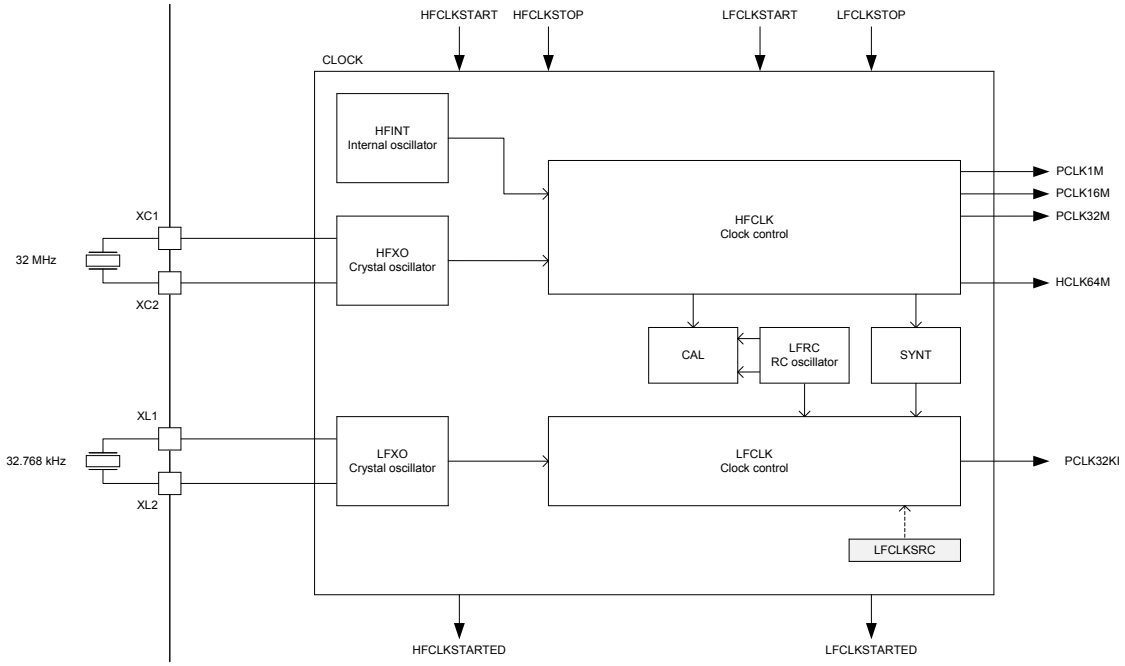

Figure 13: Clock control

17.1 HFCLK clock controller

The system supports the following high frequency clock (HFCLK) sources.

- 64 MHz internal oscillator (HFINT)
- 32 MHz crystal oscillator (HFXO)

For illustration, see *Figure 13: Clock control* on page 101.

The HFCLK clock controller provides the following clocks to the system derived from the HFCLK source:

- HCLK64M: 64 MHz CPU clock
- PCLK1M: 1 MHz peripheral clock
- PCLK16M: 16 MHz peripheral clock
- PCLK32M: 32 MHz peripheral clock

These clocks are only available when the system is in ON mode. When the system enters ON mode, the internal oscillator (HFINT) clock source will automatically start to be able to provide the required HFCLK clock(s) for the system.

The HFINT will be used when HFCLK is requested and HFXO has not been started. The HFXO is started by triggering the HFCLKSTART task and stopped using the HFCLKSTOP task. A HFCLKSTARTED event will be generated when the HFXO has started and its frequency is stable.

If the system does not require any of the clocks provided by the HFCLK clock controller, the HFCLK controller will disable all clock outputs and enter a power saving mode automatically. When one or more of the clocks are requested again, the HFCLK clock controller will resume normal operation.

The HFXO must be running to use the RADIO, NFC module or the calibration mechanism associated with the 32.768 kHz RC oscillator.

17.1.1 32 MHz crystal oscillator (HFXO)

The high frequency crystal oscillator (HFXO) is controlled by a 32 MHz external crystal.

The crystal oscillator is designed for use with an AT-cut quartz crystal in parallel resonant mode. To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet.

Figure 14: Circuit diagram of the 32 MHz crystal oscillator on page 102 shows how the crystal is connected to the 32 MHz crystal oscillator.

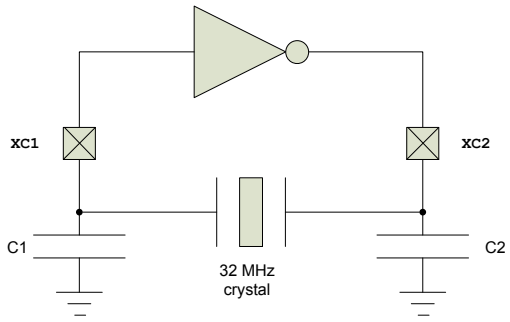

Figure 14: Circuit diagram of the 32 MHz crystal oscillator

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{(C1' \cdot C2')}{(C1' + C2')}$$

$$C1' = C1 + C_{pcb1} + C_{pin}$$
$$C2' = C2 + C_{pcb2} + C_{pin}$$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. C_{pcb1} and C_{pcb2} are stray capacitances on the PCB. C_{pin} is the pin input capacitance on the XC1 and XC2 pins; see table *High Frequency crystal oscillator (HFXO)* on page 108. The load capacitors C1 and C2 should have the same value.

For reliable operation, the crystal load capacitance, shunt capacitance, equivalent series resistance, and drive level must comply with the specifications in table *High Frequency crystal oscillator (HFXO)* on page 108. It is recommended to use a crystal with lower than maximum if the load capacitance and/or shunt capacitance is high. This will give faster start up and lower current consumption. A low load capacitance will reduce both start up time and current consumption.

17.2 LFCLK clock controller

The system supports several low frequency clock sources.

As illustrated in *Figure 13: Clock control* on page 101, the system supports the following low frequency clock sources:

- 32.768 kHz RC oscillator (LFRC)
- 32.768 kHz crystal oscillator (LFXO)
- 32.768 kHz synthesized from HFCLK (LFSYNT)

The LFCLK clock controller and all of the LFCLK clock sources are always switched off when in OFF mode.

The LFCLK clock is started by first selecting the preferred clock source in the LFCLKSRC register and then triggering the LFCLKSTART task. If the selected clock source cannot be started immediately, the 32.768 kHz RC oscillator will start automatically and generate the LFCLK until the selected clock source is available.

The LFCLK clock is stopped by triggering the LFCLKSTOP task. The LFCLKSRC register can only be modified when the LFCLK is not running.

A LFCLKSTARTED event will be generated when the selected LFCLK crystal oscillator has started.

A LFCLKSTOP task will stop the LFCLK oscillator. However, the LFCLKSTOP task can only be triggered after the STATE field in the LFCLKSTAT register indicates a 'LFCLK running' state.

The synthesized 32.768 kHz clock depends on the HFCLK to run. If high accuracy is required for the LFCLK running off the synthesized 32.768 kHz clock, the HFCLK must be generated from the HFCLK crystal oscillator.

17.2.1 32.768 kHz RC oscillator (LFRC)

The default source of the low frequency clock (LFCLK) is the 32.768 kHz RC oscillator (LFRC).

The LFRC frequency will be affected by variation in temperature. The LFRC oscillator can be calibrated to improve accuracy by using the HFXO as a reference oscillator during calibration. See Table *Low frequency RC oscillator (LFRC)* on page 109 for details on the default and calibrated accuracy of the LFRC oscillator. The LFRC oscillator does not require additional external components.

17.2.2 32.768 kHz crystal oscillator (LFXO)

For higher LFCLK accuracy (when better than +/- 250 ppm accuracy is required), the low frequency crystal oscillator (LFXO) must be used.

The 32.768 kHz crystal oscillator requires an external quartz crystal to be connected to the `XL1` and `XL2` pins in parallel resonant mode. To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet, see *Low frequency crystal oscillator (LFXO)* on page 109. The `XL1` and `XL2` share pins with the GPIO.

Figure 15: Circuit diagram of the 32.768 kHz crystal oscillator on page 103 shows LFXO circuitry.

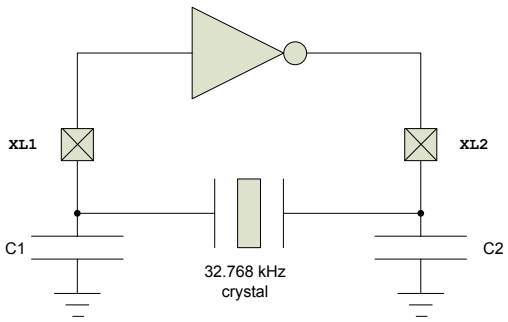

Figure 15: Circuit diagram of the 32.768 kHz crystal oscillator

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{(C1' \cdot C2')}{(C1' + C2')}$$

$$C1' = C1 + C_{pcb1} + C_{pin}$$
$$C2' = C2 + C_{pcb2} + C_{pin}$$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. C_{pcb1} and C_{pcb2} are stray capacitances on the PCB. C_{pin} is the pin input capacitance on the XC1 and XC2 pins. The load capacitors C1 and C2 should have the same value.

17.2.3 32.768 kHz synthesized from HFCLK (LFSYNT)

LFCLK can also be synthesized from the HFCLK clock source. The accuracy of LFCLK will then be the accuracy of the HFCLK.

Using the LFSYNT clock avoids the requirement for a 32.768 kHz crystal, but increases average power consumption as the HFCLK will need to be requested in the system.

17.2.4 External clock references

The LFCLK can be derived from a single-ended external reference at the nominal frequency using the XL pins.

It is also possible to share a 32.768 kHz crystal oscillator as a differential input for the LFCLK reference with another device.

To provide a single-ended externally generated reference for the LFCLK, the XL1 pin is used as input while the XL2 pin must be connected to ground (VSS).

17.2.5 Calibrating the 32.768 kHz RC oscillator

After the 32.768 kHz RC oscillator is started and running, it can be calibrated by triggering the CAL task. The 32.768 kHz RC oscillator will then temporarily request the HFCLK to calibrate itself against.

A DONE event will be generated when calibration has finished. The calibration mechanism will only work as long as HFCLK is generated from the HFCLK crystal oscillator, it is therefore necessary to explicitly start this crystal oscillator before calibration can be started, see HFCLKSTART task. See *Low frequency RC oscillator (LFRC)* on page 109 for recommendations on calibration intervals and crystal accuracy.

17.2.6 Calibration timer

The calibration timer can be used to time the calibration interval of the 32.768 kHz RC oscillator.

The calibration timer is started by triggering the CTSTART task and stopped by triggering the CTSTOP task. The calibration timer will always start counting down from the value specified in CTIV and generate a CTTO timeout event when it reaches 0. The Calibration timer will stop by itself when it reaches 0.

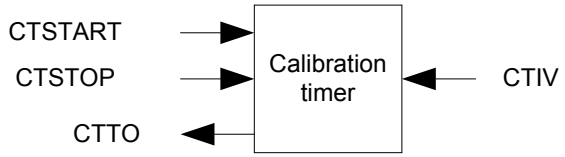

Figure 16: Calibration timer

Due to limitations in the calibration timer, only one task related to calibration, that is, CAL, CTSTART and CTSTOP, can be triggered for every period of LFCLK.

17.3 Registers

Table 19: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40000000	CLOCK	CLOCK	Clock control	

Table 20: Register Overview

Register	Offset	Description
TASKS_HFCLKSTART	0x000	Start HFCLK crystal oscillator
TASKS_HFCLKSTOP	0x004	Stop HFCLK crystal oscillator
TASKS_LFCLKSTART	0x008	Start LFCLK source
TASKS_LFCLKSTOP	0x00C	Stop LFCLK source
TASKS_CAL	0x010	Start calibration of LFRC or LFULP oscillator
TASKS_CTSTART	0x014	Start calibration timer
TASKS_CTSTOP	0x018	Stop calibration timer
EVENTS_HFCLKSTARTED	0x100	HFCLK oscillator started
EVENTS_LFCLKSTARTED	0x104	LFCLK started
EVENTS_DONE	0x10C	Calibration of LFCLK RC oscillator complete event
EVENTS_CTTO	0x110	Calibration timer timeout
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
HFCLKRUN	0x408	Status indicating that HFCLKSTART task has been triggered
HFCLKSTAT	0x40C	HFCLK status
LFCLKRUN	0x414	Status indicating that LFCLKSTART task has been triggered
LFCLKSTAT	0x418	LFCLK status
LFCLKSRCCOPY	0x41C	Copy of LFCLKSRC register, set when LFCLKSTART task was triggered
LFCLKSRC	0x518	Clock source for the LFCLK
CTIV	0x538	Calibration timer interval (retained register, same reset behaviour as RESETREAS)
TRACECONFIG	0x55C	Clocking options for the Trace Port debug interface

17.3.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															D	C		B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																														
A	RW	HFCLKSTARTED			Write '1' to Enable interrupt on *EVENTS_HFCLKSTARTED* event																																
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
B	RW	LFCLKSTARTED			Write '1' to Enable interrupt on *EVENTS_LFCLKSTARTED* event																																
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
C	RW	DONE			Write '1' to Enable interrupt on *EVENTS_DONE* event																																
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
D	RW	CTTO			Write '1' to Enable interrupt on *EVENTS_CTTO* event																																
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														

17.3.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															D	C			B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	HFCLKSTARTED																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	LFCLKSTARTED																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	DONE																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
D	RW	CTTO																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															

17.3.3 HFCLKRUN

Address offset: 0x408

Status indicating that HFCLKSTART task has been triggered

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	STATUS																																	
			NotTriggered	0																															
			Triggered	1																															

17.3.4 HFCLKSTAT

Address offset: 0x40C

HFCLK status

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																			B																A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	SRC																																	
			RC	0																															
			Xtal	1																															
B	R	STATE																																	
			NotRunning	0																															
			Running	1																															

17.3.5 LFCLKRUN

Address offset: 0x414

Status indicating that LFCLKSTART task has been triggered

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	STATUS																																	
			NotTriggered	0																															
			Triggered	1																															

17.3.6 LFCLKSTAT

Address offset: 0x418

LFCLK status

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																			B															A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	SRC																																	
			RC	0																															
			Xtal	1																															
			Synth	2																															
B	R	STATE																																	
			NotRunning	0																															
			Running	1																															

17.3.7 LFCLKSRCCOPY

Address offset: 0x41C

Copy of LFCLKSRC register, set when LFCLKSTART task was triggered

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	SRC																																	
			RC	0																															
			Xtal	1																															
			Synth	2																															

17.3.8 LFCLKSRC

Address offset: 0x518

Clock source for the LFCLK

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	SRC																																	
			RC	0																															
			Xtal	1																															
			Synth	2																															

17.3.9 CTIV

Address offset: 0x538

Calibration timer interval (retained register, same reset behaviour as RESETREAS)

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																										A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	CTIV			Calibration timer interval in multiple of 0.25 seconds. Range: 0.25 seconds to 31.75 seconds.

17.3.10 TRACECONFIG

Address offset: 0x55C

Clocking options for the Trace Port debug interface

This register is a retained register. Reset behavior is the same as debug components.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															B	B															A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TRACEPORTSPEED			Speed of Trace Port clock. Note that the TRACECLK pin will output this clock divided by two.
			32MHz	0	32 MHz Trace Port clock (TRACECLK = 16 MHz)
			16MHz	1	16 MHz Trace Port clock (TRACECLK = 8 MHz)
			8MHz	2	8 MHz Trace Port clock (TRACECLK = 4 MHz)
			4MHz	3	4 MHz Trace Port clock (TRACECLK = 2 MHz)
B	RW	TRACEMUX			Pin multiplexing of trace signals.
			GPIO	0	GPIOs multiplexed onto all trace-pins
			Serial	1	SWO multiplexed onto P0.18, GPIO multiplexed onto other trace pins
			Parallel	2	TRACECLK and TRACEDATA multiplexed onto P0.20, P0.18, P0.16, P0.15 and P0.14.

17.4 Electrical Specification

17.4.1 High frequency internal oscillator(HFINT)

Symbol	Description	Min.	Typ.	Max.	Units
f_{NOM_HFINT}	Nominal frequency		64		MHz
f_{TOL_HFINT}	Frequency tolerance		+-1	+-5	%
I_{HFINT}	Run current		55		uA
I_{START_HFINT}	Average startup current		I_HFINT		uA
t_{START_HFINT}	Startup time		3.2		us

17.4.2 High Frequency crystal oscillator (HFXO)

Symbol	Description	Min.	Typ.	Max.	Units
f_{NOM_HFXO}	Crystal frequency		32		MHz
f_{TOL_HFXO}	Frequency tolerance			+-60	ppm
$f_{TOL\_HFXO\_BLE}$	Frequency tolerance, Bluetooth low energy applications			+-40	ppm
C_{L_HFXO}	Load capacitance			12	pF
C_{0_HFXO}	Shunt capacitance			7	pF
$R_{S\_HFXO\_7PF}$	Equivalent series resistance C0 = 7 pF		30	60	ohm
$R_{S\_HFXO\_5PF}$	Equivalent series resistance C0 = 5 pF		30	80	ohm
$R_{S\_HFXO\_3PF}$	Equivalent series resistance C0 = 3 pF		30	100	ohm
P_{D_HFXO}	Drive level			100	uW
C_{PIN_HFXO}	Input capacitance XC1 and XC2		4		pF

Symbol	Description	Min.	Typ.	Max.	Units
I_{STBY_X32M}	Standby current for 32 MHz crystal oscillator core[11]		50		uA
I_{HFXO}	Run current for 32 MHz crystal oscillator		230		uA
I_{START_HFXO}	Average Startup current for high frequency crystal oscillator, first 1 ms		0.35		mA
t_{START_HFXO}	Startup time for 32 MHz crystal oscillator		0.36	0.5[12]	ms
t_{START_PLL}	Time taken for the PLL to lock the HFINT. Once locked, HFCLK is derived from HFXO		1.3		us

17.4.3 Low frequency crystal oscillator (LFXO)

Symbol	Description	Min.	Typ.	Max.	Units
f_{NOM_LFXO}	Crystal frequency		32.768		kHz
$f_{TOL\_LFXO\_BLE}$	Frequency tolerance for BLE stack			250	ppm
$f_{TOL\_LFXO\_ANT}$	Frequency tolerance for ANT stack			100	ppm
C_{L_LFXO}	Load capacitance		9	12.5	pF
C_{0_LFXO}	Shunt capacitance		1	2	pF
R_{S_LFXO}	Equivalent series resistance		60	100	kohm
P_{D_LFXO}	Drive level			1	uW
C_{pin}	Input capacitance on XL1 and XL2 pads		4		pF
I_{LFXO}	Run current for 32.768 kHz crystal oscillator		0.23		µA
t_{START_LFXO}	Startup time for 32.768 kHz crystal oscillator		0.4		s

17.4.4 Low frequency RC oscillator (LFRC)

Symbol	Description	Min.	Typ.	Max.	Units
f_{NOM_LFRC}	Nominal frequency		32.768		kHz
f_{TOL_LFRC}	Frequency tolerance			+-2	%
$f_{TOL\_CAL\_LFRC}$	Frequency tolerance for LFRC after calibration[13]			250	ppm
I_{LFRC}	Run current for 32.768 kHz RC oscillator	0.5	0.6	0.9	uA
t_{START_LFRC}	Startup time for 32.768 kHz RC oscillator		600		us

17.4.5 Synthesized low frequency clock (LFSYNT)

Symbol	Description	Min.	Typ.	Max.	Units
f_{NOM_LFSYNT}	Nominal frequency		32.768		kHz
f_{TOL_LFSYNT}	Frequency tolerance in addition to HFLCK tolerance[14]		8		ppm
I_{LFSYNT}	Run current for synthesized 32.768 kHz		100		uA
t_{START_LFSYNT}	Startup time for synthesized 32.768 kHz		100		us

[11] Current drawn if HFXO is forced on through for instance using the low latency power mode.

[12] Crystals with other specifications than TSX3225 may have different startup time. Nordic BLE stack implementations have limitations on maximum allowed startup time documented in SoftDevice Specifications.

[13] Constant temperature within ±0.5 °C

[14] Frequency tolerance will be derived from the HFCLK source clock plus the LFSYNT tolerance

18 General purpose input/output (GPIO)

The general purpose input/output (GPIO) is organized as one port with up to 32 I/Os (dependent on package) enabling access and control of up to 32 pins through one port. Each GPIO can be accessed individually.

GPIO has the following user-configurable features:

- up to 32 GPIO
- 8 GPIO with Analog channels for SAADC, COMP or LPCOMP inputs
- Configurable output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high or low level triggers on all pins
- Trigger interrupt on state changes on any pin
- All pins can be used by the PPI task/event system
- One or more GPIO outputs can be controlled through PPI and GPIOTE channels
- All pins can be individually mapped to interfaces blocks for layout flexibility
- GPIO state changes captured on SENSE signal can be stored by LATCH register

The GPIO Port peripheral implements up to 32 pins, `PIN0` through `PIN31`. Each of these pins can be individually configured in the PIN_CNF[n] registers (n=0..31).

The following parameters can be configured through these registers:

- Direction
- Drive strength
- Enabling of pull-up and pull-down resistors
- Pin sensing
- Input buffer disconnect
- Analog input (for selected pins)

The PIN_CNF registers are retained registers. See *POWER* chapter for more information about retained registers.

18.1 Pin configuration

Pins can be individually configured, through the SENSE field in the PIN_CNF[n] register, to detect either a high level or a low level on their input. When the correct level is detected on any such configured pin, the sense mechanism will set the DETECT signal high. Each pin has a separate DETECT signal, and the default behaviour is that the DETECT signal from all pins in the GPIO Port are combined into a common DETECT signal that is routed throughout the system, which then can be utilized by other peripherals, see *Figure 17: GPIO Port and the GPIO pin details* on page 110. This mechanism is functional in both ON and OFF mode.

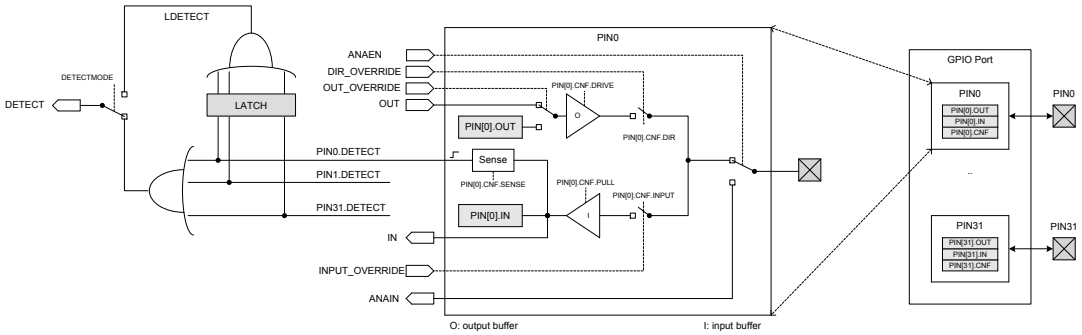

Figure 17: GPIO Port and the GPIO pin details

Figure 17: GPIO Port and the GPIO pin details on page 110 illustrates the GPIO port containing 32 individual pins, where `PIN0` is illustrated in more detail as a reference. All the signals on the left side of the illustration are used by other peripherals in the system, and therefore, are not directly available to the CPU.

Make sure that a pin is in a level that can not trigger the sense mechanism prior to enabling it. Failing to do so may cause a DETECT high to occur (and a PORT event to be fired, see *GPIO tasks and events (GPIOTE)* on page 152) upon enabling sense.

See the following peripherals for more information about how the DETECT signal is used:

- POWER: uses the DETECT signal to exit from System OFF.
- GPIOTE: uses the DETECT signal to generate the PORT event.

When a pin's PINx.DETECT signal goes high, a flag will be set in the LATCH register, e.g. when the PIN0.DETECT signal goes high, bit 0 in the LATCH register will be set to '1'.

The LATCH register will only be cleared if the CPU explicitly clears it by writing a '1' to the bit that shall be cleared, i.e. the LATCH register will not be affected by a PINx.DETECT signal being set low.

If the CPU performs a clear operation on a bit in the LATCH register when the associated PINx.DETECT signal is high, the bit in the LATCH register will not be cleared.

The LDETECT signal will be set high when one or more bits in the LATCH register are '1'. The LDETECT signal will be set low when all bits in the LATCH register are successfully cleared to '0'.

If one or more bits in the LATCH register are '1' after the CPU has performed a clear operation on the LATCH registers, a rising edge will be generated on the LDETECT signal, this is illustrated in *Figure 18: DETECT signal behavior* on page 111.

> **Note:** The CPU can query the LATCH register at any time to check if a SENSE condition has been met on one or more of the the GPIO pins even if that condition is no longer met at the time the CPU queries the LATCH register. This mechanism will work even if the LDETECT signal is not used as the DETECT signal.

The LDETECT signal is by default not connected to the GPIO port's DETECT signal, but via the DETECTMODE register it is possible to change the behaviour of the GPIO port's DETECT signal from the default behaviour described above to instead be derived directly from the LDETECT signal, see *Figure 17: GPIO Port and the GPIO pin details* on page 110. *Figure 18: DETECT signal behavior* on page 111 illustrates the DETECT signals behaviour for these two alternatives.

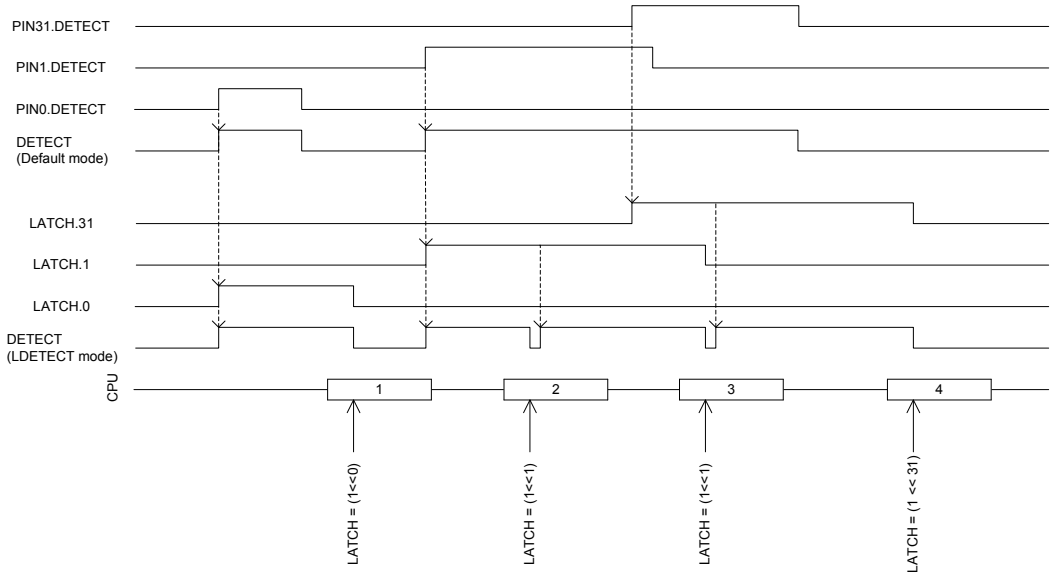

Figure 18: DETECT signal behavior

The input buffer of a GPIO pin can be disconnected from the pin to enable power savings when the pin is not used as an input, see *Figure 17: GPIO Port and the GPIO pin details* on page 110. Inputs must be connected in order to get a valid input value in the IN register and for the sense mechanism to get access to the pin.

Other peripherals in the system can attach themselves to GPIO pins and override their output value and configuration, or read their analog or digital input value, see *Figure 17: GPIO Port and the GPIO pin details* on page 110.

Selected PINs also support analog input signals, see ANAIN in *Figure 17: GPIO Port and the GPIO pin details* on page 110. The assignment of the analog pins can be found in *Pin assignments* on page 27.

> **Note:** When a pin is configured as digital input, care has been taken in the nRF52 design to minimize increased current consumption when the input voltage is between V_{IL} and V_{IH}. However, it is a good practice to ensure that the external circuitry does not drive that pin to levels between V_{IL} and V_{IH} for a long period of time.

18.2 Notes on usage and restrictions

18.2.1 GPIO located near the radio

Radio performance parameters, such as sensitivity, may be affected by high frequency digital I/O with large sink/source current close to the Radio power supply and antenna pins.

Table 21: GPIO recommended usage on page 112 identifies some GPIO that have recommended usage guidelines to maximize Radio performance in an application.

Table 21: GPIO recommended usage

Pin	GPIO	Recommended usage
27	P0.22	Low drive, low frequency I/O only.
28	P0.23	
29	P0.24	
37	P0.25	
38	P0.26	
39	P0.27	
40	P0.28	
41	P0.29	
42	P0.30	
43	P0.31	

18.2.2 NFC antenna pins

Two physical pins can be configures either as NFC antenna pins (factory default) or as GPIOs `P0.09` and `P0.10`.

When configured as NFC antenna pins, the GPIOs on those pins will automatically be set to disable mode and a protection circuit will be enabled preventing the chip being damaged in the presence of a strong NFC field. The protection circuit will short the two pins together if voltage difference exceeds approximately 2 V.

For information on how to configure these pins as normal GPIOs, see *NFCT* and *UICR* chapters. Note that the device will not be protected against strong NFC field damage if the pins are configured as GPIO and a NFC antenna is connected to the device. The pins will always be configured as NFC pins during power on reset until the configuration is set according to the UICR register.

These two pins will have some limitations when configured as GPIO. The pin capacitance will be higher on these pins and there is some current leakage between the two pins if they are driven to different logical values. To avoid leakage between the pins when configured as GPIO, these GPIO should always be at the same logical value whenever entering one of the device power saving modes.

18.3 Registers

Table 22: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x50000000	GPIO	GPIO	General purpose input and output		Deprecated
0x50000000	GPIO	P0	General purpose input and output		

Table 23: Register Overview

Register	Offset	Description
OUT	0x504	Write GPIO port
OUTSET	0x508	Set individual bits in GPIO port
OUTCLR	0x50C	Clear individual bits in GPIO port
IN	0x510	Read GPIO port
DIR	0x514	Direction of GPIO pins
DIRSET	0x518	DIR set register
DIRCLR	0x51C	DIR clear register
LATCH	0x520	Latch indicating which GPIO pins have met the criteria set in PIN_CNF[n].SENSE register
DETECTMODE	0x524	Select between default DETECT signal behaviour and LDETECT mode
PIN_CNF[0]	0x700	Configuration of GPIO pins
PIN_CNF[1]	0x704	Configuration of GPIO pins
PIN_CNF[2]	0x708	Configuration of GPIO pins
PIN_CNF[3]	0x70C	Configuration of GPIO pins
PIN_CNF[4]	0x710	Configuration of GPIO pins
PIN_CNF[5]	0x714	Configuration of GPIO pins
PIN_CNF[6]	0x718	Configuration of GPIO pins
PIN_CNF[7]	0x71C	Configuration of GPIO pins
PIN_CNF[8]	0x720	Configuration of GPIO pins
PIN_CNF[9]	0x724	Configuration of GPIO pins
PIN_CNF[10]	0x728	Configuration of GPIO pins
PIN_CNF[11]	0x72C	Configuration of GPIO pins
PIN_CNF[12]	0x730	Configuration of GPIO pins
PIN_CNF[13]	0x734	Configuration of GPIO pins
PIN_CNF[14]	0x738	Configuration of GPIO pins
PIN_CNF[15]	0x73C	Configuration of GPIO pins
PIN_CNF[16]	0x740	Configuration of GPIO pins
PIN_CNF[17]	0x744	Configuration of GPIO pins
PIN_CNF[18]	0x748	Configuration of GPIO pins
PIN_CNF[19]	0x74C	Configuration of GPIO pins
PIN_CNF[20]	0x750	Configuration of GPIO pins
PIN_CNF[21]	0x754	Configuration of GPIO pins
PIN_CNF[22]	0x758	Configuration of GPIO pins
PIN_CNF[23]	0x75C	Configuration of GPIO pins
PIN_CNF[24]	0x760	Configuration of GPIO pins
PIN_CNF[25]	0x764	Configuration of GPIO pins
PIN_CNF[26]	0x768	Configuration of GPIO pins
PIN_CNF[27]	0x76C	Configuration of GPIO pins
PIN_CNF[28]	0x770	Configuration of GPIO pins
PIN_CNF[29]	0x774	Configuration of GPIO pins
PIN_CNF[30]	0x778	Configuration of GPIO pins
PIN_CNF[31]	0x77C	Configuration of GPIO pins

18.3.1 OUT

Address offset: 0x504

Write GPIO port

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PIN0																																	
			Low	0																															
			High	1																															
B	RW	PIN1																																	
			Low	0																															
			High	1																															
C	RW	PIN2																																	
			Low	0																															
			High	1																															
D	RW	PIN3																																	
			Low	0																															
			High	1																															
E	RW	PIN4																																	
			Low	0																															
			High	1																															
F	RW	PIN5																																	
			Low	0																															
			High	1																															
G	RW	PIN6																																	
			Low	0																															
			High	1																															
H	RW	PIN7																																	
			Low	0																															
			High	1																															
I	RW	PIN8																																	
			Low	0																															
			High	1																															
J	RW	PIN9																																	
			Low	0																															
			High	1																															
K	RW	PIN10																																	
			Low	0																															
			High	1																															
L	RW	PIN11																																	
			Low	0																															
			High	1																															
M	RW	PIN12																																	
			Low	0																															
			High	1																															
N	RW	PIN13																																	
			Low	0																															
			High	1																															
O	RW	PIN14																																	
			Low	0																															
			High	1																															
P	RW	PIN15																																	
			Low	0																															
			High	1																															
Q	RW	PIN16																																	
			Low	0																															
			High	1																															
R	RW	PIN17																																	
			Low	0																															
			High	1																															
S	RW	PIN18																																	

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Low	0																															
			High	1																															
T	RW	PIN19																																	
			Low	0																															
			High	1																															
U	RW	PIN20																																	
			Low	0																															
			High	1																															
V	RW	PIN21																																	
			Low	0																															
			High	1																															
W	RW	PIN22																																	
			Low	0																															
			High	1																															
X	RW	PIN23																																	
			Low	0																															
			High	1																															
Y	RW	PIN24																																	
			Low	0																															
			High	1																															
Z	RW	PIN25																																	
			Low	0																															
			High	1																															
a	RW	PIN26																																	
			Low	0																															
			High	1																															
b	RW	PIN27																																	
			Low	0																															
			High	1																															
c	RW	PIN28																																	
			Low	0																															
			High	1																															
d	RW	PIN29																																	
			Low	0																															
			High	1																															
e	RW	PIN30																																	
			Low	0																															
			High	1																															
f	RW	PIN31																																	
			Low	0																															
			High	1																															

18.3.2 OUTSET

Address offset: 0x508

Set individual bits in GPIO port

Read: reads value of OUT register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PIN0																																	
			Low	0																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			High	1																															
			Set	1																															
B	RW	PIN1																																	
			Low	0																															
			High	1																															
			Set	1																															
C	RW	PIN2																																	
			Low	0																															
			High	1																															
			Set	1																															
D	RW	PIN3																																	
			Low	0																															
			High	1																															
			Set	1																															
E	RW	PIN4																																	
			Low	0																															
			High	1																															
			Set	1																															
F	RW	PIN5																																	
			Low	0																															
			High	1																															
			Set	1																															
G	RW	PIN6																																	
			Low	0																															
			High	1																															
			Set	1																															
H	RW	PIN7																																	
			Low	0																															
			High	1																															
			Set	1																															
I	RW	PIN8																																	
			Low	0																															
			High	1																															
			Set	1																															
J	RW	PIN9																																	
			Low	0																															
			High	1																															
			Set	1																															
K	RW	PIN10																																	
			Low	0																															
			High	1																															
			Set	1																															
L	RW	PIN11																																	
			Low	0																															
			High	1																															
			Set	1																															
M	RW	PIN12																																	
			Low	0																															
			High	1																															
			Set	1																															
N	RW	PIN13																																	
			Low	0																															
			High	1																															
			Set	1																															
O	RW	PIN14																																	

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Low	0																															
			High	1																															
			Set	1																															
P	RW	PIN15																																	
			Low	0																															
			High	1																															
			Set	1																															
Q	RW	PIN16																																	
			Low	0																															
			High	1																															
			Set	1																															
R	RW	PIN17																																	
			Low	0																															
			High	1																															
			Set	1																															
S	RW	PIN18																																	
			Low	0																															
			High	1																															
			Set	1																															
T	RW	PIN19																																	
			Low	0																															
			High	1																															
			Set	1																															
U	RW	PIN20																																	
			Low	0																															
			High	1																															
			Set	1																															
V	RW	PIN21																																	
			Low	0																															
			High	1																															
			Set	1																															
W	RW	PIN22																																	
			Low	0																															
			High	1																															
			Set	1																															
X	RW	PIN23																																	
			Low	0																															
			High	1																															
			Set	1																															
Y	RW	PIN24																																	
			Low	0																															
			High	1																															
			Set	1																															
Z	RW	PIN25																																	
			Low	0																															
			High	1																															
			Set	1																															
a	RW	PIN26																																	
			Low	0																															
			High	1																															
			Set	1																															
b	RW	PIN27																																	
			Low	0																															
			High	1																															
			Set	1																															

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																														
c	RW	PIN28																																
			Low	0																														
			High	1																														
			Set	1																														
d	RW	PIN29																																
			Low	0																														
			High	1																														
			Set	1																														
e	RW	PIN30																																
			Low	0																														
			High	1																														
			Set	1																														
f	RW	PIN31																																
			Low	0																														
			High	1																														
			Set	1																														

18.3.3 OUTCLR

Address offset: 0x50C

Clear individual bits in GPIO port

Read: reads value of OUT register.

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																														
A	RW	PIN0																																
			Low	0																														
			High	1																														
			Clear	1																														
B	RW	PIN1																																
			Low	0																														
			High	1																														
			Clear	1																														
C	RW	PIN2																																
			Low	0																														
			High	1																														
			Clear	1																														
D	RW	PIN3																																
			Low	0																														
			High	1																														
			Clear	1																														
E	RW	PIN4																																
			Low	0																														
			High	1																														
			Clear	1																														
F	RW	PIN5																																
			Low	0																														
			High	1																														
			Clear	1																														
G	RW	PIN6																																
			Low	0																														
			High	1																														

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Clear	1																															
H	RW	PIN7																																	
			Low	0																															
			High	1																															
			Clear	1																															
I	RW	PIN8																																	
			Low	0																															
			High	1																															
			Clear	1																															
J	RW	PIN9																																	
			Low	0																															
			High	1																															
			Clear	1																															
K	RW	PIN10																																	
			Low	0																															
			High	1																															
			Clear	1																															
L	RW	PIN11																																	
			Low	0																															
			High	1																															
			Clear	1																															
M	RW	PIN12																																	
			Low	0																															
			High	1																															
			Clear	1																															
N	RW	PIN13																																	
			Low	0																															
			High	1																															
			Clear	1																															
O	RW	PIN14																																	
			Low	0																															
			High	1																															
			Clear	1																															
P	RW	PIN15																																	
			Low	0																															
			High	1																															
			Clear	1																															
Q	RW	PIN16																																	
			Low	0																															
			High	1																															
			Clear	1																															
R	RW	PIN17																																	
			Low	0																															
			High	1																															
			Clear	1																															
S	RW	PIN18																																	
			Low	0																															
			High	1																															
			Clear	1																															
T	RW	PIN19																																	
			Low	0																															
			High	1																															
			Clear	1																															
U	RW	PIN20																																	
			Low	0																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			High	1																															
			Clear	1																															
V	RW	PIN21																																	
			Low	0																															
			High	1																															
			Clear	1																															
W	RW	PIN22																																	
			Low	0																															
			High	1																															
			Clear	1																															
X	RW	PIN23																																	
			Low	0																															
			High	1																															
			Clear	1																															
Y	RW	PIN24																																	
			Low	0																															
			High	1																															
			Clear	1																															
Z	RW	PIN25																																	
			Low	0																															
			High	1																															
			Clear	1																															
a	RW	PIN26																																	
			Low	0																															
			High	1																															
			Clear	1																															
b	RW	PIN27																																	
			Low	0																															
			High	1																															
			Clear	1																															
c	RW	PIN28																																	
			Low	0																															
			High	1																															
			Clear	1																															
d	RW	PIN29																																	
			Low	0																															
			High	1																															
			Clear	1																															
e	RW	PIN30																																	
			Low	0																															
			High	1																															
			Clear	1																															
f	RW	PIN31																																	
			Low	0																															
			High	1																															
			Clear	1																															

18.3.4 IN

Address offset: 0x510

Read GPIO port

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	PIN0																																	
			Low	0																															
			High	1																															
B	R	PIN1																																	
			Low	0																															
			High	1																															
C	R	PIN2																																	
			Low	0																															
			High	1																															
D	R	PIN3																																	
			Low	0																															
			High	1																															
E	R	PIN4																																	
			Low	0																															
			High	1																															
F	R	PIN5																																	
			Low	0																															
			High	1																															
G	R	PIN6																																	
			Low	0																															
			High	1																															
H	R	PIN7																																	
			Low	0																															
			High	1																															
I	R	PIN8																																	
			Low	0																															
			High	1																															
J	R	PIN9																																	
			Low	0																															
			High	1																															
K	R	PIN10																																	
			Low	0																															
			High	1																															
L	R	PIN11																																	
			Low	0																															
			High	1																															
M	R	PIN12																																	
			Low	0																															
			High	1																															
N	R	PIN13																																	
			Low	0																															
			High	1																															
O	R	PIN14																																	
			Low	0																															
			High	1																															
P	R	PIN15																																	
			Low	0																															
			High	1																															
Q	R	PIN16																																	
			Low	0																															
			High	1																															
R	R	PIN17																																	
			Low	0																															
			High	1																															
S	R	PIN18																																	

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Low	0																															
			High	1																															
T	R	PIN19																																	
			Low	0																															
			High	1																															
U	R	PIN20																																	
			Low	0																															
			High	1																															
V	R	PIN21																																	
			Low	0																															
			High	1																															
W	R	PIN22																																	
			Low	0																															
			High	1																															
X	R	PIN23																																	
			Low	0																															
			High	1																															
Y	R	PIN24																																	
			Low	0																															
			High	1																															
Z	R	PIN25																																	
			Low	0																															
			High	1																															
a	R	PIN26																																	
			Low	0																															
			High	1																															
b	R	PIN27																																	
			Low	0																															
			High	1																															
c	R	PIN28																																	
			Low	0																															
			High	1																															
d	R	PIN29																																	
			Low	0																															
			High	1																															
e	R	PIN30																																	
			Low	0																															
			High	1																															
f	R	PIN31																																	
			Low	0																															
			High	1																															

18.3.5 DIR

Address offset: 0x514

Direction of GPIO pins

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PIN0																																	
			Input	0																															
			Output	1																															
B	RW	PIN1																																	

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Input	0																															
			Output	1																															
C	RW	PIN2																																	
			Input	0																															
			Output	1																															
D	RW	PIN3																																	
			Input	0																															
			Output	1																															
E	RW	PIN4																																	
			Input	0																															
			Output	1																															
F	RW	PIN5																																	
			Input	0																															
			Output	1																															
G	RW	PIN6																																	
			Input	0																															
			Output	1																															
H	RW	PIN7																																	
			Input	0																															
			Output	1																															
I	RW	PIN8																																	
			Input	0																															
			Output	1																															
J	RW	PIN9																																	
			Input	0																															
			Output	1																															
K	RW	PIN10																																	
			Input	0																															
			Output	1																															
L	RW	PIN11																																	
			Input	0																															
			Output	1																															
M	RW	PIN12																																	
			Input	0																															
			Output	1																															
N	RW	PIN13																																	
			Input	0																															
			Output	1																															
O	RW	PIN14																																	
			Input	0																															
			Output	1																															
P	RW	PIN15																																	
			Input	0																															
			Output	1																															
Q	RW	PIN16																																	
			Input	0																															
			Output	1																															
R	RW	PIN17																																	
			Input	0																															
			Output	1																															
S	RW	PIN18																																	
			Input	0																															
			Output	1																															
T	RW	PIN19																																	
			Input	0																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Output	1																															
U	RW	PIN20																																	
			Input	0																															
			Output	1																															
V	RW	PIN21																																	
			Input	0																															
			Output	1																															
W	RW	PIN22																																	
			Input	0																															
			Output	1																															
X	RW	PIN23																																	
			Input	0																															
			Output	1																															
Y	RW	PIN24																																	
			Input	0																															
			Output	1																															
Z	RW	PIN25																																	
			Input	0																															
			Output	1																															
a	RW	PIN26																																	
			Input	0																															
			Output	1																															
b	RW	PIN27																																	
			Input	0																															
			Output	1																															
c	RW	PIN28																																	
			Input	0																															
			Output	1																															
d	RW	PIN29																																	
			Input	0																															
			Output	1																															
e	RW	PIN30																																	
			Input	0																															
			Output	1																															
f	RW	PIN31																																	
			Input	0																															
			Output	1																															

18.3.6 DIRSET

Address offset: 0x518

DIR set register

Read: reads value of DIR register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PIN0																																	
			Input	0																															
			Output	1																															
			Set	1																															
B	RW	PIN1																																	
			Input	0																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Output	1																															
			Set	1																															
C	RW	PIN2																																	
			Input	0																															
			Output	1																															
			Set	1																															
D	RW	PIN3																																	
			Input	0																															
			Output	1																															
			Set	1																															
E	RW	PIN4																																	
			Input	0																															
			Output	1																															
			Set	1																															
F	RW	PIN5																																	
			Input	0																															
			Output	1																															
			Set	1																															
G	RW	PIN6																																	
			Input	0																															
			Output	1																															
			Set	1																															
H	RW	PIN7																																	
			Input	0																															
			Output	1																															
			Set	1																															
I	RW	PIN8																																	
			Input	0																															
			Output	1																															
			Set	1																															
J	RW	PIN9																																	
			Input	0																															
			Output	1																															
			Set	1																															
K	RW	PIN10																																	
			Input	0																															
			Output	1																															
			Set	1																															
L	RW	PIN11																																	
			Input	0																															
			Output	1																															
			Set	1																															
M	RW	PIN12																																	
			Input	0																															
			Output	1																															
			Set	1																															
N	RW	PIN13																																	
			Input	0																															
			Output	1																															
			Set	1																															
O	RW	PIN14																																	
			Input	0																															
			Output	1																															
			Set	1																															
P	RW	PIN15																																	

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Input	0																															
			Output	1																															
			Set	1																															
Q	RW	PIN16																																	
			Input	0																															
			Output	1																															
			Set	1																															
R	RW	PIN17																																	
			Input	0																															
			Output	1																															
			Set	1																															
S	RW	PIN18																																	
			Input	0																															
			Output	1																															
			Set	1																															
T	RW	PIN19																																	
			Input	0																															
			Output	1																															
			Set	1																															
U	RW	PIN20																																	
			Input	0																															
			Output	1																															
			Set	1																															
V	RW	PIN21																																	
			Input	0																															
			Output	1																															
			Set	1																															
W	RW	PIN22																																	
			Input	0																															
			Output	1																															
			Set	1																															
X	RW	PIN23																																	
			Input	0																															
			Output	1																															
			Set	1																															
Y	RW	PIN24																																	
			Input	0																															
			Output	1																															
			Set	1																															
Z	RW	PIN25																																	
			Input	0																															
			Output	1																															
			Set	1																															
a	RW	PIN26																																	
			Input	0																															
			Output	1																															
			Set	1																															
b	RW	PIN27																																	
			Input	0																															
			Output	1																															
			Set	1																															
c	RW	PIN28																																	
			Input	0																															
			Output	1																															
			Set	1																															

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																													
d	RW	PIN29			Set as output pin 29																													
			Input	0	Read: pin set as input																													
			Output	1	Read: pin set as output																													
			Set	1	Write: writing a '1' sets pin to output; writing a '0' has no effect																													
e	RW	PIN30			Set as output pin 30																													
			Input	0	Read: pin set as input																													
			Output	1	Read: pin set as output																													
			Set	1	Write: writing a '1' sets pin to output; writing a '0' has no effect																													
f	RW	PIN31			Set as output pin 31																													
			Input	0	Read: pin set as input																													
			Output	1	Read: pin set as output																													
			Set	1	Write: writing a '1' sets pin to output; writing a '0' has no effect																													

18.3.7 DIRCLR

Address offset: 0x51C

DIR clear register

Read: reads value of DIR register.

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																													
A	RW	PIN0			Set as input pin 0																													
			Input	0	Read: pin set as input																													
			Output	1	Read: pin set as output																													
			Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect																													
B	RW	PIN1			Set as input pin 1																													
			Input	0	Read: pin set as input																													
			Output	1	Read: pin set as output																													
			Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect																													
C	RW	PIN2			Set as input pin 2																													
			Input	0	Read: pin set as input																													
			Output	1	Read: pin set as output																													
			Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect																													
D	RW	PIN3			Set as input pin 3																													
			Input	0	Read: pin set as input																													
			Output	1	Read: pin set as output																													
			Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect																													
E	RW	PIN4			Set as input pin 4																													
			Input	0	Read: pin set as input																													
			Output	1	Read: pin set as output																													
			Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect																													
F	RW	PIN5			Set as input pin 5																													
			Input	0	Read: pin set as input																													
			Output	1	Read: pin set as output																													
			Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect																													
G	RW	PIN6			Set as input pin 6																													
			Input	0	Read: pin set as input																													
			Output	1	Read: pin set as output																													
			Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect																													
H	RW	PIN7			Set as input pin 7																													
			Input	0	Read: pin set as input																													
			Output	1	Read: pin set as output																													

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Clear	1																															
I	RW	PIN8																																	
			Input	0																															
			Output	1																															
			Clear	1																															
J	RW	PIN9																																	
			Input	0																															
			Output	1																															
			Clear	1																															
K	RW	PIN10																																	
			Input	0																															
			Output	1																															
			Clear	1																															
L	RW	PIN11																																	
			Input	0																															
			Output	1																															
			Clear	1																															
M	RW	PIN12																																	
			Input	0																															
			Output	1																															
			Clear	1																															
N	RW	PIN13																																	
			Input	0																															
			Output	1																															
			Clear	1																															
O	RW	PIN14																																	
			Input	0																															
			Output	1																															
			Clear	1																															
P	RW	PIN15																																	
			Input	0																															
			Output	1																															
			Clear	1																															
Q	RW	PIN16																																	
			Input	0																															
			Output	1																															
			Clear	1																															
R	RW	PIN17																																	
			Input	0																															
			Output	1																															
			Clear	1																															
S	RW	PIN18																																	
			Input	0																															
			Output	1																															
			Clear	1																															
T	RW	PIN19																																	
			Input	0																															
			Output	1																															
			Clear	1																															
U	RW	PIN20																																	
			Input	0																															
			Output	1																															
			Clear	1																															
V	RW	PIN21																																	
			Input	0																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Output	1																															
			Clear	1																															
W	RW	PIN22																																	
			Input	0																															
			Output	1																															
			Clear	1																															
X	RW	PIN23																																	
			Input	0																															
			Output	1																															
			Clear	1																															
Y	RW	PIN24																																	
			Input	0																															
			Output	1																															
			Clear	1																															
Z	RW	PIN25																																	
			Input	0																															
			Output	1																															
			Clear	1																															
a	RW	PIN26																																	
			Input	0																															
			Output	1																															
			Clear	1																															
b	RW	PIN27																																	
			Input	0																															
			Output	1																															
			Clear	1																															
c	RW	PIN28																																	
			Input	0																															
			Output	1																															
			Clear	1																															
d	RW	PIN29																																	
			Input	0																															
			Output	1																															
			Clear	1																															
e	RW	PIN30																																	
			Input	0																															
			Output	1																															
			Clear	1																															
f	RW	PIN31																																	
			Input	0																															
			Output	1																															
			Clear	1																															

18.3.8 LATCH

Address offset: 0x520

Latch indicating which GPIO pins have met the criteria set in PIN_CNF[n].SENSE register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	LATCH																																	

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
				The bit position in the register relates to the pin number in the GPIO port, e.g. bit 0 relates to GPIO pin number 0. To clear a bit in the LATCH register the CPU must explicitly write a '1' to that bit.																																	

18.3.9 DETECTMODE

Address offset: 0x524

Select between default DETECT signal behaviour and LDETECT mode

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DETECTMODE																																	Select between default DETECT signal behaviour and LDETECT mode
			Default	0																															Use default behaviour
			LDETECT	1																															Use LDETECT behaviour

18.3.10 PIN_CNF[0]

Address offset: 0x700

Configuration of GPIO pins

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D				C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DIR																																	Pin direction
			Input	0																															Configure pin as an input pin
			Output	1																															Configure pin as an output pin
B	RW	INPUT																																	Connect or disconnect input buffer
			Connect	0																															Connect input buffer
			Disconnect	1																															Disconnect input buffer
C	RW	PULL																																	Pull configuration
			Disabled	0																															No pull
			Pulldown	1																															Pull down on pin
			Pullup	3																															Pull up on pin
D	RW	DRIVE																																	Drive configuration
			S0S1	0																															Standard '0', standard '1'
			H0S1	1																															High drive '0', standard '1'
			S0H1	2																															Standard '0', high drive '1'
			H0H1	3																															High drive '0', high 'drive '1''
			D0S1	4																															Disconnect '0' standard '1'
			D0H1	5																															Disconnect '0', high drive '1'
			S0D1	6																															Standard '0'. disconnect '1'
			H0D1	7																															High drive '0', disconnect '1'
E	RW	SENSE																																	Pin sensing mechanism
			Disabled	0																															Disabled
			High	2																															Sense for high level
			Low	3																															Sense for low level

18.3.11 PIN_CNF[1]

Address offset: 0x704

Configuration of GPIO pins

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D					C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DIR																																	
			Input	0																															
			Output	1																															
B	RW	INPUT																																	
			Connect	0																															
			Disconnect	1																															
C	RW	PULL																																	
			Disabled	0																															
			Pulldown	1																															
			Pullup	3																															
D	RW	DRIVE																																	
			S0S1	0																															
			H0S1	1																															
			S0H1	2																															
			H0H1	3																															
			D0S1	4																															
			D0H1	5																															
			S0D1	6																															
			H0D1	7																															
E	RW	SENSE																																	
			Disabled	0																															
			High	2																															
			Low	3																															

18.3.12 PIN_CNF[2]

Address offset: 0x708

Configuration of GPIO pins

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D					C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DIR																																	
			Input	0																															
			Output	1																															
B	RW	INPUT																																	
			Connect	0																															
			Disconnect	1																															
C	RW	PULL																																	
			Disabled	0																															
			Pulldown	1																															
			Pullup	3																															
D	RW	DRIVE																																	
			S0S1	0																															
			H0S1	1																															
			S0H1	2																															
			H0H1	3																															
			D0S1	4																															
			D0H1	5																															
			S0D1	6																															
			H0D1	7																															
E	RW	SENSE																																	

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Disabled	0																															
			High	2																															
			Low	3																															

18.3.13 PIN_CNF[3]

Address offset: 0x70C

Configuration of GPIO pins

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DIR																																	
			Input	0																															
			Output	1																															
B	RW	INPUT																																	
			Connect	0																															
			Disconnect	1																															
C	RW	PULL																																	
			Disabled	0																															
			Pulldown	1																															
			Pullup	3																															
D	RW	DRIVE																																	
			S0S1	0																															
			H0S1	1																															
			S0H1	2																															
			H0H1	3																															
			D0S1	4																															
			D0H1	5																															
			S0D1	6																															
			H0D1	7																															
E	RW	SENSE																																	
			Disabled	0																															
			High	2																															
			Low	3																															

18.3.14 PIN_CNF[4]

Address offset: 0x710

Configuration of GPIO pins

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DIR																																	
			Input	0																															
			Output	1																															
B	RW	INPUT																																	
			Connect	0																															
			Disconnect	1																															
C	RW	PULL																																	
			Disabled	0																															
			Pulldown	1																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Pullup	3																															
D	RW	DRIVE																																	
			S0S1	0																															
			H0S1	1																															
			S0H1	2																															
			H0H1	3																															
			D0S1	4																															
			D0H1	5																															
			S0D1	6																															
			H0D1	7																															
E	RW	SENSE																																	
			Disabled	0																															
			High	2																															
			Low	3																															

18.3.15 PIN_CNF[5]

Address offset: 0x714

Configuration of GPIO pins

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DIR																																	
			Input	0																															
			Output	1																															
B	RW	INPUT																																	
			Connect	0																															
			Disconnect	1																															
C	RW	PULL																																	
			Disabled	0																															
			Pulldown	1																															
			Pullup	3																															
D	RW	DRIVE																																	
			S0S1	0																															
			H0S1	1																															
			S0H1	2																															
			H0H1	3																															
			D0S1	4																															
			D0H1	5																															
			S0D1	6																															
			H0D1	7																															
E	RW	SENSE																																	
			Disabled	0																															
			High	2																															
			Low	3																															

18.3.16 PIN_CNF[6]

Address offset: 0x718

Configuration of GPIO pins

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																	E	E						D	D	D					C	C	B	A
Reset 0x00000002			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																														**Description**
A	RW	DIR																																Pin direction
			Input	0																														Configure pin as an input pin
			Output	1																														Configure pin as an output pin
B	RW	INPUT																																Connect or disconnect input buffer
			Connect	0																														Connect input buffer
			Disconnect	1																														Disconnect input buffer
C	RW	PULL																																Pull configuration
			Disabled	0																														No pull
			Pulldown	1																														Pull down on pin
			Pullup	3																														Pull up on pin
D	RW	DRIVE																																Drive configuration
			S0S1	0																														Standard '0', standard '1'
			H0S1	1																														High drive '0', standard '1'
			S0H1	2																														Standard '0', high drive '1'
			H0H1	3																														High drive '0', high 'drive '1''
			D0S1	4																														Disconnect '0' standard '1'
			D0H1	5																														Disconnect '0', high drive '1'
			S0D1	6																														Standard '0'. disconnect '1'
			H0D1	7																														High drive '0', disconnect '1'
E	RW	SENSE																																Pin sensing mechanism
			Disabled	0																														Disabled
			High	2																														Sense for high level
			Low	3																														Sense for low level

18.3.17 PIN_CNF[7]

Address offset: 0x71C

Configuration of GPIO pins

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																	E	E						D	D	D					C	C	B	A
Reset 0x00000002			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																														**Description**
A	RW	DIR																																Pin direction
			Input	0																														Configure pin as an input pin
			Output	1																														Configure pin as an output pin
B	RW	INPUT																																Connect or disconnect input buffer
			Connect	0																														Connect input buffer
			Disconnect	1																														Disconnect input buffer
C	RW	PULL																																Pull configuration
			Disabled	0																														No pull
			Pulldown	1																														Pull down on pin
			Pullup	3																														Pull up on pin
D	RW	DRIVE																																Drive configuration
			S0S1	0																														Standard '0', standard '1'
			H0S1	1																														High drive '0', standard '1'
			S0H1	2																														Standard '0', high drive '1'
			H0H1	3																														High drive '0', high 'drive '1''
			D0S1	4																														Disconnect '0' standard '1'
			D0H1	5																														Disconnect '0', high drive '1'
			S0D1	6																														Standard '0'. disconnect '1'
			H0D1	7																														High drive '0', disconnect '1'
E	RW	SENSE																																Pin sensing mechanism
			Disabled	0																														Disabled
			High	2																														Sense for high level

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Low	3																															
			Sense for low level																																

18.3.18 PIN_CNF[8]

Address offset: 0x720

Configuration of GPIO pins

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DIR																																	
			Input	0																															
			Output	1																															
B	RW	INPUT																																	
			Connect	0																															
			Disconnect	1																															
C	RW	PULL																																	
			Disabled	0																															
			Pulldown	1																															
			Pullup	3																															
D	RW	DRIVE																																	
			S0S1	0																															
			H0S1	1																															
			S0H1	2																															
			H0H1	3																															
			D0S1	4																															
			D0H1	5																															
			S0D1	6																															
			H0D1	7																															
E	RW	SENSE																																	
			Disabled	0																															
			High	2																															
			Low	3																															

18.3.19 PIN_CNF[9]

Address offset: 0x724

Configuration of GPIO pins

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DIR																																	
			Input	0																															
			Output	1																															
B	RW	INPUT																																	
			Connect	0																															
			Disconnect	1																															
C	RW	PULL																																	
			Disabled	0																															
			Pulldown	1																															
			Pullup	3																															
D	RW	DRIVE																																	

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			S0S1	0																															
			H0S1	1																															
			S0H1	2																															
			H0H1	3																															
			D0S1	4																															
			D0H1	5																															
			S0D1	6																															
			H0D1	7																															
E	RW	SENSE																																	
			Disabled	0																															
			High	2																															
			Low	3																															

18.3.20 PIN_CNF[10]

Address offset: 0x728

Configuration of GPIO pins

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DIR																																	
			Input	0																															
			Output	1																															
B	RW	INPUT																																	
			Connect	0																															
			Disconnect	1																															
C	RW	PULL																																	
			Disabled	0																															
			Pulldown	1																															
			Pullup	3																															
D	RW	DRIVE																																	
			S0S1	0																															
			H0S1	1																															
			S0H1	2																															
			H0H1	3																															
			D0S1	4																															
			D0H1	5																															
			S0D1	6																															
			H0D1	7																															
E	RW	SENSE																																	
			Disabled	0																															
			High	2																															
			Low	3																															

18.3.21 PIN_CNF[11]

Address offset: 0x72C

Configuration of GPIO pins

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																	E	E						D	D	D					C	C	B	A
Reset 0x00000002			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																														
A	RW	DIR																																
			Input	0																														
			Output	1																														
B	RW	INPUT																																
			Connect	0																														
			Disconnect	1																														
C	RW	PULL																																
			Disabled	0																														
			Pulldown	1																														
			Pullup	3																														
D	RW	DRIVE																																
			S0S1	0																														
			H0S1	1																														
			S0H1	2																														
			H0H1	3																														
			D0S1	4																														
			D0H1	5																														
			S0D1	6																														
			H0D1	7																														
E	RW	SENSE																																
			Disabled	0																														
			High	2																														
			Low	3																														

18.3.22 PIN_CNF[12]

Address offset: 0x730

Configuration of GPIO pins

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																	E	E						D	D	D					C	C	B	A
Reset 0x00000002			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																														
A	RW	DIR																																
			Input	0																														
			Output	1																														
B	RW	INPUT																																
			Connect	0																														
			Disconnect	1																														
C	RW	PULL																																
			Disabled	0																														
			Pulldown	1																														
			Pullup	3																														
D	RW	DRIVE																																
			S0S1	0																														
			H0S1	1																														
			S0H1	2																														
			H0H1	3																														
			D0S1	4																														
			D0H1	5																														
			S0D1	6																														
			H0D1	7																														
E	RW	SENSE																																
			Disabled	0																														
			High	2																														

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Low	3																															
			Sense for low level																																

18.3.23 PIN_CNF[13]

Address offset: 0x734

Configuration of GPIO pins

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DIR																																	
			Input	0																															
			Output	1																															
B	RW	INPUT																																	
			Connect	0																															
			Disconnect	1																															
C	RW	PULL																																	
			Disabled	0																															
			Pulldown	1																															
			Pullup	3																															
D	RW	DRIVE																																	
			S0S1	0																															
			H0S1	1																															
			S0H1	2																															
			H0H1	3																															
			D0S1	4																															
			D0H1	5																															
			S0D1	6																															
			H0D1	7																															
E	RW	SENSE																																	
			Disabled	0																															
			High	2																															
			Low	3																															
			Sense for low level																																

18.3.24 PIN_CNF[14]

Address offset: 0x738

Configuration of GPIO pins

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DIR																																	
			Input	0																															
			Output	1																															
B	RW	INPUT																																	
			Connect	0																															
			Disconnect	1																															
C	RW	PULL																																	
			Disabled	0																															
			Pulldown	1																															
			Pullup	3																															
D	RW	DRIVE																																	

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			S0S1	0																															
			H0S1	1																															
			S0H1	2																															
			H0H1	3																															
			D0S1	4																															
			D0H1	5																															
			S0D1	6																															
			H0D1	7																															
E	RW	SENSE																																	
			Disabled	0																															
			High	2																															
			Low	3																															

18.3.25 PIN_CNF[15]

Address offset: 0x73C

Configuration of GPIO pins

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DIR																																	
			Input	0																															
			Output	1																															
B	RW	INPUT																																	
			Connect	0																															
			Disconnect	1																															
C	RW	PULL																																	
			Disabled	0																															
			Pulldown	1																															
			Pullup	3																															
D	RW	DRIVE																																	
			S0S1	0																															
			H0S1	1																															
			S0H1	2																															
			H0H1	3																															
			D0S1	4																															
			D0H1	5																															
			S0D1	6																															
			H0D1	7																															
E	RW	SENSE																																	
			Disabled	0																															
			High	2																															
			Low	3																															

18.3.26 PIN_CNF[16]

Address offset: 0x740

Configuration of GPIO pins

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																	E	E						D	D	D					C	C	B	A
Reset 0x00000002			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																														**Description**
A	RW	DIR																																Pin direction
			Input	0																														Configure pin as an input pin
			Output	1																														Configure pin as an output pin
B	RW	INPUT																																Connect or disconnect input buffer
			Connect	0																														Connect input buffer
			Disconnect	1																														Disconnect input buffer
C	RW	PULL																																Pull configuration
			Disabled	0																														No pull
			Pulldown	1																														Pull down on pin
			Pullup	3																														Pull up on pin
D	RW	DRIVE																																Drive configuration
			S0S1	0																														Standard '0', standard '1'
			H0S1	1																														High drive '0', standard '1'
			S0H1	2																														Standard '0', high drive '1'
			H0H1	3																														High drive '0', high 'drive '1''
			D0S1	4																														Disconnect '0' standard '1'
			D0H1	5																														Disconnect '0', high drive '1'
			S0D1	6																														Standard '0'. disconnect '1'
			H0D1	7																														High drive '0', disconnect '1'
E	RW	SENSE																																Pin sensing mechanism
			Disabled	0																														Disabled
			High	2																														Sense for high level
			Low	3																														Sense for low level

18.3.27 PIN_CNF[17]

Address offset: 0x744

Configuration of GPIO pins

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																	E	E						D	D	D					C	C	B	A
Reset 0x00000002			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																														**Description**
A	RW	DIR																																Pin direction
			Input	0																														Configure pin as an input pin
			Output	1																														Configure pin as an output pin
B	RW	INPUT																																Connect or disconnect input buffer
			Connect	0																														Connect input buffer
			Disconnect	1																														Disconnect input buffer
C	RW	PULL																																Pull configuration
			Disabled	0																														No pull
			Pulldown	1																														Pull down on pin
			Pullup	3																														Pull up on pin
D	RW	DRIVE																																Drive configuration
			S0S1	0																														Standard '0', standard '1'
			H0S1	1																														High drive '0', standard '1'
			S0H1	2																														Standard '0', high drive '1'
			H0H1	3																														High drive '0', high 'drive '1''
			D0S1	4																														Disconnect '0' standard '1'
			D0H1	5																														Disconnect '0', high drive '1'
			S0D1	6																														Standard '0'. disconnect '1'
			H0D1	7																														High drive '0', disconnect '1'
E	RW	SENSE																																Pin sensing mechanism
			Disabled	0																														Disabled
			High	2																														Sense for high level

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Low	3																															
			Sense for low level																																

18.3.28 PIN_CNF[18]

Address offset: 0x748

Configuration of GPIO pins

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DIR																																	
			Input	0																															
			Output	1																															
B	RW	INPUT																																	
			Connect	0																															
			Disconnect	1																															
C	RW	PULL																																	
			Disabled	0																															
			Pulldown	1																															
			Pullup	3																															
D	RW	DRIVE																																	
			S0S1	0																															
			H0S1	1																															
			S0H1	2																															
			H0H1	3																															
			D0S1	4																															
			D0H1	5																															
			S0D1	6																															
			H0D1	7																															
E	RW	SENSE																																	
			Disabled	0																															
			High	2																															
			Low	3																															
			Sense for low level																																

18.3.29 PIN_CNF[19]

Address offset: 0x74C

Configuration of GPIO pins

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DIR																																	
			Input	0																															
			Output	1																															
B	RW	INPUT																																	
			Connect	0																															
			Disconnect	1																															
C	RW	PULL																																	
			Disabled	0																															
			Pulldown	1																															
			Pullup	3																															
D	RW	DRIVE																																	

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			S0S1	0																															
			H0S1	1																															
			S0H1	2																															
			H0H1	3																															
			D0S1	4																															
			D0H1	5																															
			S0D1	6																															
			H0D1	7																															
E	RW	SENSE																																	
			Disabled	0																															
			High	2																															
			Low	3																															

18.3.30 PIN_CNF[20]

Address offset: 0x750

Configuration of GPIO pins

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DIR																																	
			Input	0																															
			Output	1																															
B	RW	INPUT																																	
			Connect	0																															
			Disconnect	1																															
C	RW	PULL																																	
			Disabled	0																															
			Pulldown	1																															
			Pullup	3																															
D	RW	DRIVE																																	
			S0S1	0																															
			H0S1	1																															
			S0H1	2																															
			H0H1	3																															
			D0S1	4																															
			D0H1	5																															
			S0D1	6																															
			H0D1	7																															
E	RW	SENSE																																	
			Disabled	0																															
			High	2																															
			Low	3																															

18.3.31 PIN_CNF[21]

Address offset: 0x754

Configuration of GPIO pins

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																	E	E						D	D	D					C	C	B	A
Reset 0x00000002			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																														**Description**
A	RW	DIR																																Pin direction
			Input	0																														Configure pin as an input pin
			Output	1																														Configure pin as an output pin
B	RW	INPUT																																Connect or disconnect input buffer
			Connect	0																														Connect input buffer
			Disconnect	1																														Disconnect input buffer
C	RW	PULL																																Pull configuration
			Disabled	0																														No pull
			Pulldown	1																														Pull down on pin
			Pullup	3																														Pull up on pin
D	RW	DRIVE																																Drive configuration
			S0S1	0																														Standard '0', standard '1'
			H0S1	1																														High drive '0', standard '1'
			S0H1	2																														Standard '0', high drive '1'
			H0H1	3																														High drive '0', high 'drive '1''
			D0S1	4																														Disconnect '0' standard '1'
			D0H1	5																														Disconnect '0', high drive '1'
			S0D1	6																														Standard '0'. disconnect '1'
			H0D1	7																														High drive '0', disconnect '1'
E	RW	SENSE																																Pin sensing mechanism
			Disabled	0																														Disabled
			High	2																														Sense for high level
			Low	3																														Sense for low level

18.3.32 PIN_CNF[22]

Address offset: 0x758

Configuration of GPIO pins

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																	E	E						D	D	D					C	C	B	A
Reset 0x00000002			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																														**Description**
A	RW	DIR																																Pin direction
			Input	0																														Configure pin as an input pin
			Output	1																														Configure pin as an output pin
B	RW	INPUT																																Connect or disconnect input buffer
			Connect	0																														Connect input buffer
			Disconnect	1																														Disconnect input buffer
C	RW	PULL																																Pull configuration
			Disabled	0																														No pull
			Pulldown	1																														Pull down on pin
			Pullup	3																														Pull up on pin
D	RW	DRIVE																																Drive configuration
			S0S1	0																														Standard '0', standard '1'
			H0S1	1																														High drive '0', standard '1'
			S0H1	2																														Standard '0', high drive '1'
			H0H1	3																														High drive '0', high 'drive '1''
			D0S1	4																														Disconnect '0' standard '1'
			D0H1	5																														Disconnect '0', high drive '1'
			S0D1	6																														Standard '0'. disconnect '1'
			H0D1	7																														High drive '0', disconnect '1'
E	RW	SENSE																																Pin sensing mechanism
			Disabled	0																														Disabled
			High	2																														Sense for high level

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Low	3																															
			Sense for low level																																

18.3.33 PIN_CNF[23]

Address offset: 0x75C

Configuration of GPIO pins

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DIR																																	
			Input	0																															
			Output	1																															
B	RW	INPUT																																	
			Connect	0																															
			Disconnect	1																															
C	RW	PULL																																	
			Disabled	0																															
			Pulldown	1																															
			Pullup	3																															
D	RW	DRIVE																																	
			S0S1	0																															
			H0S1	1																															
			S0H1	2																															
			H0H1	3																															
			D0S1	4																															
			D0H1	5																															
			S0D1	6																															
			H0D1	7																															
E	RW	SENSE																																	
			Disabled	0																															
			High	2																															
			Low	3																															
			Sense for low level																																

18.3.34 PIN_CNF[24]

Address offset: 0x760

Configuration of GPIO pins

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DIR																																	
			Input	0																															
			Output	1																															
B	RW	INPUT																																	
			Connect	0																															
			Disconnect	1																															
C	RW	PULL																																	
			Disabled	0																															
			Pulldown	1																															
			Pullup	3																															
D	RW	DRIVE																																	

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			S0S1	0																															
			H0S1	1																															
			S0H1	2																															
			H0H1	3																															
			D0S1	4																															
			D0H1	5																															
			S0D1	6																															
			H0D1	7																															
E	RW	SENSE																																	
			Disabled	0																															
			High	2																															
			Low	3																															

18.3.35 PIN_CNF[25]

Address offset: 0x764

Configuration of GPIO pins

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DIR																																	
			Input	0																															
			Output	1																															
B	RW	INPUT																																	
			Connect	0																															
			Disconnect	1																															
C	RW	PULL																																	
			Disabled	0																															
			Pulldown	1																															
			Pullup	3																															
D	RW	DRIVE																																	
			S0S1	0																															
			H0S1	1																															
			S0H1	2																															
			H0H1	3																															
			D0S1	4																															
			D0H1	5																															
			S0D1	6																															
			H0D1	7																															
E	RW	SENSE																																	
			Disabled	0																															
			High	2																															
			Low	3																															

18.3.36 PIN_CNF[26]

Address offset: 0x768

Configuration of GPIO pins

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																	E	E						D	D	D					C	C	B	A
Reset 0x00000002			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																														**Description**
A	RW	DIR																																Pin direction
			Input	0																														Configure pin as an input pin
			Output	1																														Configure pin as an output pin
B	RW	INPUT																																Connect or disconnect input buffer
			Connect	0																														Connect input buffer
			Disconnect	1																														Disconnect input buffer
C	RW	PULL																																Pull configuration
			Disabled	0																														No pull
			Pulldown	1																														Pull down on pin
			Pullup	3																														Pull up on pin
D	RW	DRIVE																																Drive configuration
			S0S1	0																														Standard '0', standard '1'
			H0S1	1																														High drive '0', standard '1'
			S0H1	2																														Standard '0', high drive '1'
			H0H1	3																														High drive '0', high 'drive '1''
			D0S1	4																														Disconnect '0' standard '1'
			D0H1	5																														Disconnect '0', high drive '1'
			S0D1	6																														Standard '0'. disconnect '1'
			H0D1	7																														High drive '0', disconnect '1'
E	RW	SENSE																																Pin sensing mechanism
			Disabled	0																														Disabled
			High	2																														Sense for high level
			Low	3																														Sense for low level

18.3.37 PIN_CNF[27]

Address offset: 0x76C

Configuration of GPIO pins

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																	E	E						D	D	D					C	C	B	A
Reset 0x00000002			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																														**Description**
A	RW	DIR																																Pin direction
			Input	0																														Configure pin as an input pin
			Output	1																														Configure pin as an output pin
B	RW	INPUT																																Connect or disconnect input buffer
			Connect	0																														Connect input buffer
			Disconnect	1																														Disconnect input buffer
C	RW	PULL																																Pull configuration
			Disabled	0																														No pull
			Pulldown	1																														Pull down on pin
			Pullup	3																														Pull up on pin
D	RW	DRIVE																																Drive configuration
			S0S1	0																														Standard '0', standard '1'
			H0S1	1																														High drive '0', standard '1'
			S0H1	2																														Standard '0', high drive '1'
			H0H1	3																														High drive '0', high 'drive '1''
			D0S1	4																														Disconnect '0' standard '1'
			D0H1	5																														Disconnect '0', high drive '1'
			S0D1	6																														Standard '0'. disconnect '1'
			H0D1	7																														High drive '0', disconnect '1'
E	RW	SENSE																																Pin sensing mechanism
			Disabled	0																														Disabled
			High	2																														Sense for high level

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Low	3																															
			Sense for low level																																

18.3.38 PIN_CNF[28]

Address offset: 0x770

Configuration of GPIO pins

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DIR																																	
			Input	0																															
			Output	1																															
B	RW	INPUT																																	
			Connect	0																															
			Disconnect	1																															
C	RW	PULL																																	
			Disabled	0																															
			Pulldown	1																															
			Pullup	3																															
D	RW	DRIVE																																	
			S0S1	0																															
			H0S1	1																															
			S0H1	2																															
			H0H1	3																															
			D0S1	4																															
			D0H1	5																															
			S0D1	6																															
			H0D1	7																															
E	RW	SENSE																																	
			Disabled	0																															
			High	2																															
			Low	3																															
			Sense for low level																																

18.3.39 PIN_CNF[29]

Address offset: 0x774

Configuration of GPIO pins

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D						C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DIR																																	
			Input	0																															
			Output	1																															
B	RW	INPUT																																	
			Connect	0																															
			Disconnect	1																															
C	RW	PULL																																	
			Disabled	0																															
			Pulldown	1																															
			Pullup	3																															
D	RW	DRIVE																																	

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																	E	E						D	D	D					C	C	B	A
Reset 0x00000002			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																													
			S0S1	0	Standard '0', standard '1'																													
			H0S1	1	High drive '0', standard '1'																													
			S0H1	2	Standard '0', high drive '1'																													
			H0H1	3	High drive '0', high 'drive '1''																													
			D0S1	4	Disconnect '0' standard '1'																													
			D0H1	5	Disconnect '0', high drive '1'																													
			S0D1	6	Standard '0'. disconnect '1'																													
			H0D1	7	High drive '0', disconnect '1'																													
E	RW	SENSE			Pin sensing mechanism																													
			Disabled	0	Disabled																													
			High	2	Sense for high level																													
			Low	3	Sense for low level																													

18.3.40 PIN_CNF[30]

Address offset: 0x778

Configuration of GPIO pins

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																	E	E						D	D	D					C	C	B	A
Reset 0x00000002			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																													
A	RW	DIR			Pin direction																													
			Input	0	Configure pin as an input pin																													
			Output	1	Configure pin as an output pin																													
B	RW	INPUT			Connect or disconnect input buffer																													
			Connect	0	Connect input buffer																													
			Disconnect	1	Disconnect input buffer																													
C	RW	PULL			Pull configuration																													
			Disabled	0	No pull																													
			Pulldown	1	Pull down on pin																													
			Pullup	3	Pull up on pin																													
D	RW	DRIVE			Drive configuration																													
			S0S1	0	Standard '0', standard '1'																													
			H0S1	1	High drive '0', standard '1'																													
			S0H1	2	Standard '0', high drive '1'																													
			H0H1	3	High drive '0', high 'drive '1''																													
			D0S1	4	Disconnect '0' standard '1'																													
			D0H1	5	Disconnect '0', high drive '1'																													
			S0D1	6	Standard '0'. disconnect '1'																													
			H0D1	7	High drive '0', disconnect '1'																													
E	RW	SENSE			Pin sensing mechanism																													
			Disabled	0	Disabled																													
			High	2	Sense for high level																													
			Low	3	Sense for low level																													

18.3.41 PIN_CNF[31]

Address offset: 0x77C

Configuration of GPIO pins

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E	E						D	D	D					C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DIR																																	
			Input	0																															
			Output	1																															
B	RW	INPUT																																	
			Connect	0																															
			Disconnect	1																															
C	RW	PULL																																	
			Disabled	0																															
			Pulldown	1																															
			Pullup	3																															
D	RW	DRIVE																																	
			S0S1	0																															
			H0S1	1																															
			S0H1	2																															
			H0H1	3																															
			D0S1	4																															
			D0H1	5																															
			S0D1	6																															
			H0D1	7																															
E	RW	SENSE																																	
			Disabled	0																															
			High	2																															
			Low	3																															

18.4 Electrical Specification

18.4.1 GPIO Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage	0.7 x VDD		VDD	V
V_{IL}	Input low voltage	VSS		0.3 x VDD	V
$V_{OH,SD}$	Output high voltage, standard drive, 0.5 mA	VDD-0.4		VDD	V
$V_{OH,HDH}$	Output high voltage, high drive, 5 mA, VDD >= 2.7 V	VDD-0.4		VDD	V
$V_{OH,HDL}$	Output high voltage, high drive, 3 mA, VDD >= 1.7 V	VDD-0.4		VDD	V
$V_{OL,SD}$	Output low voltage, standard drive, 0.5 mA	VSS		VSS+0.4	V
$V_{OL,HDH}$	Output low voltage, high drive, 5 mA, VDD >= 2.7 V	VSS		VSS+0.4	V
$V_{OL,HDL}$	Output low voltage, high drive, 3 mA, VDD >= 1.7 V	VSS		VSS+0.4	V
I_{SSNK}	Short current, standard drive			15	mA
I_{HSNK}	Short current, high drive			50	mA
$I_{OL,SD}$	Current at VSS+0.4 V, output set low, standard drive	1	2	4	mA
$I_{OL,HDH}$	Current at VSS+0.4 V, output set low, high drive, VDD >= 2.7 V	6	10	15	mA
$I_{OL,HDL}$	Current at VSS+0.4 V, output set low, high drive, VDD >= 1.7 V	3			mA
$I_{OH,SD}$	Current at VDD-0.4 V, output set high, standard drive	1	2	4	mA
$I_{OH,HDH}$	Current at VDD-0.4 V, output set high, high drive, VDD >= 2.7 V	6	9	14	mA
$I_{OH,HDL}$	Current at VDD-0.4 V, output set high, high drive, VDD >= 1.7 V	3			mA
$t_{RF,15pF}$	Rise/fall time, low drive mode, 10-90%, 15 pF load[1]	6	9	19	ns
$t_{RF,25pF}$	Rise/fall time, low drive mode, 10-90%, 25 pF load[1]	10	13	30	ns
$t_{RF,50pF}$	Rise/fall time, low drive mode, 10-90%, 50 pF load[1]	18	25	61	ns
$t_{HRF,15pF}$	Rise/Fall time, high drive mode, 10-90%, 15 pF load[1]	2	4	8	ns
$t_{HRF,25pF}$	Rise/Fall time, high drive mode, 10-90%, 25 pF load[1]	3	5	11	ns
$t_{HRF,50pF}$	Rise/Fall time, high drive mode, 10-90%, 50 pF load[1]	5	8	19	ns

[1] Rise and fall times based on simulations

Symbol	Description	Min.	Typ.	Max.	Units
R_{PU}	Pull-up resistance	11	13	16	kΩ
R_{PD}	Pull-down resistance	11	13	16	kΩ
C_{PAD}	Pad capacitance		3		pF
C_{PAD_NFC}	Pad capacitance on NFC pads		4		pF
I_{NFC_LEAK}	Leakage current between NFC pads when driven to different states		1	4	uA

The current drawn from the battery when GPIO is active as an output is calculated as follows:

$I_{GPIO}=V_{DD}\ C_{load}\ f$

C_{load} being the load capacitance and "f" is the switching frequency.

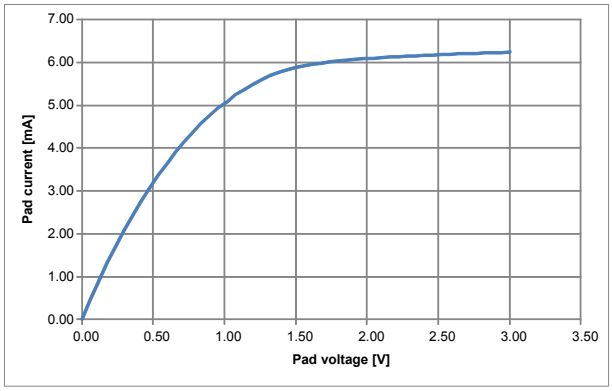

Figure 19: GPIO drive strength vs Voltage, standard drive

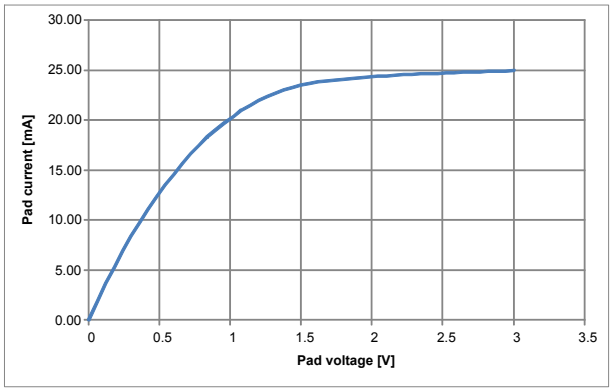

Figure 20: GPIO drive strength vs Voltage, high drive

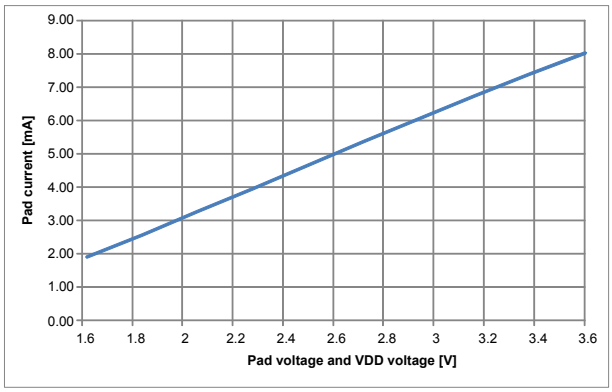

Figure 21: Max sink current vs Voltage, standard drive

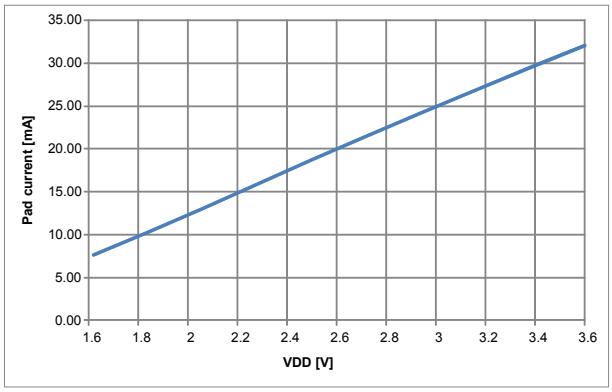

Figure 22: Max sink current vs Voltage, high drive

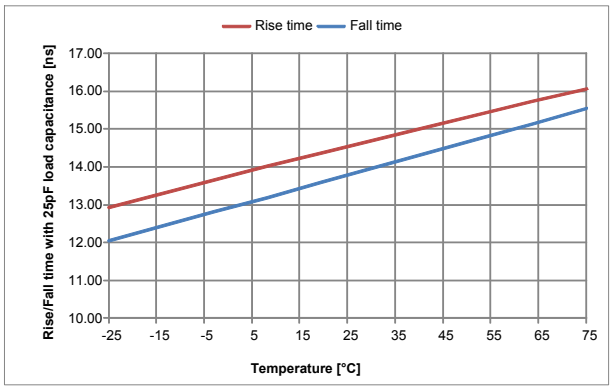

Figure 23: Rise and fall time vs Temperature

19 GPIO tasks and events (GPIOTE)

The GPIO tasks and events (GPIOTE) module provides functionality for accessing GPIO pins using tasks and events. Each GPIOTE channel can be assigned to one pin.

A GPIOTE block enables GPIOs on Port 0 to generate events on pin state change which can be used to carry out tasks through the PPI system. A GPIO can also be driven to change state on system events using the PPI system. Low power detection of pin state changes on Port 0 is possible when in System ON or System OFF.

Table 24: GPIOTE properties

Instance	Number of GPIOTE channels
GPIOTE	8

Up to three tasks can be used in each GPIOTE channel for performing write operations to a pin. Two tasks are fixed (SET and CLR), and one is configurable to perform following operations:

- Set
- Clear
- Toggle

An event can be generated in each GPIOTE channel from one of the following input conditions:

- Rising edge
- Falling edge
- Any change

19.1 Pin events and tasks

The GPIOTE module has a number of tasks and events that can be configured to operate on individual GPIO pins.

The tasks (SET[n], CLR[n] and OUT[n]) can be used for writing to individual pins, and the events (IN[n]) can be generated from changes occurring at the inputs of individual pins.

The SET task will set the pin selected in CONFIG[n].PSEL to high.

The CLR task will set the pin low.

The effect of the OUT task on the pin is configurable in CONFIG[n].POLARITY , and can either set the pin high, set it low, or toggle it.

The tasks and events are configured using the CONFIG[n] registers. Every set of SET, CLR and OUT[n] tasks and IN[n] events has one CONFIG[n] register associated with it.

As long as a SET[n], CLR[n] and OUT[n] task or an IN[n] event is configured to control a pin **n**, the pin's output value will only be updated by the GPIOTE module. The pin's output value as specified in the GPIO will therefore be ignored as long as the pin is controlled by GPIOTE. Attempting to write a pin as a normal GPIO pin will have no effect. When the GPIOTE is disconnected from a pin, see MODE field in CONFIG[n] register, the associated pin will get the output and configuration values specified in the GPIO module.

When conflicting tasks are triggered simultaneously (i.e. during the same clock cycle) in one channel, priorities are defined in *Table 25: Task priorities: resulting GPIO state upon two conflicting tasks* on page 152 below.

Priorities in situations not documented in the table are to be considered as undefined.

Table 25: Task priorities: resulting GPIO state upon two conflicting tasks

1st task	2nd task	GPIO result
OUT None	CLR	No change
OUT None	SET	No change
OUT LoToHi	CLR	High

1st task	2nd task	GPIO result
OUT LoToHi	SET	High
OUT HiToLo	CLR	Low
OUT HiToLo	SET	Low
CLR	SET	Low

When setting the CONFIG[n] registers, MODE=Disabled does not have the same effect as MODE=Task and POLARITY=None. In the latter case, a CLR or SET task occurring at the exact same time as OUT will end up with no change on the pin, see the table above.

When a GPIOTE channel is configured to operate on a pin as a task, the initial value of that pin is configured in the OUTINIT field of CONFIG[n].

19.2 Port event

PORT is an event that can be generated from multiple input pins using the GPIO DETECT signal.

The event will be generated on the rising edge of the DETECT signal. See *GPIO* chapter for more information about the DETECT signal.

Trying to put the system to sleep while DETECT is high will not wake the system up again. Make sure to clear all DETECT sources prior to entering sleep. If the LATCH register is used as a source, if any bit in LATCH is still high after clearing all or part of the register(for instance due to one of the PINx.DETECT signal still high), a new rising edge will be generated on DETECT, see *Figure 18: DETECT signal behavior* on page 111

Trying to put the system to off while DETECT is high will wake up the system immediately.

This feature is always enabled although the peripheral itself appears to be IDLE, that is, no clocks or other power intensive infrastructure have to be requested to keep this feature enabled. This feature can therefore be used to wake up the CPU from a WFI or WFE type sleep in System ON with all peripherals and the CPU idle, that is, lowest power consumption in System ON mode.

> **Note:** In order to prevent spurious interrupts from the PORT event while configuring the sources, the user shall first disable interrupts on the PORT event (through INTENCLR.PORT), then configure the sources (PIN_CNF[n].SENSE), clear any potential event that could have occurred during configuration (write '1' to EVENTS_PORT), and finally enable interrupts (through INTENSET.PORT).

19.3 Tasks and events pin configuration

Each GPIOTE channel is associated with one physical GPIO pin through the CONFIG.PSEL field.

When Event mode is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will be configured as an input, overriding the setting in GPIO. Similarly, when Task mode is selected in CONFIG.MODE the pin specified by CONFIG.PSEL will be configured as an output, overriding the setting in GPIO. When Disabled is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will use its configuration from the PIN[n].CNF registers in GPIO.

Only one GPIOTE channel can be assigned to one physical pin. Failing to do so may result in unpredictable behavior.

19.4 Registers

Table 26: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40006000	GPIOTE	GPIOTE	GPIO tasks and events	

Table 27: Register Overview

Register	Offset	Description
TASKS_OUT[0]	0x000	Task for writing to pin specified in CONFIG[0].PSEL. Action on pin is configured in CONFIG[0].POLARITY.
TASKS_OUT[1]	0x004	Task for writing to pin specified in CONFIG[1].PSEL. Action on pin is configured in CONFIG[1].POLARITY.
TASKS_OUT[2]	0x008	Task for writing to pin specified in CONFIG[2].PSEL. Action on pin is configured in CONFIG[2].POLARITY.
TASKS_OUT[3]	0x00C	Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is configured in CONFIG[3].POLARITY.
TASKS_OUT[4]	0x010	Task for writing to pin specified in CONFIG[4].PSEL. Action on pin is configured in CONFIG[4].POLARITY.
TASKS_OUT[5]	0x014	Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is configured in CONFIG[5].POLARITY.
TASKS_OUT[6]	0x018	Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is configured in CONFIG[6].POLARITY.
TASKS_OUT[7]	0x01C	Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is configured in CONFIG[7].POLARITY.
TASKS_SET[0]	0x030	Task for writing to pin specified in CONFIG[0].PSEL. Action on pin is to set it high.
TASKS_SET[1]	0x034	Task for writing to pin specified in CONFIG[1].PSEL. Action on pin is to set it high.
TASKS_SET[2]	0x038	Task for writing to pin specified in CONFIG[2].PSEL. Action on pin is to set it high.
TASKS_SET[3]	0x03C	Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is to set it high.
TASKS_SET[4]	0x040	Task for writing to pin specified in CONFIG[4].PSEL. Action on pin is to set it high.
TASKS_SET[5]	0x044	Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is to set it high.
TASKS_SET[6]	0x048	Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it high.
TASKS_SET[7]	0x04C	Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it high.
TASKS_CLR[0]	0x060	Task for writing to pin specified in CONFIG[0].PSEL. Action on pin is to set it low.
TASKS_CLR[1]	0x064	Task for writing to pin specified in CONFIG[1].PSEL. Action on pin is to set it low.
TASKS_CLR[2]	0x068	Task for writing to pin specified in CONFIG[2].PSEL. Action on pin is to set it low.
TASKS_CLR[3]	0x06C	Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is to set it low.
TASKS_CLR[4]	0x070	Task for writing to pin specified in CONFIG[4].PSEL. Action on pin is to set it low.
TASKS_CLR[5]	0x074	Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is to set it low.
TASKS_CLR[6]	0x078	Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low.
TASKS_CLR[7]	0x07C	Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it low.
EVENTS_IN[0]	0x100	Event generated from pin specified in CONFIG[0].PSEL
EVENTS_IN[1]	0x104	Event generated from pin specified in CONFIG[1].PSEL
EVENTS_IN[2]	0x108	Event generated from pin specified in CONFIG[2].PSEL
EVENTS_IN[3]	0x10C	Event generated from pin specified in CONFIG[3].PSEL
EVENTS_IN[4]	0x110	Event generated from pin specified in CONFIG[4].PSEL
EVENTS_IN[5]	0x114	Event generated from pin specified in CONFIG[5].PSEL
EVENTS_IN[6]	0x118	Event generated from pin specified in CONFIG[6].PSEL
EVENTS_IN[7]	0x11C	Event generated from pin specified in CONFIG[7].PSEL
EVENTS_PORT	0x17C	Event generated from multiple input GPIO pins with SENSE mechanism enabled
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
CONFIG[0]	0x510	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[1]	0x514	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[2]	0x518	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[3]	0x51C	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[4]	0x520	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[5]	0x524	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[6]	0x528	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[7]	0x52C	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

19.4.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				I																								H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
A	RW	IN0																										Write '1' to Enable interrupt on *EVENTS_IN[0]* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
B	RW	IN1																										Write '1' to Enable interrupt on *EVENTS_IN[1]* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
C	RW	IN2																										Write '1' to Enable interrupt on *EVENTS_IN[2]* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
D	RW	IN3																										Write '1' to Enable interrupt on *EVENTS_IN[3]* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
E	RW	IN4																										Write '1' to Enable interrupt on *EVENTS_IN[4]* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
F	RW	IN5																										Write '1' to Enable interrupt on *EVENTS_IN[5]* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
G	RW	IN6																										Write '1' to Enable interrupt on *EVENTS_IN[6]* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
H	RW	IN7																										Write '1' to Enable interrupt on *EVENTS_IN[7]* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
I	RW	PORT																										Write '1' to Enable interrupt on *EVENTS_PORT* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							

19.4.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				I																								H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
A	RW	IN0																										Write '1' to Disable interrupt on *EVENTS_IN[0]* event							
			Clear	1																								Disable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
B	RW	IN1																										Write '1' to Disable interrupt on *EVENTS_IN[1]* event							
			Clear	1																								Disable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
C	RW	IN2																										Write '1' to Disable interrupt on *EVENTS_IN[2]* event							

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				I																								H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
D	RW	IN3																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
E	RW	IN4																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
F	RW	IN5																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
G	RW	IN6																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
H	RW	IN7																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
I	RW	PORT																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															

19.4.3 CONFIG[0]

Address offset: 0x510

Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															D			C	C				B	B	B	B							A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	MODE																																	
			Disabled	0																															
			Event	1																															
			Task	3																															
B	RW	PSEL		[0..31]																															

Disabled. Pin specified by PSEL will not be acquired by the GPIOTE module.

Event mode

The pin specified by PSEL will be configured as an input and the IN[n] event will be generated if operation specified in POLARITY occurs on the pin.

Task mode

The GPIO specified by PSEL will be configured as an output and triggering the SET[n], CLR[n] or OUT[n] task will perform the operation specified by POLARITY on the pin. When enabled as a task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module.

GPIO number associated with SET[n], CLR[n] and OUT[n] tasks and IN[n] event

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															D			C	C				B	B	B	B	B							A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
C	RW	POLARITY																																	
				When In task mode: Operation to be performed on output when OUT[n] task is triggered. When In event mode: Operation on input that shall trigger IN[n] event.																																
			None	0																															
				Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity.																															
			LoToHi	1																															
				Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin.																															
			HiToLo	2																															
				Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin.																															
			Toggle	3																															
				Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin.																															
D	RW	OUTINIT																																	
				When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect.																															
			Low	0																															
				Task mode: Initial value of pin before task triggering is low																															
			High	1																															
				Task mode: Initial value of pin before task triggering is high																															

19.4.4 CONFIG[1]

Address offset: 0x514

Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															D			C	C				B	B	B	B	B							A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	MODE																																	
				Mode																															
			Disabled	0																															
				Disabled. Pin specified by PSEL will not be acquired by the GPIOTE module.																															
			Event	1																															
				Event mode The pin specified by PSEL will be configured as an input and the IN[n] event will be generated if operation specified in POLARITY occurs on the pin.																															
			Task	3																															
				Task mode The GPIO specified by PSEL will be configured as an output and triggering the SET[n], CLR[n] or OUT[n] task will perform the operation specified by POLARITY on the pin. When enabled as a task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module.																															
B	RW	PSEL		[0..31]																															
				GPIO number associated with SET[n], CLR[n] and OUT[n] tasks and IN[n] event																															
C	RW	POLARITY																																	
				When In task mode: Operation to be performed on output when OUT[n] task is triggered. When In event mode: Operation on input that shall trigger IN[n] event.																															
			None	0																															
				Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity.																															
			LoToHi	1																															
				Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin.																															
			HiToLo	2																															
				Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin.																															
			Toggle	3																															
				Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin.																															
D	RW	OUTINIT																																	
				When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect.																															
			Low	0																															
				Task mode: Initial value of pin before task triggering is low																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															D			C	C				B	B	B	B	B							A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**											**Description**																				
			High	1											Task mode: Initial value of pin before task triggering is high																				

19.4.5 CONFIG[2]

Address offset: 0x518

Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															D			C	C				B	B	B	B	B							A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**											**Description**																				
A	RW	MODE													Mode																				
			Disabled	0											Disabled. Pin specified by PSEL will not be acquired by the GPIOTE module.																				
			Event	1											Event mode The pin specified by PSEL will be configured as an input and the IN[n] event will be generated if operation specified in POLARITY occurs on the pin.																				
			Task	3											Task mode The GPIO specified by PSEL will be configured as an output and triggering the SET[n], CLR[n] or OUT[n] task will perform the operation specified by POLARITY on the pin. When enabled as a task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module.																				
B	RW	PSEL		[0..31]											GPIO number associated with SET[n], CLR[n] and OUT[n] tasks and IN[n] event																				
C	RW	POLARITY													When In task mode: Operation to be performed on output when OUT[n] task is triggered. When In event mode: Operation on input that shall trigger IN[n] event.																				
			None	0											Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity.																				
			LoToHi	1											Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin.																				
			HiToLo	2											Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin.																				
			Toggle	3											Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin.																				
D	RW	OUTINIT													When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect.																				
			Low	0											Task mode: Initial value of pin before task triggering is low																				
			High	1											Task mode: Initial value of pin before task triggering is high																				

19.4.6 CONFIG[3]

Address offset: 0x51C

Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															D			C	C				B	B	B	B	B							A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**											**Description**																				
A	RW	MODE													Mode																				

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id														D			C	C				B	B	B	B	B							A	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
			Disabled								0																Disabled. Pin specified by PSEL will not be acquired by the GPIOTE module.							
			Event								1																Event mode The pin specified by PSEL will be configured as an input and the IN[n] event will be generated if operation specified in POLARITY occurs on the pin.							
			Task								3																Task mode The GPIO specified by PSEL will be configured as an output and triggering the SET[n], CLR[n] or OUT[n] task will perform the operation specified by POLARITY on the pin. When enabled as a task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module.							
B	RW	PSEL									[0..31]																GPIO number associated with SET[n], CLR[n] and OUT[n] tasks and IN[n] event							
C	RW	POLARITY																									When In task mode: Operation to be performed on output when OUT[n] task is triggered. When In event mode: Operation on input that shall trigger IN[n] event.							
			None								0																Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity.							
			LoToHi								1																Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin.							
			HiToLo								2																Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin.							
			Toggle								3																Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin.							
D	RW	OUTINIT																									When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect.							
			Low								0																Task mode: Initial value of pin before task triggering is low							
			High								1																Task mode: Initial value of pin before task triggering is high							

19.4.7 CONFIG[4]

Address offset: 0x520

Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id														D			C	C				B	B	B	B	B							A	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	RW	MODE																									Mode							
			Disabled								0																Disabled. Pin specified by PSEL will not be acquired by the GPIOTE module.							
			Event								1																Event mode The pin specified by PSEL will be configured as an input and the IN[n] event will be generated if operation specified in POLARITY occurs on the pin.							
			Task								3																Task mode The GPIO specified by PSEL will be configured as an output and triggering the SET[n], CLR[n] or OUT[n] task will perform the operation specified by POLARITY on the pin. When enabled as a task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module.							

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															D			C	C				B	B	B	B	B							A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
B	RW	PSEL		[0..31]																															
				GPIO number associated with SET[n], CLR[n] and OUT[n] tasks and IN[n] event																															
C	RW	POLARITY																																	
				When In task mode: Operation to be performed on output when OUT[n] task is triggered. When In event mode: Operation on input that shall trigger IN[n] event.																															
			None	0																															
				Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity.																															
			LoToHi	1																															
				Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin.																															
			HiToLo	2																															
				Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin.																															
			Toggle	3																															
				Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin.																															
D	RW	OUTINIT																																	
				When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect.																															
			Low	0																															
				Task mode: Initial value of pin before task triggering is low																															
			High	1																															
				Task mode: Initial value of pin before task triggering is high																															

19.4.8 CONFIG[5]

Address offset: 0x524

Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															D			C	C				B	B	B	B	B							A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	MODE																																	
				Mode																															
			Disabled	0																															
				Disabled. Pin specified by PSEL will not be acquired by the GPIOTE module.																															
			Event	1																															
				Event mode The pin specified by PSEL will be configured as an input and the IN[n] event will be generated if operation specified in POLARITY occurs on the pin.																															
			Task	3																															
				Task mode The GPIO specified by PSEL will be configured as an output and triggering the SET[n], CLR[n] or OUT[n] task will perform the operation specified by POLARITY on the pin. When enabled as a task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module.																															
B	RW	PSEL		[0..31]																															
				GPIO number associated with SET[n], CLR[n] and OUT[n] tasks and IN[n] event																															
C	RW	POLARITY																																	
				When In task mode: Operation to be performed on output when OUT[n] task is triggered. When In event mode: Operation on input that shall trigger IN[n] event.																															
			None	0																															
				Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity.																															
			LoToHi	1																															
				Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin.																															
			HiToLo	2																															
				Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin.																															
			Toggle	3																															
				Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin.																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															D			C	C				B	B	B	B	B							A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
D	RW	OUTINIT																																	
				When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect.																																	
			Low	0																																	
				Task mode: Initial value of pin before task triggering is low																																	
			High	1																																	
				Task mode: Initial value of pin before task triggering is high																																	

19.4.9 CONFIG[6]

Address offset: 0x528

Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															D			C	C				B	B	B	B	B							A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	MODE																																	
				Mode																																	
			Disabled	0																																	
				Disabled. Pin specified by PSEL will not be acquired by the GPIOTE module.																																	
			Event	1																																	
				Event mode The pin specified by PSEL will be configured as an input and the IN[n] event will be generated if operation specified in POLARITY occurs on the pin.																																	
			Task	3																																	
				Task mode The GPIO specified by PSEL will be configured as an output and triggering the SET[n], CLR[n] or OUT[n] task will perform the operation specified by POLARITY on the pin. When enabled as a task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module.																																	
B	RW	PSEL		[0..31]																																	
				GPIO number associated with SET[n], CLR[n] and OUT[n] tasks and IN[n] event																																	
C	RW	POLARITY																																	
				When In task mode: Operation to be performed on output when OUT[n] task is triggered. When In event mode: Operation on input that shall trigger IN[n] event.																																	
			None	0																																	
				Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity.																																	
			LoToHi	1																																	
				Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin.																																	
			HiToLo	2																																	
				Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin.																																	
			Toggle	3																																	
				Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin.																																	
D	RW	OUTINIT																																	
				When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect.																																	
			Low	0																																	
				Task mode: Initial value of pin before task triggering is low																																	
			High	1																																	
				Task mode: Initial value of pin before task triggering is high																																	

19.4.10 CONFIG[7]

Address offset: 0x52C

Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id												D			C	C				B	B	B	B	B							A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	MODE			Mode
			Disabled	0	Disabled. Pin specified by PSEL will not be acquired by the GPIOTE module.
			Event	1	Event mode The pin specified by PSEL will be configured as an input and the IN[n] event will be generated if operation specified in POLARITY occurs on the pin.
			Task	3	Task mode The GPIO specified by PSEL will be configured as an output and triggering the SET[n], CLR[n] or OUT[n] task will perform the operation specified by POLARITY on the pin. When enabled as a task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module.
B	RW	PSEL		[0..31]	GPIO number associated with SET[n], CLR[n] and OUT[n] tasks and IN[n] event
C	RW	POLARITY			When In task mode: Operation to be performed on output when OUT[n] task is triggered. When In event mode: Operation on input that shall trigger IN[n] event.
			None	0	Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity.
			LoToHi	1	Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin.
			HiToLo	2	Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin.
			Toggle	3	Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin.
D	RW	OUTINIT			When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect.
			Low	0	Task mode: Initial value of pin before task triggering is low
			High	1	Task mode: Initial value of pin before task triggering is high

19.5 Electrical Specification

19.5.1 GPIOTE Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
$I_{GPIOTE,IN}$	Run current with 1 or more GPIOTE active channels in Input mode		0.1	0.5	µA
$I_{GPIOTE,OUT}$	Run current with 1 or more GPIOTE active channels in Output mode		0.1		µA
$I_{GPIOTE,IDLE}$	Run current when all channels in Idle mode. PORT event can be generated with a delay of up to t_{1V3}.		0.1		µA

20 Programmable peripheral interconnect (PPI)

The Programmable peripheral interconnect (PPI) enables peripherals to interact autonomously with each other using tasks and events independent of the CPU. The PPI allows precise synchronization between peripherals when real-time application constraints exist and eliminates the need for CPU activity to implement behavior which can be predefined using PPI.

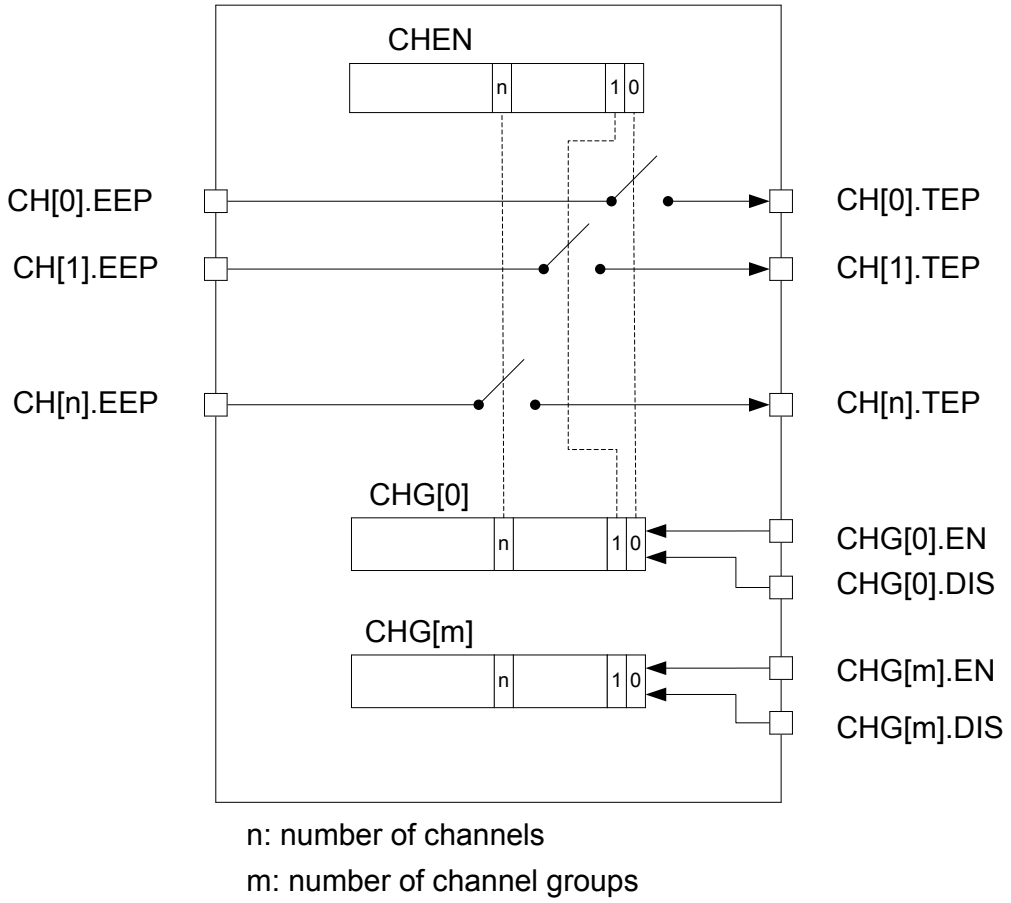

Figure 24: PPI block diagram

The PPI system has, in addition to the fully programmable peripheral interconnections, a set of channels where the event end point (EEP) and task end point (TEP) are fixed in hardware. These fixed channels can be individually enabled, disabled, or added to PPI channel groups in the same way as ordinary PPI channels.

Table 28: Configurable and fixed PPI channels

Instance	Channel	Number of channels	Number of groups
PPI	0-19	20	6
PPI (fixed)	20-31	12	

The PPI provides a mechanism to automatically trigger a task in one peripheral as a result of an event occurring in another peripheral. A task is connected to an event through a PPI channel. The PPI channel is composed of two end point registers, the event end point (EEP) and the task end point (TEP). A peripheral task is connected to a TEP using the address of the task register associated with the task. Similarly, a peripheral event is connected to an EEP using the address of the event register associated with the event.

Each TEP implements a fork mechanism that enables a second task to be triggered at the same time as the task specified in the TEP is triggered. This second task is configured in the task end point register in the FORK registers groups, e.g. FORK.TEP[0] is associated with PPI channel CH[0].

There are two ways of enabling and disabling PPI channels:

- Enable or disable PPI channels individually using the CHEN, CHENSET, and CHENCLR registers.
- Enable or disable PPI channels in PPI channel groups through the groups' ENABLE and DISABLE tasks. Prior to these tasks being triggered, the PPI channel group must be configured to define which PPI channels belongs to which groups.

Note that if CHG[n].EN and CHG[n].DIS occur simultaneously, EN has priority

PPI tasks (for example, CHG[0].EN) can be triggered through the PPI like any other task, which means they can be hooked up to a PPI channel as a TEP. One event can trigger multiple tasks by using multiple channels and one task can be triggered by multiple events in the same way.

20.1 Pre-programmed channels

Some of the PPI channels are pre-programmed. These channels cannot be configured by the CPU, but can be added to groups and enabled and disabled like the general purpose PPI channels.

For a list of pre-programmed PPI channels, see the table below.

Table 29: Pre-programmed channels

Channel	EEP	TEP
20	TIMER0->EVENTS_COMPARE[0]	RADIO->TASKS_TXEN
21	TIMER0->EVENTS_COMPARE[0]	RADIO->TASKS_RXEN
22	TIMER0->EVENTS_COMPARE[1]	RADIO->TASKS_DISABLE
23	RADIO->EVENTS_BCMATCH	AAR->TASKS_START
24	RADIO->EVENTS_READY	CCM->TASKS_KSGEN
25	RADIO->EVENTS_ADDRESS	CCM->TASKS_CRYPT
26	RADIO->EVENTS_ADDRESS	TIMER0->TASKS_CAPTURE[1]
27	RADIO->EVENTS_END	TIMER0->TASKS_CAPTURE[2]
28	RTC0->EVENTS_COMPARE[0]	RADIO->TASKS_TXEN
29	RTC0->EVENTS_COMPARE[0]	RADIO->TASKS_RXEN
30	RTC0->EVENTS_COMPARE[0]	TIMER0->TASKS_CLEAR
31	RTC0->EVENTS_COMPARE[0]	TIMER0->TASKS_START

20.2 Registers

Table 30: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4001F000	PPI	PPI	PPI controller	

Table 31: Register Overview

Register	Offset	Description
TASKS_CHG[0].EN	0x000	Enable channel group 0
TASKS_CHG[0].DIS	0x004	Disable channel group 0
TASKS_CHG[1].EN	0x008	Enable channel group 1
TASKS_CHG[1].DIS	0x00C	Disable channel group 1
TASKS_CHG[2].EN	0x010	Enable channel group 2
TASKS_CHG[2].DIS	0x014	Disable channel group 2
TASKS_CHG[3].EN	0x018	Enable channel group 3
TASKS_CHG[3].DIS	0x01C	Disable channel group 3
TASKS_CHG[4].EN	0x020	Enable channel group 4
TASKS_CHG[4].DIS	0x024	Disable channel group 4
TASKS_CHG[5].EN	0x028	Enable channel group 5
TASKS_CHG[5].DIS	0x02C	Disable channel group 5
CHEN	0x500	Channel enable register
CHENSET	0x504	Channel enable set register
CHENCLR	0x508	Channel enable clear register
CH[0].EEP	0x510	Channel 0 event end-point
CH[0].TEP	0x514	Channel 0 task end-point
CH[1].EEP	0x518	Channel 1 event end-point
CH[1].TEP	0x51C	Channel 1 task end-point

Register	Offset	Description
CH[2].EEP	0x520	Channel 2 event end-point
CH[2].TEP	0x524	Channel 2 task end-point
CH[3].EEP	0x528	Channel 3 event end-point
CH[3].TEP	0x52C	Channel 3 task end-point
CH[4].EEP	0x530	Channel 4 event end-point
CH[4].TEP	0x534	Channel 4 task end-point
CH[5].EEP	0x538	Channel 5 event end-point
CH[5].TEP	0x53C	Channel 5 task end-point
CH[6].EEP	0x540	Channel 6 event end-point
CH[6].TEP	0x544	Channel 6 task end-point
CH[7].EEP	0x548	Channel 7 event end-point
CH[7].TEP	0x54C	Channel 7 task end-point
CH[8].EEP	0x550	Channel 8 event end-point
CH[8].TEP	0x554	Channel 8 task end-point
CH[9].EEP	0x558	Channel 9 event end-point
CH[9].TEP	0x55C	Channel 9 task end-point
CH[10].EEP	0x560	Channel 10 event end-point
CH[10].TEP	0x564	Channel 10 task end-point
CH[11].EEP	0x568	Channel 11 event end-point
CH[11].TEP	0x56C	Channel 11 task end-point
CH[12].EEP	0x570	Channel 12 event end-point
CH[12].TEP	0x574	Channel 12 task end-point
CH[13].EEP	0x578	Channel 13 event end-point
CH[13].TEP	0x57C	Channel 13 task end-point
CH[14].EEP	0x580	Channel 14 event end-point
CH[14].TEP	0x584	Channel 14 task end-point
CH[15].EEP	0x588	Channel 15 event end-point
CH[15].TEP	0x58C	Channel 15 task end-point
CH[16].EEP	0x590	Channel 16 event end-point
CH[16].TEP	0x594	Channel 16 task end-point
CH[17].EEP	0x598	Channel 17 event end-point
CH[17].TEP	0x59C	Channel 17 task end-point
CH[18].EEP	0x5A0	Channel 18 event end-point
CH[18].TEP	0x5A4	Channel 18 task end-point
CH[19].EEP	0x5A8	Channel 19 event end-point
CH[19].TEP	0x5AC	Channel 19 task end-point
CHG[0]	0x800	Channel group 0
CHG[1]	0x804	Channel group 1
CHG[2]	0x808	Channel group 2
CHG[3]	0x80C	Channel group 3
CHG[4]	0x810	Channel group 4
CHG[5]	0x814	Channel group 5
FORK[0].TEP	0x910	Channel 0 task end-point
FORK[1].TEP	0x914	Channel 1 task end-point
FORK[2].TEP	0x918	Channel 2 task end-point
FORK[3].TEP	0x91C	Channel 3 task end-point
FORK[4].TEP	0x920	Channel 4 task end-point
FORK[5].TEP	0x924	Channel 5 task end-point
FORK[6].TEP	0x928	Channel 6 task end-point
FORK[7].TEP	0x92C	Channel 7 task end-point
FORK[8].TEP	0x930	Channel 8 task end-point
FORK[9].TEP	0x934	Channel 9 task end-point
FORK[10].TEP	0x938	Channel 10 task end-point
FORK[11].TEP	0x93C	Channel 11 task end-point
FORK[12].TEP	0x940	Channel 12 task end-point
FORK[13].TEP	0x944	Channel 13 task end-point
FORK[14].TEP	0x948	Channel 14 task end-point
FORK[15].TEP	0x94C	Channel 15 task end-point

Register	Offset	Description
FORK[16].TEP	0x950	Channel 16 task end-point
FORK[17].TEP	0x954	Channel 17 task end-point
FORK[18].TEP	0x958	Channel 18 task end-point
FORK[19].TEP	0x95C	Channel 19 task end-point
FORK[20].TEP	0x960	Channel 20 task end-point
FORK[21].TEP	0x964	Channel 21 task end-point
FORK[22].TEP	0x968	Channel 22 task end-point
FORK[23].TEP	0x96C	Channel 23 task end-point
FORK[24].TEP	0x970	Channel 24 task end-point
FORK[25].TEP	0x974	Channel 25 task end-point
FORK[26].TEP	0x978	Channel 26 task end-point
FORK[27].TEP	0x97C	Channel 27 task end-point
FORK[28].TEP	0x980	Channel 28 task end-point
FORK[29].TEP	0x984	Channel 29 task end-point
FORK[30].TEP	0x988	Channel 30 task end-point
FORK[31].TEP	0x98C	Channel 31 task end-point

20.2.1 CHEN

Address offset: 0x500

Channel enable register

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	CH0			Enable or disable channel 0
			Disabled	0	Disable channel
			Enabled	1	Enable channel
B	RW	CH1			Enable or disable channel 1
			Disabled	0	Disable channel
			Enabled	1	Enable channel
C	RW	CH2			Enable or disable channel 2
			Disabled	0	Disable channel
			Enabled	1	Enable channel
D	RW	CH3			Enable or disable channel 3
			Disabled	0	Disable channel
			Enabled	1	Enable channel
E	RW	CH4			Enable or disable channel 4
			Disabled	0	Disable channel
			Enabled	1	Enable channel
F	RW	CH5			Enable or disable channel 5
			Disabled	0	Disable channel
			Enabled	1	Enable channel
G	RW	CH6			Enable or disable channel 6
			Disabled	0	Disable channel
			Enabled	1	Enable channel
H	RW	CH7			Enable or disable channel 7
			Disabled	0	Disable channel
			Enabled	1	Enable channel
I	RW	CH8			Enable or disable channel 8
			Disabled	0	Disable channel
			Enabled	1	Enable channel
J	RW	CH9			Enable or disable channel 9
			Disabled	0	Disable channel
			Enabled	1	Enable channel
K	RW	CH10			Enable or disable channel 10
			Disabled	0	Disable channel

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Enabled	1																															
L	RW	CH11																																	
			Disabled	0																															
			Enabled	1																															
M	RW	CH12																																	
			Disabled	0																															
			Enabled	1																															
N	RW	CH13																																	
			Disabled	0																															
			Enabled	1																															
O	RW	CH14																																	
			Disabled	0																															
			Enabled	1																															
P	RW	CH15																																	
			Disabled	0																															
			Enabled	1																															
Q	RW	CH16																																	
			Disabled	0																															
			Enabled	1																															
R	RW	CH17																																	
			Disabled	0																															
			Enabled	1																															
S	RW	CH18																																	
			Disabled	0																															
			Enabled	1																															
T	RW	CH19																																	
			Disabled	0																															
			Enabled	1																															
U	RW	CH20																																	
			Disabled	0																															
			Enabled	1																															
V	RW	CH21																																	
			Disabled	0																															
			Enabled	1																															
W	RW	CH22																																	
			Disabled	0																															
			Enabled	1																															
X	RW	CH23																																	
			Disabled	0																															
			Enabled	1																															
Y	RW	CH24																																	
			Disabled	0																															
			Enabled	1																															
Z	RW	CH25																																	
			Disabled	0																															
			Enabled	1																															
a	RW	CH26																																	
			Disabled	0																															
			Enabled	1																															
b	RW	CH27																																	
			Disabled	0																															
			Enabled	1																															
c	RW	CH28																																	
			Disabled	0																															
			Enabled	1																															

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																													
d	RW	CH29			Enable or disable channel 29																															
			Disabled	0	Disable channel																															
			Enabled	1	Enable channel																															
e	RW	CH30			Enable or disable channel 30																															
			Disabled	0	Disable channel																															
			Enabled	1	Enable channel																															
f	RW	CH31			Enable or disable channel 31																															
			Disabled	0	Disable channel																															
			Enabled	1	Enable channel																															

20.2.2 CHENSET

Address offset: 0x504

Channel enable set register

Read: reads value of CH{i} field in CHEN register.

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																													
A	RW	CH0			Channel 0 enable set register. Writing '0' has no effect																															
			Disabled	0	Read: channel disabled																															
			Enabled	1	Read: channel enabled																															
			Set	1	Write: Enable channel																															
B	RW	CH1			Channel 1 enable set register. Writing '0' has no effect																															
			Disabled	0	Read: channel disabled																															
			Enabled	1	Read: channel enabled																															
			Set	1	Write: Enable channel																															
C	RW	CH2			Channel 2 enable set register. Writing '0' has no effect																															
			Disabled	0	Read: channel disabled																															
			Enabled	1	Read: channel enabled																															
			Set	1	Write: Enable channel																															
D	RW	CH3			Channel 3 enable set register. Writing '0' has no effect																															
			Disabled	0	Read: channel disabled																															
			Enabled	1	Read: channel enabled																															
			Set	1	Write: Enable channel																															
E	RW	CH4			Channel 4 enable set register. Writing '0' has no effect																															
			Disabled	0	Read: channel disabled																															
			Enabled	1	Read: channel enabled																															
			Set	1	Write: Enable channel																															
F	RW	CH5			Channel 5 enable set register. Writing '0' has no effect																															
			Disabled	0	Read: channel disabled																															
			Enabled	1	Read: channel enabled																															
			Set	1	Write: Enable channel																															
G	RW	CH6			Channel 6 enable set register. Writing '0' has no effect																															
			Disabled	0	Read: channel disabled																															
			Enabled	1	Read: channel enabled																															
			Set	1	Write: Enable channel																															
H	RW	CH7			Channel 7 enable set register. Writing '0' has no effect																															
			Disabled	0	Read: channel disabled																															
			Enabled	1	Read: channel enabled																															
			Set	1	Write: Enable channel																															
I	RW	CH8			Channel 8 enable set register. Writing '0' has no effect																															
			Disabled	0	Read: channel disabled																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Enabled	1																															
			Set	1																															
J	RW	CH9																																	
			Disabled	0																															
			Enabled	1																															
			Set	1																															
K	RW	CH10																																	
			Disabled	0																															
			Enabled	1																															
			Set	1																															
L	RW	CH11																																	
			Disabled	0																															
			Enabled	1																															
			Set	1																															
M	RW	CH12																																	
			Disabled	0																															
			Enabled	1																															
			Set	1																															
N	RW	CH13																																	
			Disabled	0																															
			Enabled	1																															
			Set	1																															
O	RW	CH14																																	
			Disabled	0																															
			Enabled	1																															
			Set	1																															
P	RW	CH15																																	
			Disabled	0																															
			Enabled	1																															
			Set	1																															
Q	RW	CH16																																	
			Disabled	0																															
			Enabled	1																															
			Set	1																															
R	RW	CH17																																	
			Disabled	0																															
			Enabled	1																															
			Set	1																															
S	RW	CH18																																	
			Disabled	0																															
			Enabled	1																															
			Set	1																															
T	RW	CH19																																	
			Disabled	0																															
			Enabled	1																															
			Set	1																															
U	RW	CH20																																	
			Disabled	0																															
			Enabled	1																															
			Set	1																															
V	RW	CH21																																	
			Disabled	0																															
			Enabled	1																															
			Set	1																															
W	RW	CH22																																	

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Disabled	0																															
			Enabled	1																															
			Set	1																															
X	RW	CH23																																	
			Disabled	0																															
			Enabled	1																															
			Set	1																															
Y	RW	CH24																																	
			Disabled	0																															
			Enabled	1																															
			Set	1																															
Z	RW	CH25																																	
			Disabled	0																															
			Enabled	1																															
			Set	1																															
a	RW	CH26																																	
			Disabled	0																															
			Enabled	1																															
			Set	1																															
b	RW	CH27																																	
			Disabled	0																															
			Enabled	1																															
			Set	1																															
c	RW	CH28																																	
			Disabled	0																															
			Enabled	1																															
			Set	1																															
d	RW	CH29																																	
			Disabled	0																															
			Enabled	1																															
			Set	1																															
e	RW	CH30																																	
			Disabled	0																															
			Enabled	1																															
			Set	1																															
f	RW	CH31																																	
			Disabled	0																															
			Enabled	1																															
			Set	1																															

20.2.3 CHENCLR

Address offset: 0x508

Channel enable clear register

Read: reads value of CH{i} field in CHEN register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	CH0																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
B	RW	CH1																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
C	RW	CH2																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
D	RW	CH3																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
E	RW	CH4																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
F	RW	CH5																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
G	RW	CH6																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
H	RW	CH7																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
I	RW	CH8																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
J	RW	CH9																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
K	RW	CH10																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
L	RW	CH11																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
M	RW	CH12																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
N	RW	CH13																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
O	RW	CH14																																	
			Disabled	0																															
			Enabled	1																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Clear	1																															
P	RW	CH15																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
Q	RW	CH16																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
R	RW	CH17																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
S	RW	CH18																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
T	RW	CH19																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
U	RW	CH20																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
V	RW	CH21																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
W	RW	CH22																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
X	RW	CH23																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
Y	RW	CH24																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
Z	RW	CH25																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
a	RW	CH26																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
b	RW	CH27																																	
			Disabled	0																															
			Enabled	1																															
			Clear	1																															
c	RW	CH28																																	
			Disabled	0																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																									**Description**						
			Enabled	1																									Read: channel enabled						
			Clear	1																									Write: disable channel						
d	RW	CH29																											Channel 29 enable clear register. Writing '0' has no effect						
			Disabled	0																									Read: channel disabled						
			Enabled	1																									Read: channel enabled						
			Clear	1																									Write: disable channel						
e	RW	CH30																											Channel 30 enable clear register. Writing '0' has no effect						
			Disabled	0																									Read: channel disabled						
			Enabled	1																									Read: channel enabled						
			Clear	1																									Write: disable channel						
f	RW	CH31																											Channel 31 enable clear register. Writing '0' has no effect						
			Disabled	0																									Read: channel disabled						
			Enabled	1																									Read: channel enabled						
			Clear	1																									Write: disable channel						

20.2.4 CH[0].EEP

Address offset: 0x510

Channel 0 event end-point

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																									**Description**						
A	RW	EEP																											Pointer to event register. Accepts only addresses to registers from the Event group.						

20.2.5 CH[0].TEP

Address offset: 0x514

Channel 0 task end-point

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																									**Description**						
A	RW	TEP																											Pointer to task register. Accepts only addresses to registers from the Task group.						

20.2.6 CH[1].EEP

Address offset: 0x518

Channel 1 event end-point

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																									**Description**						
A	RW	EEP																											Pointer to event register. Accepts only addresses to registers from the Event group.						

20.2.7 CH[1].TEP

Address offset: 0x51C

Channel 1 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register. Accepts only addresses to registers from the Task group.

20.2.8 CH[2].EEP

Address offset: 0x520

Channel 2 event end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	EEP			Pointer to event register. Accepts only addresses to registers from the Event group.

20.2.9 CH[2].TEP

Address offset: 0x524

Channel 2 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register. Accepts only addresses to registers from the Task group.

20.2.10 CH[3].EEP

Address offset: 0x528

Channel 3 event end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	EEP			Pointer to event register. Accepts only addresses to registers from the Event group.

20.2.11 CH[3].TEP

Address offset: 0x52C

Channel 3 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register. Accepts only addresses to registers from the Task group.

20.2.12 CH[4].EEP

Address offset: 0x530

Channel 4 event end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	EEP			Pointer to event register. Accepts only addresses to registers from the Event group.

20.2.13 CH[4].TEP

Address offset: 0x534

Channel 4 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register. Accepts only addresses to registers from the Task group.

20.2.14 CH[5].EEP

Address offset: 0x538

Channel 5 event end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	EEP			Pointer to event register. Accepts only addresses to registers from the Event group.

20.2.15 CH[5].TEP

Address offset: 0x53C

Channel 5 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register. Accepts only addresses to registers from the Task group.

20.2.16 CH[6].EEP

Address offset: 0x540

Channel 6 event end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	EEP			Pointer to event register. Accepts only addresses to registers from the Event group.

20.2.17 CH[6].TEP

Address offset: 0x544

Channel 6 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register. Accepts only addresses to registers from the Task group.

20.2.18 CH[7].EEP

Address offset: 0x548

Channel 7 event end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	EEP			Pointer to event register. Accepts only addresses to registers from the Event group.

20.2.19 CH[7].TEP

Address offset: 0x54C

Channel 7 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register. Accepts only addresses to registers from the Task group.

20.2.20 CH[8].EEP

Address offset: 0x550

Channel 8 event end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	EEP			Pointer to event register. Accepts only addresses to registers from the Event group.

20.2.21 CH[8].TEP

Address offset: 0x554

Channel 8 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register. Accepts only addresses to registers from the Task group.

20.2.22 CH[9].EEP

Address offset: 0x558

Channel 9 event end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	EEP			Pointer to event register. Accepts only addresses to registers from the Event group.

20.2.23 CH[9].TEP

Address offset: 0x55C

Channel 9 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register. Accepts only addresses to registers from the Task group.

20.2.24 CH[10].EEP

Address offset: 0x560

Channel 10 event end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	EEP			Pointer to event register. Accepts only addresses to registers from the Event group.

20.2.25 CH[10].TEP

Address offset: 0x564

Channel 10 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register. Accepts only addresses to registers from the Task group.

20.2.26 CH[11].EEP

Address offset: 0x568

Channel 11 event end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	EEP			Pointer to event register. Accepts only addresses to registers from the Event group.

20.2.27 CH[11].TEP

Address offset: 0x56C

Channel 11 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register. Accepts only addresses to registers from the Task group.

20.2.28 CH[12].EEP

Address offset: 0x570

Channel 12 event end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	EEP			Pointer to event register. Accepts only addresses to registers from the Event group.

20.2.29 CH[12].TEP

Address offset: 0x574

Channel 12 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register. Accepts only addresses to registers from the Task group.

20.2.30 CH[13].EEP

Address offset: 0x578

Channel 13 event end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	EEP			Pointer to event register. Accepts only addresses to registers from the Event group.

20.2.31 CH[13].TEP

Address offset: 0x57C

Channel 13 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register. Accepts only addresses to registers from the Task group.

20.2.32 CH[14].EEP

Address offset: 0x580

Channel 14 event end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	EEP			Pointer to event register. Accepts only addresses to registers from the Event group.

20.2.33 CH[14].TEP

Address offset: 0x584

Channel 14 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register. Accepts only addresses to registers from the Task group.

20.2.34 CH[15].EEP

Address offset: 0x588

Channel 15 event end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	EEP			Pointer to event register. Accepts only addresses to registers from the Event group.

20.2.35 CH[15].TEP

Address offset: 0x58C

Channel 15 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register. Accepts only addresses to registers from the Task group.

20.2.36 CH[16].EEP

Address offset: 0x590

Channel 16 event end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	EEP			Pointer to event register. Accepts only addresses to registers from the Event group.

20.2.37 CH[16].TEP

Address offset: 0x594

Channel 16 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register. Accepts only addresses to registers from the Task group.

20.2.38 CH[17].EEP

Address offset: 0x598

Channel 17 event end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	EEP			Pointer to event register. Accepts only addresses to registers from the Event group.

20.2.39 CH[17].TEP

Address offset: 0x59C

Channel 17 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register. Accepts only addresses to registers from the Task group.

20.2.40 CH[18].EEP

Address offset: 0x5A0

Channel 18 event end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	EEP			Pointer to event register. Accepts only addresses to registers from the Event group.

20.2.41 CH[18].TEP

Address offset: 0x5A4

Channel 18 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register. Accepts only addresses to registers from the Task group.

20.2.42 CH[19].EEP

Address offset: 0x5A8

Channel 19 event end-point

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	EEP			Pointer to event register. Accepts only addresses to registers from the Event group.

20.2.43 CH[19].TEP

Address offset: 0x5AC

Channel 19 task end-point

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	TEP			Pointer to task register. Accepts only addresses to registers from the Task group.

20.2.44 CHG[0]

Address offset: 0x800

Channel group 0

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e d c b a Z Y X W V U T S R Q P O N M L K J I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	CH0			Include or exclude channel 0
			Excluded	0	Exclude
			Included	1	Include
B	RW	CH1			Include or exclude channel 1
			Excluded	0	Exclude
			Included	1	Include
C	RW	CH2			Include or exclude channel 2
			Excluded	0	Exclude
			Included	1	Include
D	RW	CH3			Include or exclude channel 3
			Excluded	0	Exclude
			Included	1	Include
E	RW	CH4			Include or exclude channel 4
			Excluded	0	Exclude
			Included	1	Include
F	RW	CH5			Include or exclude channel 5
			Excluded	0	Exclude
			Included	1	Include
G	RW	CH6			Include or exclude channel 6
			Excluded	0	Exclude
			Included	1	Include
H	RW	CH7			Include or exclude channel 7
			Excluded	0	Exclude
			Included	1	Include
I	RW	CH8			Include or exclude channel 8
			Excluded	0	Exclude
			Included	1	Include
J	RW	CH9			Include or exclude channel 9
			Excluded	0	Exclude
			Included	1	Include
K	RW	CH10			Include or exclude channel 10

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Excluded	0																															
			Included	1																															
L	RW	CH11																																	
			Excluded	0																															
			Included	1																															
M	RW	CH12																																	
			Excluded	0																															
			Included	1																															
N	RW	CH13																																	
			Excluded	0																															
			Included	1																															
O	RW	CH14																																	
			Excluded	0																															
			Included	1																															
P	RW	CH15																																	
			Excluded	0																															
			Included	1																															
Q	RW	CH16																																	
			Excluded	0																															
			Included	1																															
R	RW	CH17																																	
			Excluded	0																															
			Included	1																															
S	RW	CH18																																	
			Excluded	0																															
			Included	1																															
T	RW	CH19																																	
			Excluded	0																															
			Included	1																															
U	RW	CH20																																	
			Excluded	0																															
			Included	1																															
V	RW	CH21																																	
			Excluded	0																															
			Included	1																															
W	RW	CH22																																	
			Excluded	0																															
			Included	1																															
X	RW	CH23																																	
			Excluded	0																															
			Included	1																															
Y	RW	CH24																																	
			Excluded	0																															
			Included	1																															
Z	RW	CH25																																	
			Excluded	0																															
			Included	1																															
a	RW	CH26																																	
			Excluded	0																															
			Included	1																															
b	RW	CH27																																	
			Excluded	0																															
			Included	1																															
c	RW	CH28																																	
			Excluded	0																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Included	1																															
d	RW	CH29																																	
			Excluded	0																															
			Included	1																															
e	RW	CH30																																	
			Excluded	0																															
			Included	1																															
f	RW	CH31																																	
			Excluded	0																															
			Included	1																															

20.2.45 CHG[1]

Address offset: 0x804

Channel group 1

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	CH0																																	
			Excluded	0																															
			Included	1																															
B	RW	CH1																																	
			Excluded	0																															
			Included	1																															
C	RW	CH2																																	
			Excluded	0																															
			Included	1																															
D	RW	CH3																																	
			Excluded	0																															
			Included	1																															
E	RW	CH4																																	
			Excluded	0																															
			Included	1																															
F	RW	CH5																																	
			Excluded	0																															
			Included	1																															
G	RW	CH6																																	
			Excluded	0																															
			Included	1																															
H	RW	CH7																																	
			Excluded	0																															
			Included	1																															
I	RW	CH8																																	
			Excluded	0																															
			Included	1																															
J	RW	CH9																																	
			Excluded	0																															
			Included	1																															
K	RW	CH10																																	
			Excluded	0																															
			Included	1																															
L	RW	CH11																																	
			Excluded	0																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
			Included	1	Include
M	RW	CH12			Include or exclude channel 12
			Excluded	0	Exclude
			Included	1	Include
N	RW	CH13			Include or exclude channel 13
			Excluded	0	Exclude
			Included	1	Include
O	RW	CH14			Include or exclude channel 14
			Excluded	0	Exclude
			Included	1	Include
P	RW	CH15			Include or exclude channel 15
			Excluded	0	Exclude
			Included	1	Include
Q	RW	CH16			Include or exclude channel 16
			Excluded	0	Exclude
			Included	1	Include
R	RW	CH17			Include or exclude channel 17
			Excluded	0	Exclude
			Included	1	Include
S	RW	CH18			Include or exclude channel 18
			Excluded	0	Exclude
			Included	1	Include
T	RW	CH19			Include or exclude channel 19
			Excluded	0	Exclude
			Included	1	Include
U	RW	CH20			Include or exclude channel 20
			Excluded	0	Exclude
			Included	1	Include
V	RW	CH21			Include or exclude channel 21
			Excluded	0	Exclude
			Included	1	Include
W	RW	CH22			Include or exclude channel 22
			Excluded	0	Exclude
			Included	1	Include
X	RW	CH23			Include or exclude channel 23
			Excluded	0	Exclude
			Included	1	Include
Y	RW	CH24			Include or exclude channel 24
			Excluded	0	Exclude
			Included	1	Include
Z	RW	CH25			Include or exclude channel 25
			Excluded	0	Exclude
			Included	1	Include
a	RW	CH26			Include or exclude channel 26
			Excluded	0	Exclude
			Included	1	Include
b	RW	CH27			Include or exclude channel 27
			Excluded	0	Exclude
			Included	1	Include
c	RW	CH28			Include or exclude channel 28
			Excluded	0	Exclude
			Included	1	Include
d	RW	CH29			Include or exclude channel 29
			Excluded	0	Exclude
			Included	1	Include

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
e	RW	CH30			Include or exclude channel 30
			Excluded	0	Exclude
			Included	1	Include
f	RW	CH31			Include or exclude channel 31
			Excluded	0	Exclude
			Included	1	Include

20.2.46 CHG[2]

Address offset: 0x808

Channel group 2

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	CH0			Include or exclude channel 0
			Excluded	0	Exclude
			Included	1	Include
B	RW	CH1			Include or exclude channel 1
			Excluded	0	Exclude
			Included	1	Include
C	RW	CH2			Include or exclude channel 2
			Excluded	0	Exclude
			Included	1	Include
D	RW	CH3			Include or exclude channel 3
			Excluded	0	Exclude
			Included	1	Include
E	RW	CH4			Include or exclude channel 4
			Excluded	0	Exclude
			Included	1	Include
F	RW	CH5			Include or exclude channel 5
			Excluded	0	Exclude
			Included	1	Include
G	RW	CH6			Include or exclude channel 6
			Excluded	0	Exclude
			Included	1	Include
H	RW	CH7			Include or exclude channel 7
			Excluded	0	Exclude
			Included	1	Include
I	RW	CH8			Include or exclude channel 8
			Excluded	0	Exclude
			Included	1	Include
J	RW	CH9			Include or exclude channel 9
			Excluded	0	Exclude
			Included	1	Include
K	RW	CH10			Include or exclude channel 10
			Excluded	0	Exclude
			Included	1	Include
L	RW	CH11			Include or exclude channel 11
			Excluded	0	Exclude
			Included	1	Include
M	RW	CH12			Include or exclude channel 12
			Excluded	0	Exclude
			Included	1	Include

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
N	RW	CH13																																	
			Excluded	0																															
			Included	1																															
O	RW	CH14																																	
			Excluded	0																															
			Included	1																															
P	RW	CH15																																	
			Excluded	0																															
			Included	1																															
Q	RW	CH16																																	
			Excluded	0																															
			Included	1																															
R	RW	CH17																																	
			Excluded	0																															
			Included	1																															
S	RW	CH18																																	
			Excluded	0																															
			Included	1																															
T	RW	CH19																																	
			Excluded	0																															
			Included	1																															
U	RW	CH20																																	
			Excluded	0																															
			Included	1																															
V	RW	CH21																																	
			Excluded	0																															
			Included	1																															
W	RW	CH22																																	
			Excluded	0																															
			Included	1																															
X	RW	CH23																																	
			Excluded	0																															
			Included	1																															
Y	RW	CH24																																	
			Excluded	0																															
			Included	1																															
Z	RW	CH25																																	
			Excluded	0																															
			Included	1																															
a	RW	CH26																																	
			Excluded	0																															
			Included	1																															
b	RW	CH27																																	
			Excluded	0																															
			Included	1																															
c	RW	CH28																																	
			Excluded	0																															
			Included	1																															
d	RW	CH29																																	
			Excluded	0																															
			Included	1																															
e	RW	CH30																																	
			Excluded	0																															
			Included	1																															
f	RW	CH31																																	

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																														
			Excluded	0																														
			Included	1																														

20.2.47 CHG[3]

Address offset: 0x80C

Channel group 3

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																														
A	RW	CH0																																
			Excluded	0																														
			Included	1																														
B	RW	CH1																																
			Excluded	0																														
			Included	1																														
C	RW	CH2																																
			Excluded	0																														
			Included	1																														
D	RW	CH3																																
			Excluded	0																														
			Included	1																														
E	RW	CH4																																
			Excluded	0																														
			Included	1																														
F	RW	CH5																																
			Excluded	0																														
			Included	1																														
G	RW	CH6																																
			Excluded	0																														
			Included	1																														
H	RW	CH7																																
			Excluded	0																														
			Included	1																														
I	RW	CH8																																
			Excluded	0																														
			Included	1																														
J	RW	CH9																																
			Excluded	0																														
			Included	1																														
K	RW	CH10																																
			Excluded	0																														
			Included	1																														
L	RW	CH11																																
			Excluded	0																														
			Included	1																														
M	RW	CH12																																
			Excluded	0																														
			Included	1																														
N	RW	CH13																																
			Excluded	0																														
			Included	1																														
O	RW	CH14																																

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Excluded	0																															
			Included	1																															
P	RW	CH15																																	
			Excluded	0																															
			Included	1																															
Q	RW	CH16																																	
			Excluded	0																															
			Included	1																															
R	RW	CH17																																	
			Excluded	0																															
			Included	1																															
S	RW	CH18																																	
			Excluded	0																															
			Included	1																															
T	RW	CH19																																	
			Excluded	0																															
			Included	1																															
U	RW	CH20																																	
			Excluded	0																															
			Included	1																															
V	RW	CH21																																	
			Excluded	0																															
			Included	1																															
W	RW	CH22																																	
			Excluded	0																															
			Included	1																															
X	RW	CH23																																	
			Excluded	0																															
			Included	1																															
Y	RW	CH24																																	
			Excluded	0																															
			Included	1																															
Z	RW	CH25																																	
			Excluded	0																															
			Included	1																															
a	RW	CH26																																	
			Excluded	0																															
			Included	1																															
b	RW	CH27																																	
			Excluded	0																															
			Included	1																															
c	RW	CH28																																	
			Excluded	0																															
			Included	1																															
d	RW	CH29																																	
			Excluded	0																															
			Included	1																															
e	RW	CH30																																	
			Excluded	0																															
			Included	1																															
f	RW	CH31																																	
			Excluded	0																															
			Included	1																															

20.2.48 CHG[4]

Address offset: 0x810

Channel group 4

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	CH0																																	Include or exclude channel 0
			Excluded	0																															Exclude
			Included	1																															Include
B	RW	CH1																																	Include or exclude channel 1
			Excluded	0																															Exclude
			Included	1																															Include
C	RW	CH2																																	Include or exclude channel 2
			Excluded	0																															Exclude
			Included	1																															Include
D	RW	CH3																																	Include or exclude channel 3
			Excluded	0																															Exclude
			Included	1																															Include
E	RW	CH4																																	Include or exclude channel 4
			Excluded	0																															Exclude
			Included	1																															Include
F	RW	CH5																																	Include or exclude channel 5
			Excluded	0																															Exclude
			Included	1																															Include
G	RW	CH6																																	Include or exclude channel 6
			Excluded	0																															Exclude
			Included	1																															Include
H	RW	CH7																																	Include or exclude channel 7
			Excluded	0																															Exclude
			Included	1																															Include
I	RW	CH8																																	Include or exclude channel 8
			Excluded	0																															Exclude
			Included	1																															Include
J	RW	CH9																																	Include or exclude channel 9
			Excluded	0																															Exclude
			Included	1																															Include
K	RW	CH10																																	Include or exclude channel 10
			Excluded	0																															Exclude
			Included	1																															Include
L	RW	CH11																																	Include or exclude channel 11
			Excluded	0																															Exclude
			Included	1																															Include
M	RW	CH12																																	Include or exclude channel 12
			Excluded	0																															Exclude
			Included	1																															Include
N	RW	CH13																																	Include or exclude channel 13
			Excluded	0																															Exclude
			Included	1																															Include
O	RW	CH14																																	Include or exclude channel 14
			Excluded	0																															Exclude
			Included	1																															Include
P	RW	CH15																																	Include or exclude channel 15
			Excluded	0																															Exclude
			Included	1																															Include
Q	RW	CH16																																	Include or exclude channel 16
			Excluded	0																															Exclude

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Included	1																															
R	RW	CH17																																	
			Excluded	0																															
			Included	1																															
S	RW	CH18																																	
			Excluded	0																															
			Included	1																															
T	RW	CH19																																	
			Excluded	0																															
			Included	1																															
U	RW	CH20																																	
			Excluded	0																															
			Included	1																															
V	RW	CH21																																	
			Excluded	0																															
			Included	1																															
W	RW	CH22																																	
			Excluded	0																															
			Included	1																															
X	RW	CH23																																	
			Excluded	0																															
			Included	1																															
Y	RW	CH24																																	
			Excluded	0																															
			Included	1																															
Z	RW	CH25																																	
			Excluded	0																															
			Included	1																															
a	RW	CH26																																	
			Excluded	0																															
			Included	1																															
b	RW	CH27																																	
			Excluded	0																															
			Included	1																															
c	RW	CH28																																	
			Excluded	0																															
			Included	1																															
d	RW	CH29																																	
			Excluded	0																															
			Included	1																															
e	RW	CH30																																	
			Excluded	0																															
			Included	1																															
f	RW	CH31																																	
			Excluded	0																															
			Included	1																															

20.2.49 CHG[5]

Address offset: 0x814

Channel group 5

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	CH0																																	
			Excluded	0																															
			Included	1																															
B	RW	CH1																																	
			Excluded	0																															
			Included	1																															
C	RW	CH2																																	
			Excluded	0																															
			Included	1																															
D	RW	CH3																																	
			Excluded	0																															
			Included	1																															
E	RW	CH4																																	
			Excluded	0																															
			Included	1																															
F	RW	CH5																																	
			Excluded	0																															
			Included	1																															
G	RW	CH6																																	
			Excluded	0																															
			Included	1																															
H	RW	CH7																																	
			Excluded	0																															
			Included	1																															
I	RW	CH8																																	
			Excluded	0																															
			Included	1																															
J	RW	CH9																																	
			Excluded	0																															
			Included	1																															
K	RW	CH10																																	
			Excluded	0																															
			Included	1																															
L	RW	CH11																																	
			Excluded	0																															
			Included	1																															
M	RW	CH12																																	
			Excluded	0																															
			Included	1																															
N	RW	CH13																																	
			Excluded	0																															
			Included	1																															
O	RW	CH14																																	
			Excluded	0																															
			Included	1																															
P	RW	CH15																																	
			Excluded	0																															
			Included	1																															
Q	RW	CH16																																	
			Excluded	0																															
			Included	1																															
R	RW	CH17																																	
			Excluded	0																															
			Included	1																															
S	RW	CH18																																	

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Excluded	0																															
			Included	1																															
T	RW	CH19																																	
			Excluded	0																															
			Included	1																															
U	RW	CH20																																	
			Excluded	0																															
			Included	1																															
V	RW	CH21																																	
			Excluded	0																															
			Included	1																															
W	RW	CH22																																	
			Excluded	0																															
			Included	1																															
X	RW	CH23																																	
			Excluded	0																															
			Included	1																															
Y	RW	CH24																																	
			Excluded	0																															
			Included	1																															
Z	RW	CH25																																	
			Excluded	0																															
			Included	1																															
a	RW	CH26																																	
			Excluded	0																															
			Included	1																															
b	RW	CH27																																	
			Excluded	0																															
			Included	1																															
c	RW	CH28																																	
			Excluded	0																															
			Included	1																															
d	RW	CH29																																	
			Excluded	0																															
			Included	1																															
e	RW	CH30																																	
			Excluded	0																															
			Included	1																															
f	RW	CH31																																	
			Excluded	0																															
			Included	1																															

20.2.50 FORK[0].TEP

Address offset: 0x910

Channel 0 task end-point

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	TEP																																	

20.2.51 FORK[1].TEP

Address offset: 0x914

Channel 1 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.52 FORK[2].TEP

Address offset: 0x918

Channel 2 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.53 FORK[3].TEP

Address offset: 0x91C

Channel 3 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.54 FORK[4].TEP

Address offset: 0x920

Channel 4 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.55 FORK[5].TEP

Address offset: 0x924

Channel 5 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.56 FORK[6].TEP

Address offset: 0x928

Channel 6 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.57 FORK[7].TEP

Address offset: 0x92C

Channel 7 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.58 FORK[8].TEP

Address offset: 0x930

Channel 8 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.59 FORK[9].TEP

Address offset: 0x934

Channel 9 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.60 FORK[10].TEP

Address offset: 0x938

Channel 10 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.61 FORK[11].TEP

Address offset: 0x93C

Channel 11 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.62 FORK[12].TEP

Address offset: 0x940

Channel 12 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.63 FORK[13].TEP

Address offset: 0x944

Channel 13 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.64 FORK[14].TEP

Address offset: 0x948

Channel 14 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.65 FORK[15].TEP

Address offset: 0x94C

Channel 15 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.66 FORK[16].TEP

Address offset: 0x950

Channel 16 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.67 FORK[17].TEP

Address offset: 0x954

Channel 17 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.68 FORK[18].TEP

Address offset: 0x958

Channel 18 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.69 FORK[19].TEP

Address offset: 0x95C

Channel 19 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.70 FORK[20].TEP

Address offset: 0x960

Channel 20 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.71 FORK[21].TEP

Address offset: 0x964

Channel 21 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.72 FORK[22].TEP

Address offset: 0x968

Channel 22 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.73 FORK[23].TEP

Address offset: 0x96C

Channel 23 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.74 FORK[24].TEP

Address offset: 0x970

Channel 24 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.75 FORK[25].TEP

Address offset: 0x974

Channel 25 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.76 FORK[26].TEP

Address offset: 0x978

Channel 26 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.77 FORK[27].TEP

Address offset: 0x97C

Channel 27 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.78 FORK[28].TEP

Address offset: 0x980

Channel 28 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.79 FORK[29].TEP

Address offset: 0x984

Channel 29 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.80 FORK[30].TEP

Address offset: 0x988

Channel 30 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

20.2.81 FORK[31].TEP

Address offset: 0x98C

Channel 31 task end-point

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TEP			Pointer to task register

21 2.4 GHz Radio (RADIO)

The RADIO contains a 2.4 GHz radio receiver and a 2.4 GHz radio transmitter that is compatible with Nordic's proprietary 1 Mbps and 2 Mbps radio modes in addition to 1 Mbps *Bluetooth* low energy mode.

21.1 Functional description

EasyDMA in combination with an automated packet assembler and packet disassembler, and an automated CRC generator and CRC checker, makes it very easy to configure and use the RADIO.

See *Figure 25: RADIO block diagram* on page 199 for details.

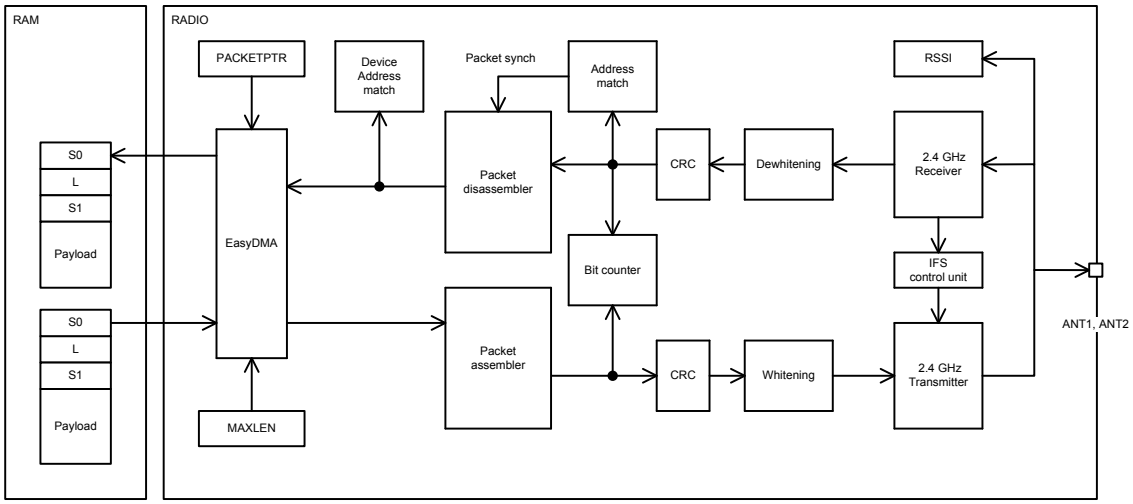

Figure 25: RADIO block diagram

The RADIO includes a Device Address Match unit and an interframe spacing control unit that can be utilized to simplify address white listing and interframe spacing respectively, in *Bluetooth* Smart and similar applications.

The RADIO also includes a Received Signal Strength Indicator (RSSI) and a bit counter. The bit counter generates events when a preconfigured number of bits have been sent or received by the RADIO.

21.1.1 EasyDMA

The RADIO use EasyDMA for reading and writing of data packets from and to the RAM without CPU involvement.

As illustrated in *Figure 25: RADIO block diagram* on page 199, the RADIO's EasyDMA utilizes the same PACKETPTR for receiving and transmitting packets. The CPU should reconfigure this pointer every time before the RADIO is started via the START task.

The structure of a radio packet is described in detail in *Packet configuration* on page 200. The data that is stored in Data RAM and transported by EasyDMA consists of S0, LENGTH, S1, the payload itself, and a static add-on sent immediately after the payload.

The size of each of the above elements in the frame is configurable (see *Packet configuration* on page 200), and the space occupied in RAM depends on these settings. A size of zero is possible for any of the fields, it is up to the user to make sure that the resulting frame complies with the RF protocol chosen.

For the field sizes defined in bits, the occupation in RAM will always be rounded up to the next full byte size (for instance 3 bit length will allocate 1 byte in RAM, 9 bit length will allocate 2 bytes, etc.).

In addition, the S0INCL field in PCNF0 determines if S0 is present in RAM at all if its length is zero. If present, one byte is allocated in RAM.

The size of S0 is configured through the S0LEN field in PCNF0. The size of LENGTH is configured through the LFLEN field in PCNF0. The size of S1 is configured through the S1LEN field in PCNF0. The size of the payload is configured through value in RAM corresponding to the LENGTH field. The size of the static add-on to the payload is configured through the STATLEN field in PCNF1.

The MAXLEN field in the PCNF1 register configures the maximum packet payload plus add-on size in number of bytes that can be transmitted or received by the RADIO. This feature can be used to ensure that the RADIO does not overwrite, or read beyond, the RAM assigned to the packet payload. This means that if the packet payload length defined by PCNF1.STATLEN and the LENGTH field in the packet specifies a packet larger than MAXLEN, the payload will be truncated at MAXLEN.

Note that MAXLEN includes the payload and the add-on, but excludes the size occupied by the S0, LENGTH and S1 fields. This has to be taken into account when allocating RAM.

If the payload plus add-on length is specified larger than MAXLEN, the RADIO will still transmit or receive in the same way as before except the payload is now truncated to MAXLEN. The packet's LENGTH field will not be altered when the payload is truncated. The RADIO will calculate CRC as if the packet length is equal to MAXLEN.

If the PACKETPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 34 for more information about the different memory regions.

The DISABLED event indicates that the EasyDMA has finished accessing the RAM.

21.1.2 Packet configuration

A Radio packet contains the following fields: PREAMBLE, ADDRESS, S0, LENGTH, S1, PAYLOAD and CRC.

See *Figure 26: On-air packet layout* on page 200. Not shown in the figure is the static payload add-on (the length of which is defined in STATLEN, and which is 0 bytes long in a standard BLE packet), and would be sent between PAYLOAD and CRC. The Radio sends the different fields in the packet in the order they are illustrated below, from left to right. The preamble will be sent least significant bit first on-air.

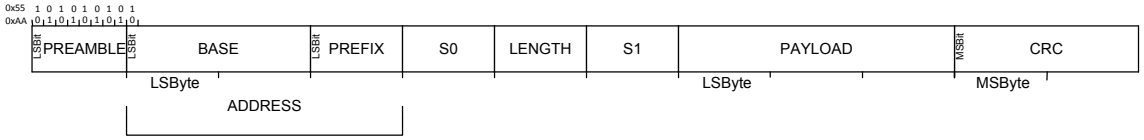

Figure 26: On-air packet layout

For all modes that can be specified in the MODE register, the PREAMBLE is one byte long. If the first bit of the ADDRESS is 0 the preamble will be set to 0xAA otherwise the PREAMBLE will be set to 0x55.

Radio packets are stored in memory inside instances of a radio packet data structure as illustrated in *Figure 27: In-RAM representation of radio packet, S0, LENGTH and S1 are optional* on page 200. The PREAMBLE, ADDRESS and CRC fields are omitted in this data structure.

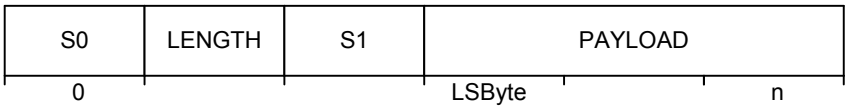

Figure 27: In-RAM representation of radio packet, S0, LENGTH and S1 are optional

The byte ordering on air is always Least Significant Byte First for the ADDRESS and PAYLOAD fields and Most Significant Byte First for the CRC field. The ADDRESS fields are always transmitted and received least

significant bit first on-air. The CRC field is always transmitted and received Most Significant Bit first. The bit-endian, i.e. which order the bits are sent and received in, of the S0, LENGTH, S1 and PAYLOAD fields can be configured via the ENDIAN in PCNF1.

The S0INCL field in PCNF0 determines if S0 is present in RAM at all if its length is zero. If present, one byte is allocated in RAM.

The sizes of the S0, LENGTH and S1 fields can be individually configured via S0LEN, LFLEN and S1LEN in PCNF0 respectively. If any of these fields are configured to be less than 8 bit long the, the least significant bits of the fields, as seen from the RAM representation, are used.

If S0, LENGTH or S1 are specified with zero length their fields will be omitted in memory, otherwise each field will be represented as a separate byte, regardless of the number of bits in their on-air counterpart.

21.1.3 Maximum packet length

Independent of the configuration of MAXLEN, the combined length of S0, LENGTH, S1 and PAYLOAD cannot exceed 258 bytes.

21.1.4 Address configuration

The on-air radio ADDRESS field is composed of two parts, the base address field and the address prefix field.

The size of the base address field is configurable via BALEN in PCNF1. The base address is truncated from LSByte if the BALEN is less than 4. See *Table 32: Definition of logical addresses* on page 201.

The on-air addresses are defined in the BASEn and PREFIXn registers, and it is only when writing these registers the user will have to relate to actual on-air addresses. For other radio address registers such as the TXADDRESS, RXADDRESSES and RXMATCH registers, logical radio addresses ranging from 0 to 7 are being used. The relationship between the on-air radio addresses and the logical addresses is described in *Table 32: Definition of logical addresses* on page 201.

Table 32: Definition of logical addresses

Logical address	Base address	Prefix byte
0	BASE0	PREFIX0.AP0
1	BASE1	PREFIX0.AP1
2	BASE1	PREFIX0.AP2
3	BASE1	PREFIX0.AP3
4	BASE1	PREFIX1.AP4
5	BASE1	PREFIX1.AP5
6	BASE1	PREFIX1.AP6
7	BASE1	PREFIX1.AP7

21.1.5 Data whitening

The RADIO is able to do packet whitening and de-whitening.

See WHITEEN in PCNF1 register for how to enable whitening. When enabled, whitening and de-whitening will be handled by the RADIO automatically as packets are sent and received, i.e. radio packets located in RAM will not be whitened.

The whitening word is generated using polynomial $g(D) = D^7 + D^4 + 1$, which then is XORed with the data packet that is to be whitened, or de-whitened, see the figure below.

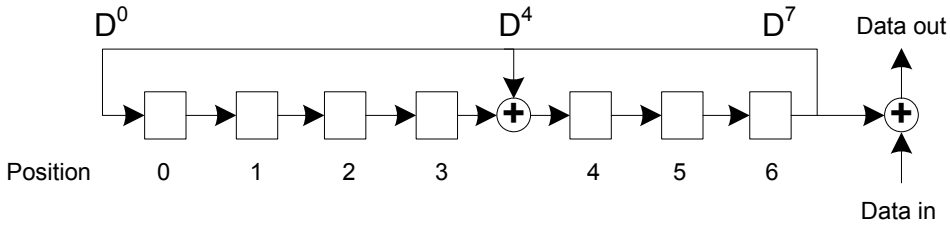

Figure 28: Data whitening and de-whitening

Whitening and de-whitening will be performed over the whole packet, except for the preamble, and the address field.

The linear feedback shift register, illustrated in *Figure 28: Data whitening and de-whitening* on page 202 can be initialised via the DATAWHITEIV register.

21.1.6 CRC

The CRC generator in the RADIO calculates the CRC over the whole packet excluding the preamble. If desirable, the address field can be excluded from the CRC calculation as well

See CRCCNF register for more information.

The CRC polynomial is configurable as illustrated in *Figure 29: CRC generation of an n bit CRC* on page 202 where bit 0 in the CRCPOLY register corresponds to X^0 and bit 1 corresponds to X^1 etc. See CRCPOLY for more information.

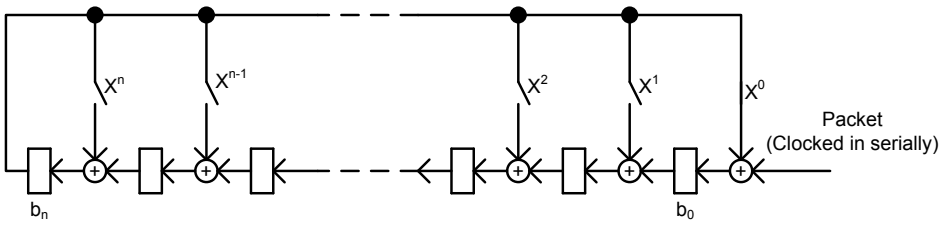

Figure 29: CRC generation of an n bit CRC

As illustrated in *Figure 29: CRC generation of an n bit CRC* on page 202, the CRC is calculated by feeding the packet serially through the CRC generator. Before the packet is clocked through the CRC generator, the CRC generator's latches b_0 through b_n will be initialized with a predefined value specified in the CRCINIT register. When the whole packet is clocked through the CRC generator, latches b_0 through b_n will hold the resulting CRC. This value will be used by the RADIO during both transmission and reception but it is not available to be read by the CPU at any time. A received CRC can however be read by the CPU via the RXCRC register independent of whether or not it has passed the CRC check.

The length (n) of the CRC is configurable, see CRCCNF for more information.

After the whole packet including the CRC has been received, the RADIO will generate a CRCOK event if no CRC errors were detected, or alternatively generate a CRCERROR event if CRC errors were detected.

The status of the CRC check can be read from the CRCSTATUS register after a packet has been received.

21.1.7 Radio states

The RADIO can enter a number of states.

The RADIO can enter the states described the table below. An overview state diagram for the RADIO is illustrated in *Figure 30: Radio states* on page 203. This figure shows how the tasks and events relate to the RADIO's operation. The RADIO does not prevent a task from being triggered from the wrong state. If a task is triggered from the wrong state, for example if the RXEN task is triggered from the RXDISABLE state, this may lead to incorrect behaviour. As illustrated in *Figure 30: Radio states* on page 203, the PAYLOAD event is always generated even if the payload is zero.

Table 33: RADIO state diagram

State	Description
DISABLED	No operations are going on inside the radio and the power consumption is at a minimum
RXRU	The radio is ramping up and preparing for reception
RXIDLE	The radio is ready for reception to start
RX	Reception has been started and the addresses enabled in the RXADDRESSES register are being monitored
TXRU	The radio is ramping up and preparing for transmission
TXIDLE	The radio is ready for transmission to start
TX	The radio is transmitting a packet
RXDISABLE	The radio is disabling the receiver
TXDISABLE	The radio is disabling the transmitter

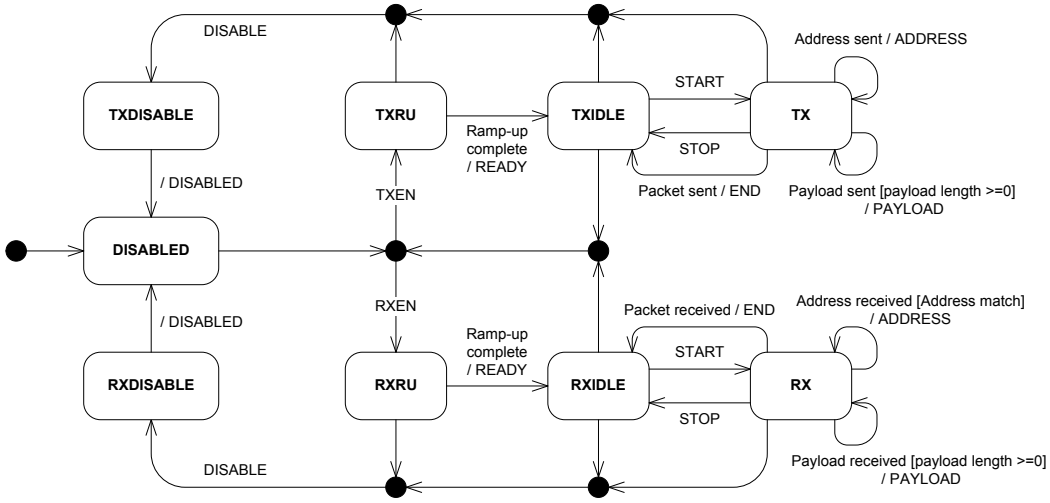

Figure 30: Radio states

21.1.8 Transmit sequence

Before the RADIO is able to transmit a packet, it must first ramp-up in TX mode.

See TXRU in *Figure 30: Radio states* on page 203 and *Figure 31: Transmit sequence* on page 204 etc. A TXRU ramp-up sequence is initiated when the TXEN task is triggered. After the radio has successfully ramped up it will generate the READY event indicating that a packet transmission can be initiate. A packet transmission is initiated by triggering the START task. As illustrated in *Figure 30: Radio states* on page 203 the START task can first be triggered after the RADIO has entered into the TXIDLE state.

Figure 31: Transmit sequence on page 204 illustrates a single packet transmission where the CPU manually triggers the different tasks needed to control the flow of the RADIO, i.e. no shortcuts are used. If shortcuts are not used, a certain amount of delay caused by CPU execution is expected between READY and START, and between END and DISABLE. As illustrated in *Figure 31: Transmit sequence* on page 204 the RADIO will by default transmit '1's between READY and START, and between END and DISABLED. What is transmitted can be programmed through the DTX field in the MODECNF0 register.

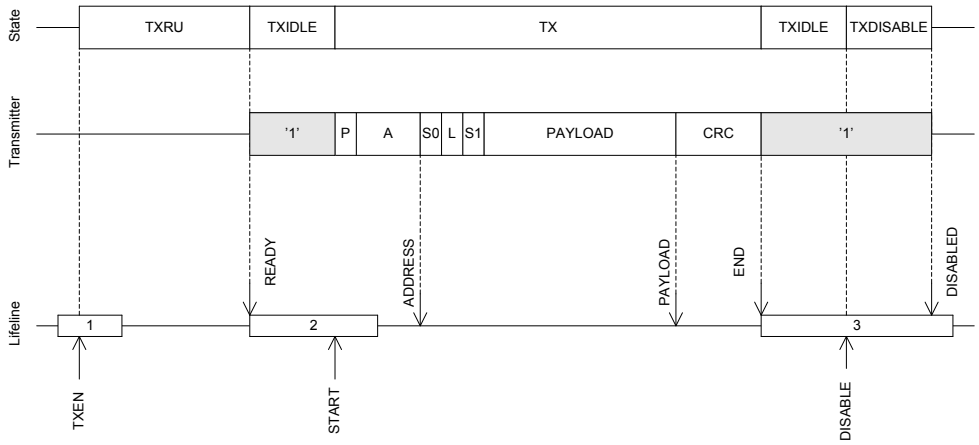

Figure 31: Transmit sequence

A slightly modified version of the transmit sequence from *Figure 31: Transmit sequence* on page 204 is illustrated in *Figure 32: Transmit sequence using shortcuts to avoid delays* on page 204 where the RADIO is configured to use shortcuts between READY and START, and between END and DISABLE, which means that no delay is introduced.

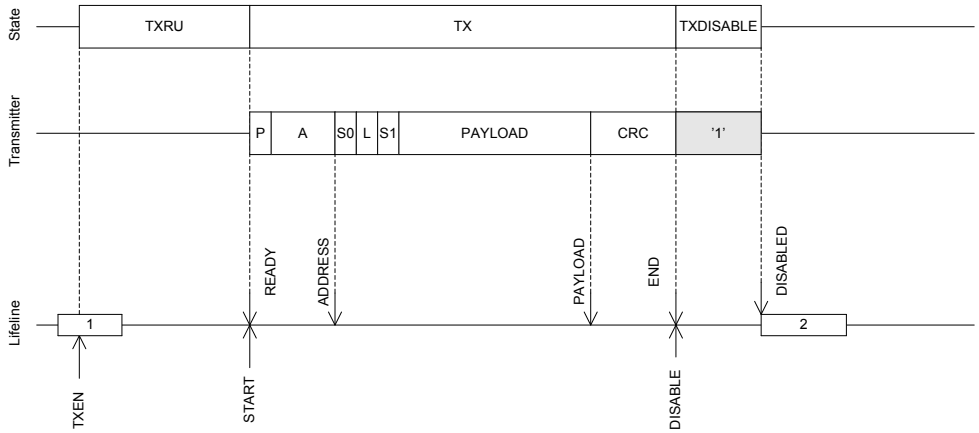

Figure 32: Transmit sequence using shortcuts to avoid delays

The RADIO is able to send multiple packets one after the other without having to disable and re-enable the RADIO between packets, this is illustrated in *Figure 33: Transmission of multiple packets* on page 205.

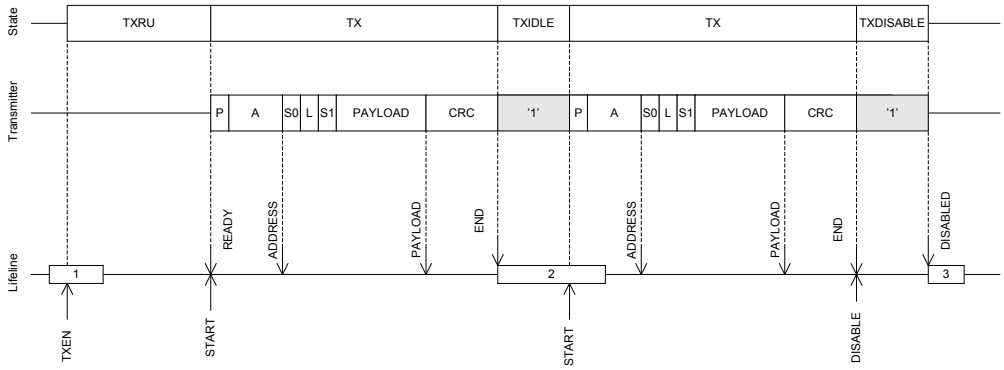

Figure 33: Transmission of multiple packets

21.1.9 Receive sequence

Before the RADIO is able to receive a packet, it must first ramp-up in RX mode

See RXRU in *Figure 30: Radio states* on page 203 and *Figure 34: Receive sequence* on page 205 etc.
An RXRU ramp-up sequence is initiated when the RXEN task is triggered. After the radio has successfully ramped up it will generate the READY event indicating that a packet reception can be initiated. A packet reception is initiated by triggering the START task. As illustrated in *Figure 30: Radio states* on page 203 the START task can, first be triggered after the RADIO has entered into the RXIDLE state.

Figure 34: Receive sequence on page 205 illustrates a single packet reception where the CPU manually triggers the different tasks needed to control the flow of the RADIO, i.e. no shortcuts are used. If shortcuts are not used, a certain amount of delay, caused by CPU execution, is expected between READY and START, and between END and DISABLE. As illustrated *Figure 34: Receive sequence* on page 205 the RADIO will be listening and possibly receiving undefined data, illustrated with an 'X', from START and until a packet with valid preamble (P) is received.

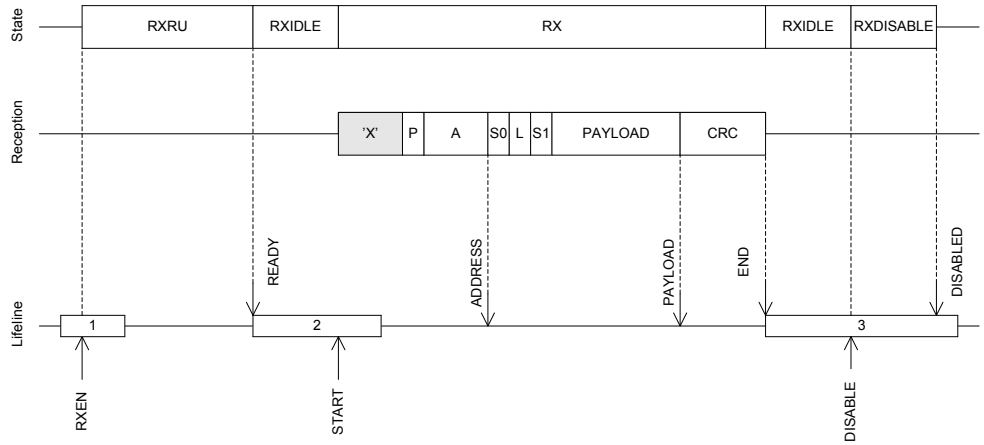

Figure 34: Receive sequence

A slightly modified version of the receive sequence from *Figure 34: Receive sequence* on page 205 is illustrated in *Figure 35: Receive sequence using shortcuts to avoid delays* on page 206 where the the RADIO is configured to use shortcuts between READY and START, and between END and DISABLE, which means that no delay is introduced.

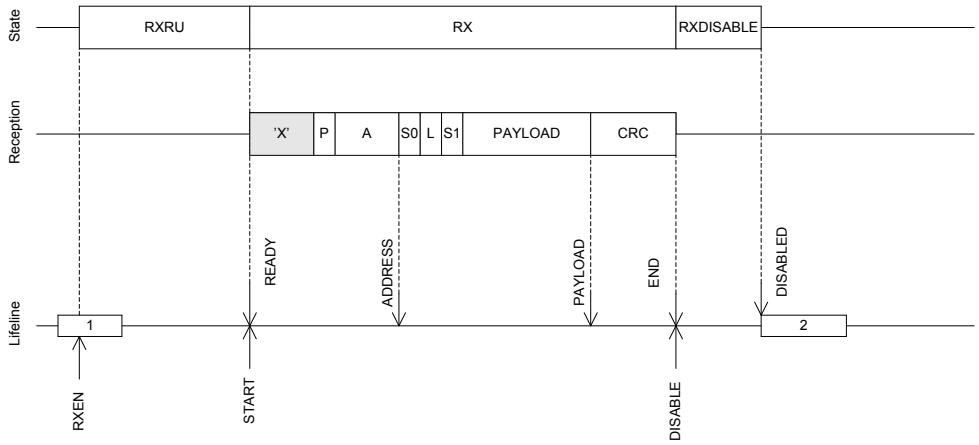

Figure 35: Receive sequence using shortcuts to avoid delays

The RADIO is able to receive multiple packets one after the other without having to disable and re-enable the RADIO between packets, this is illustrated *Figure 36: Reception of multiple packets* on page 206.

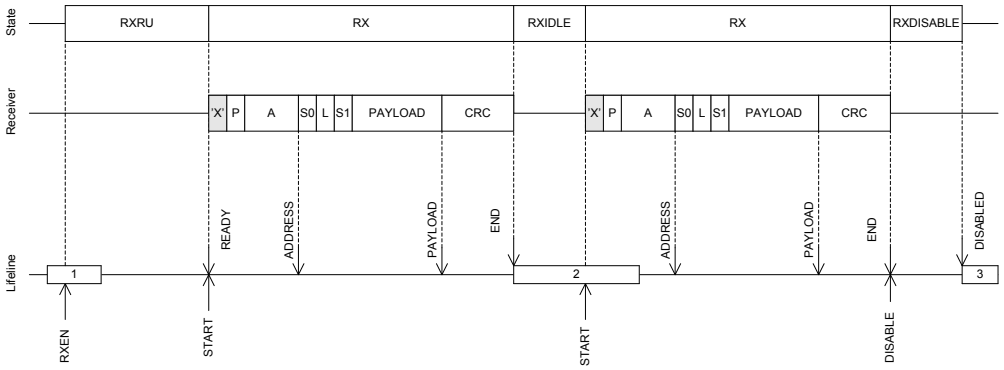

Figure 36: Reception of multiple packets

21.1.10 Received Signal Strength Indicator (RSSI)

The radio implements a mechanism for measuring the power in the received radio signal. This feature is called Received Signal Strength Indicator (RSSI).

Sampling of the received signal strength is started by using the RSSISTART task. The sample can be read from the RSSISAMPLE register.

The sample period of the RSSI is defined by $RSSI_{PERIOD}$, see the device product specification for details. The RSSI sample will hold the average received signal strength during this sample period.

For the RSSI sample to be valid the radio has to be enabled in receive mode (RXEN task) and the reception has to be started (READY event followed by START task).

21.1.11 Interframe spacing

Interframe spacing is the time interval between two consecutive packets.

It is defined as the time, in micro seconds, from the end of the last bit of the previous packet received and to the start of the first bit of the subsequent packet that is transmitted. The RADIO is able to enforce this

interval as specified in the TIFS register as long as TIFS is not specified to be shorter than the RADIO's turn-around time [15], i.e. the time needed to switch off the receiver, and switch back on the transmitter.

TIFS is only enforced if END_DISABLE and DISABLED_TXEN shortcuts are enabled. TIFS is only qualified for use in BLE_1MBIT mode.

21.1.12 Device address match

The device address match feature is tailored for address white listing in a Bluetooth Smart and similar implementations.

This feature enables on-the-fly device address matching while receiving a packet on air. This feature only works in receive mode and as long as RADIO is configured for little endian, see PCNF1.ENDIAN.

The Device Address match unit assumes that the 48 first bits of the payload is the device address and that bit number 6 in S0 is the TxAdd bit. See the Bluetooth Core Specification for more information about device addresses, TxAdd and white listing.

The RADIO is able to listen for 8 different device addresses at the same time. These addresses are specified in a DAB/DAP register pair, one pair per address, in addition to a TxAdd bit configured in the DACNF register. The DAB register specifies the 32 least significant bits of the device address, while the DAP register specifies the 16 most significant bits of the device address.

Each of the device addresses can be individually included or excluded from the matching mechanism. This is configured in the DACNF register.

21.1.13 Bit counter

The RADIO implements a simple counter that can be configured to generate an event after a specific number of bits have been transmitted or received.

By using shortcuts, this counter can be started from different events generated by the RADIO and hence count relative to these.

The bit counter is started by triggering the BCSTART task, and stopped by triggering the BCSTOP task. A BCMATCH event will be generated when the bit counter has counted the number of bits specified in the BCC register. The bit counter will continue to count bits until the DISABLED event is generated or until the BCSTOP task is triggered. The CPU can therefore, after a BCMATCH event, reconfigure the BCC value for new BCMATCH events within the same packet.

The bit counter can only be started after the RADIO has received the ADDRESS event.

The bit counter will stop and reset on BCSTOP, STOP, END and DISABLE tasks.

The figure below illustrates how the bit counter can be used to generate a BCMATCH event in the beginning of the packet payload, and again generate a second BCMATCH event after sending 2 bytes (16 bits) of the payload.

[15] See product specification for more information on the timing value t_{TXEN}.

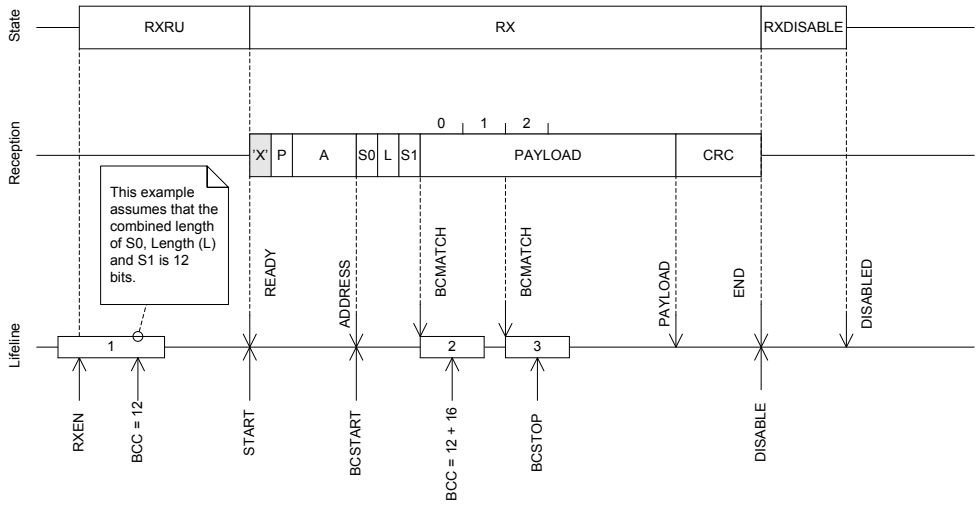

Figure 37: Bit counter example

21.2 Registers

Table 34: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40001000	RADIO	RADIO	2.4 GHz radio	

Table 35: Register Overview

Register	Offset	Description
TASKS_TXEN	0x000	Enable RADIO in TX mode
TASKS_RXEN	0x004	Enable RADIO in RX mode
TASKS_START	0x008	Start RADIO
TASKS_STOP	0x00C	Stop RADIO
TASKS_DISABLE	0x010	Disable RADIO
TASKS_RSSISTART	0x014	Start the RSSI and take one single sample of the receive signal strength.
TASKS_RSSISTOP	0x018	Stop the RSSI measurement
TASKS_BCSTART	0x01C	Start the bit counter
TASKS_BCSTOP	0x020	Stop the bit counter
EVENTS_READY	0x100	RADIO has ramped up and is ready to be started
EVENTS_ADDRESS	0x104	Address sent or received
EVENTS_PAYLOAD	0x108	Packet payload sent or received
EVENTS_END	0x10C	Packet sent or received
EVENTS_DISABLED	0x110	RADIO has been disabled
EVENTS_DEVMATCH	0x114	A device address match occurred on the last received packet
EVENTS_DEVMISS	0x118	No device address match occurred on the last received packet
EVENTS_RSSIEND	0x11C	Sampling of receive signal strength complete. A new RSSI sample is ready for readout from the *RSSISAMPLE* on page 218 register
EVENTS_BCMATCH	0x128	Bit counter reached bit count value specified in the *BCC* on page 219 register
EVENTS_CRCOK	0x130	Packet received with CRC ok
EVENTS_CRCERROR	0x134	Packet received with CRC error
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
CRCSTATUS	0x400	CRC status
RXMATCH	0x408	Received address

Register	Offset	Description	
RXCRC	0x40C	CRC field of previously received packet	
DAI	0x410	Device address match index	
PACKETPTR	0x504	Packet pointer	
FREQUENCY	0x508	Frequency	
TXPOWER	0x50C	Output power	
MODE	0x510	Data rate and modulation	
PCNF0	0x514	Packet configuration register 0	
PCNF1	0x518	Packet configuration register 1	
BASE0	0x51C	Base address 0	
BASE1	0x520	Base address 1	
PREFIX0	0x524	Prefixes bytes for logical addresses 0-3	
PREFIX1	0x528	Prefixes bytes for logical addresses 4-7	
TXADDRESS	0x52C	Transmit address select	
RXADDRESSES	0x530	Receive address select	
CRCCNF	0x534	CRC configuration	
CRCPOLY	0x538	CRC polynomial	
CRCINIT	0x53C	CRC initial value	
	0x540		Reserved
TIFS	0x544	Inter Frame Spacing in us	
RSSISAMPLE	0x548	RSSI sample	
STATE	0x550	Current radio state	
DATAWHITEIV	0x554	Data whitening initial value	
BCC	0x560	Bit counter compare	
DAB[0]	0x600	Device address base segment 0	
DAB[1]	0x604	Device address base segment 1	
DAB[2]	0x608	Device address base segment 2	
DAB[3]	0x60C	Device address base segment 3	
DAB[4]	0x610	Device address base segment 4	
DAB[5]	0x614	Device address base segment 5	
DAB[6]	0x618	Device address base segment 6	
DAB[7]	0x61C	Device address base segment 7	
DAP[0]	0x620	Device address prefix 0	
DAP[1]	0x624	Device address prefix 1	
DAP[2]	0x628	Device address prefix 2	
DAP[3]	0x62C	Device address prefix 3	
DAP[4]	0x630	Device address prefix 4	
DAP[5]	0x634	Device address prefix 5	
DAP[6]	0x638	Device address prefix 6	
DAP[7]	0x63C	Device address prefix 7	
DACNF	0x640	Device address match configuration	
MODECNF0	0x650	Radio mode configuration register 0	
POWER	0xFFC	Peripheral power control	

21.2.1 SHORTS

Address offset: 0x200

Shortcut register

Bit number																															
Id																					H		G	F	E	D	C	B	A		
Reset 0x00000000																					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	READY_START			Shortcut between *EVENTS_READY* event and *TASKS_START* task
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
B	RW	END_DISABLE			Shortcut between *EVENTS_END* event and *TASKS_DISABLE* task
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
C	RW	DISABLED_TXEN			Shortcut between *EVENTS_DISABLED* event and *TASKS_TXEN* task
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
D	RW	DISABLED_RXEN			Shortcut between *EVENTS_DISABLED* event and *TASKS_RXEN* task
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
E	RW	ADDRESS_RSSISTART			Shortcut between *EVENTS_ADDRESS* event and *TASKS_RSSISTART* task
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
F	RW	END_START			Shortcut between *EVENTS_END* event and *TASKS_START* task
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
G	RW	ADDRESS_BCSTART			Shortcut between *EVENTS_ADDRESS* event and *TASKS_BCSTART* task
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
H	RW	DISABLED_RSSISTOP			Shortcut between *EVENTS_DISABLED* event and *TASKS_RSSISTOP* task
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut

21.2.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				L K I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	READY			Write '1' to Enable interrupt on *EVENTS_READY* event
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
B	RW	ADDRESS			Write '1' to Enable interrupt on *EVENTS_ADDRESS* event
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
C	RW	PAYLOAD			Write '1' to Enable interrupt on *EVENTS_PAYLOAD* event
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	END			Write '1' to Enable interrupt on *EVENTS_END* event
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
E	RW	DISABLED			Write '1' to Enable interrupt on *EVENTS_DISABLED* event
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW	DEVMATCH			Write '1' to Enable interrupt on *EVENTS_DEVMATCH* event
			Set	1	Enable

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																						L	K		I			H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Disabled	0																															
			Enabled	1																															
G	RW	DEVMISS																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
H	RW	RSSIEND																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
I	RW	BCMATCH																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
K	RW	CRCOK																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
L	RW	CRCERROR																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															

21.2.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																						L	K		I			H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	READY																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	ADDRESS																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	PAYLOAD																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
D	RW	END																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
E	RW	DISABLED																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
F	RW	DEVMATCH																																	
			Clear	1																															
			Disabled	0																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																						L	K		I			H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Enabled	1																															
G	RW	DEVMISS																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
H	RW	RSSIEND																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
I	RW	BCMATCH																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
K	RW	CRCOK																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
L	RW	CRCERROR																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															

21.2.4 CRCSTATUS

Address offset: 0x400

CRC status

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	CRCSTATUS																																	
			CRCError	0																															
			CRCOk	1																															

21.2.5 RXMATCH

Address offset: 0x408

Received address

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																A	A	A	
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	RXMATCH																																	
				Logical address of which previous packet was received																															

21.2.6 RXCRC

Address offset: 0x40C

CRC field of previously received packet

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id									A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	R	RXCRC			CRC field of previously received packet CRC field of previously received packet

21.2.7 DAI

Address offset: 0x410

Device address match index

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																														A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	R	DAI			Device address match index Index (n) of device address, see DAB[n] and DAP[n], that got an address match.

21.2.8 PACKETPTR

Address offset: 0x504

Packet pointer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	PACKETPTR			Packet pointer Packet address to be used for the next transmission or reception. When transmitting, the packet pointed to by this address will be transmitted and when receiving, the received packet will be written to this address. This address is a byte aligned ram address.

21.2.9 FREQUENCY

Address offset: 0x508

Frequency

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																										A	A	A	A	A	A	A
Reset 0x00000002	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	FREQUENCY		[0..100]	Radio channel frequency Frequency = 2400 + FREQUENCY (MHz).

21.2.10 TXPOWER

Address offset: 0x50C

Output power

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																									A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TXPOWER			RADIO output power.

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A
Reset 0x00000000			**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**Value Id**	**Value**	**Description**
			Output power in number of dBm, i.e. if the value -20 is specified
			the output power will be set to -20dBm.
	Pos4dBm	0x04	+4 dBm
	Pos3dBm	0x03	+3 dBm
	0dBm	0x00	0 dBm
	Neg4dBm	0xFC	-4 dBm
	Neg8dBm	0xF8	-8 dBm
	Neg12dBm	0xF4	-12 dBm
	Neg16dBm	0xF0	-16 dBm
	Neg20dBm	0xEC	-20 dBm
	Neg30dBm	0xD8	-40 dBm Deprecated
	Neg40dBm	0xD8	-40 dBm

21.2.11 MODE

Address offset: 0x510

Data rate and modulation

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	MODE			Radio data rate and modulation setting. The radio supports
					Frequency-shift Keying (FSK) modulation.
			Nrf_1Mbit	0	1 Mbit/s Nordic proprietary radio mode
			Nrf_2Mbit	1	2 Mbit/s Nordic proprietary radio mode
			Nrf_250Kbit	2	250 kbit/s Nordic proprietary radio mode Deprecated
			Ble_1Mbit	3	1 Mbit/s Bluetooth Low Energy

21.2.12 PCNF0

Address offset: 0x514

Packet configuration register 0

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				G F E E E E C A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	LFLEN			Length on air of LENGTH field in number of bits.
C	RW	S0LEN			Length on air of S0 field in number of bytes.
E	RW	S1LEN			Length on air of S1 field in number of bits.
F	RW	S1INCL			Include or exclude S1 field in RAM
			Automatic	0	Include S1 field in RAM only if S1LEN > 0
			Include	1	Always include S1 field in RAM independent of S1LEN
G	RW	PLEN			Length of preamble on air. Decision point: *Registers* on page
					208 task
			8bit	0	8-bit preamble
			16bit	1	16-bit preamble

21.2.13 PCNF1

Address offset: 0x518

Packet configuration register 1

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id										E	D						C	C	C	B	B	B	B	B	B	B	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	MAXLEN		[0..255]																															
				Maximum length of packet payload. If the packet payload is larger than MAXLEN, the radio will truncate the payload to MAXLEN.																																
B	RW	STATLEN		[0..255]																															
				Static length in number of bytes The static length parameter is added to the total length of the payload when sending and receiving packets, e.g. if the static length is set to N the radio will receive or send N bytes more than what is defined in the LENGTH field of the packet.																																
C	RW	BALEN		[2..4]																															
				Base address length in number of bytes The address field is composed of the base address and the one byte long address prefix, e.g. set BALEN=2 to get a total address of 3 bytes.																																
D	RW	ENDIAN																																	
				On air endianness of packet, this applies to the S0, LENGTH, S1 and the PAYLOAD fields.																																
			Little	0																															
				Least Significant bit on air first																																
			Big	1																															
				Most significant bit on air first																																
E	RW	WHITEEN																																	
				Enable or disable packet whitening																																
			Disabled	0																															
				Disable																																
			Enabled	1																															
				Enable																																

21.2.14 BASE0

Address offset: 0x51C

Base address 0

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	BASE0																																	
				Base address 0 Radio base address 0.																																

21.2.15 BASE1

Address offset: 0x520

Base address 1

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	BASE1																																	
				Base address 1 Radio base address 1.																																

21.2.16 PREFIX0

Address offset: 0x524

Prefixes bytes for logical addresses 0-3

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				D	D	D	D	D	D	D	D	C	C	C	C	C	C	C	C	B	B	B	B	B	B	B	B	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	AP0																																	
				Address prefix 0.																																

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				D	D	D	D	D	D	D	D	C	C	C	C	C	C	C	C	B	B	B	B	B	B	B	B	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
B	RW	AP1																																	
				Address prefix 1.																																	
C	RW	AP2																																	
				Address prefix 2.																																	
D	RW	AP3																																	
				Address prefix 3.																																	

21.2.17 PREFIX1

Address offset: 0x528

Prefixes bytes for logical addresses 4-7

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				D	D	D	D	D	D	D	D	C	C	C	C	C	C	C	C	B	B	B	B	B	B	B	B	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	AP4																																	
				Address prefix 4.																																	
B	RW	AP5																																	
				Address prefix 5.																																	
C	RW	AP6																																	
				Address prefix 6.																																	
D	RW	AP7																																	
				Address prefix 7.																																	

21.2.18 TXADDRESS

Address offset: 0x52C

Transmit address select

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	TXADDRESS																																	
				Transmit address select Logical address to be used when transmitting a packet.																																	

21.2.19 RXADDRESSES

Address offset: 0x530

Receive address select

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	ADDR0																																	
				Enable or disable reception on logical address 0.																																	
			Disabled	0																																	
				Disable																																	
			Enabled	1																																	
				Enable																																	
B	RW	ADDR1																																	
				Enable or disable reception on logical address 1.																																	
			Disabled	0																																	
				Disable																																	
			Enabled	1																																	
				Enable																																	
C	RW	ADDR2																																	
				Enable or disable reception on logical address 2.																																	
			Disabled	0																																	
				Disable																																	
			Enabled	1																																	
				Enable																																	
D	RW	ADDR3																																	
				Enable or disable reception on logical address 3.																																	
			Disabled	0																																	
				Disable																																	
			Enabled	1																																	
				Enable																																	
E	RW	ADDR4																																	
				Enable or disable reception on logical address 4.																																	
			Disabled	0																																	
				Disable																																	
			Enabled	1																																	
				Enable																																	
F	RW	ADDR5																																	
				Enable or disable reception on logical address 5.																																	

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Disabled	0																															
			Enabled	1																															
G	RW	ADDR6																																	
			Disabled	0																															
			Enabled	1																															
H	RW	ADDR7																																	
			Disabled	0																															
			Enabled	1																															

21.2.20 CRCCNF

Address offset: 0x534

CRC configuration

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																											B							A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	LEN		[1..3]																															
			Disabled	0																															
			One	1																															
			Two	2																															
			Three	3																															
B	RW	SKIPADDR																																	
			Include	0																															
			Skip	1																															

21.2.21 CRCPOLY

Address offset: 0x538

CRC polynomial

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id												A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	CRCPOLY																																	
				CRC polynomial Each term in the CRC polynomial is mapped to a bit in this register which index corresponds to the term's exponent. The least significant term/bit is hard-wired internally to 1, and bit number 0 of the register content is ignored by the hardware. The following example is for an 8 bit CRC polynomial: x8 + x7 + x3 + x2 + 1 = 1 1000 1101 .																																		

21.2.22 CRCINIT

Address offset: 0x53C

CRC initial value

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id												A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	CRCINIT																																	
				CRC initial value																															

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id									A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
					Initial value for CRC calculation.

21.2.23 TIFS

Address offset: 0x544

Inter Frame Spacing in us

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																									A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TIFS			Inter Frame Spacing in us Inter frame space is the time interval between two consecutive packets. It is defined as the time, in micro seconds, from the end of the last bit of the previous packet to the start of the first bit of the subsequent packet.

21.2.24 RSSISAMPLE

Address offset: 0x548

RSSI sample

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																										A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	R	RSSISAMPLE		[0..127]	RSSI sample RSSI sample result. The value of this register is read as a positive value while the actual received signal strength is a negative value. Actual received signal strength is therefore as follows: received signal strength = -A dBm

21.2.25 STATE

Address offset: 0x550

Current radio state

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																													A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	R	STATE			Current radio state
			Disabled	0	RADIO is in the Disabled state
			RxRu	1	RADIO is in the RXRU state
			RxIdle	2	RADIO is in the RXIDLE state
			Rx	3	RADIO is in the RX state
			RxDisable	4	RADIO is in the RXDISABLED state
			TxRu	9	RADIO is in the TXRU state
			TxIdle	10	RADIO is in the TXIDLE state
			Tx	11	RADIO is in the TX state
			TxDisable	12	RADIO is in the TXDISABLED state

21.2.26 DATAWHITEIV

Address offset: 0x554

Data whitening initial value

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																													A	A	A	A	A	A	A
Reset 0x00000040				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DATAWHITEIV																											Data whitening initial value. Bit 6 is hard-wired to '1', writing '0' to it has no effect, and it will always be read back and used by the device as '1'. Bit 0 corresponds to Position 6 of the LSFR, Bit 1 to Position 5, etc.							

21.2.27 BCC

Address offset: 0x560

Bit counter compare

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	BCC																											Bit counter compare Bit counter compare register							

21.2.28 DAB[0]

Address offset: 0x600

Device address base segment 0

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DAB																											Device address base segment 0						

21.2.29 DAB[1]

Address offset: 0x604

Device address base segment 1

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DAB																											Device address base segment 1						

21.2.30 DAB[2]

Address offset: 0x608

Device address base segment 2

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DAB																											Device address base segment 2						

21.2.31 DAB[3]

Address offset: 0x60C

Device address base segment 3

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	DAB			Device address base segment 3

21.2.32 DAB[4]

Address offset: 0x610

Device address base segment 4

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	DAB			Device address base segment 4

21.2.33 DAB[5]

Address offset: 0x614

Device address base segment 5

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	DAB			Device address base segment 5

21.2.34 DAB[6]

Address offset: 0x618

Device address base segment 6

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	DAB			Device address base segment 6

21.2.35 DAB[7]

Address offset: 0x61C

Device address base segment 7

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	DAB			Device address base segment 7

21.2.36 DAP[0]

Address offset: 0x620

Device address prefix 0

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	DAP			Device address prefix 0

21.2.37 DAP[1]

Address offset: 0x624

Device address prefix 1

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	DAP			Device address prefix 1

21.2.38 DAP[2]

Address offset: 0x628

Device address prefix 2

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	DAP			Device address prefix 2

21.2.39 DAP[3]

Address offset: 0x62C

Device address prefix 3

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	DAP			Device address prefix 3

21.2.40 DAP[4]

Address offset: 0x630

Device address prefix 4

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	DAP			Device address prefix 4

21.2.41 DAP[5]

Address offset: 0x634

Device address prefix 5

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	DAP			Device address prefix 5

21.2.42 DAP[6]

Address offset: 0x638

Device address prefix 6

Bit number					31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																					A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																															
A	RW	DAP			Device address prefix 6																															

21.2.43 DAP[7]

Address offset: 0x63C

Device address prefix 7

Bit number					31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																					A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																															
A	RW	DAP			Device address prefix 7																															

21.2.44 DACNF

Address offset: 0x640

Device address match configuration

Bit number					31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																					P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																															
A	RW	ENA0			Enable or disable device address matching using device address 0																															
			Disabled	0	Disabled																															
			Enabled	1	Enabled																															
B	RW	ENA1			Enable or disable device address matching using device address 1																															
			Disabled	0	Disabled																															
			Enabled	1	Enabled																															
C	RW	ENA2			Enable or disable device address matching using device address 2																															
			Disabled	0	Disabled																															
			Enabled	1	Enabled																															
D	RW	ENA3			Enable or disable device address matching using device address 3																															
			Disabled	0	Disabled																															
			Enabled	1	Enabled																															
E	RW	ENA4			Enable or disable device address matching using device address 4																															
			Disabled	0	Disabled																															
			Enabled	1	Enabled																															
F	RW	ENA5			Enable or disable device address matching using device address 5																															
			Disabled	0	Disabled																															
			Enabled	1	Enabled																															
G	RW	ENA6			Enable or disable device address matching using device address 6																															
			Disabled	0	Disabled																															
			Enabled	1	Enabled																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																				P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
H	RW	ENA7																																	
			Disabled	0																															
			Enabled	1																															
I	RW	TXADD0																																	
J	RW	TXADD1																																	
K	RW	TXADD2																																	
L	RW	TXADD3																																	
M	RW	TXADD4																																	
N	RW	TXADD5																																	
O	RW	TXADD6																																	
P	RW	TXADD7																																	

21.2.45 MODECNF0

Address offset: 0x650

Radio mode configuration register 0

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																										C	C								A
Reset 0x00000200				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	RU																																	
			Default	0																															
			Fast	1																															
C	RW	DTX																																	
			B1	0																															
			B0	1																															
			Center	2																															

Default TX value

Specifies what the RADIO will transmit when it is not started, i.e. between:

Registers on page 208 and *Registers* on page 208

Registers on page 208 and *Registers* on page 208

Registers on page 208 and *Registers* on page 208

Transmit '1'

Transmit '0'

Transmit center frequency

When tuning the crystal for centre frequency, the RADIO must be set in DTX = Center mode to be able to achieve the expected accuracy.

21.2.46 POWER

Address offset: 0xFFC

Peripheral power control

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000001				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	POWER																																	
			Disabled	0																															
			Enabled	1																															

Peripheral power control. The peripheral and its registers will be reset to its initial state by switching the peripheral off and then back on again.

Peripheral is powered off

Peripheral is powered on

21.3 Electrical Specification

21.3.1 General Radio Characteristics

Symbol	Description	Min.	Typ.	Max.	Units
f_{OP}	Operating frequencies	2360		2500	MHz
$f_{PLL,PROG,RES}$	PLL programming resolution		2		kHz
$f_{PLL,CH,SP}$	PLL channel spacing		1		MHz
$f_{DELTA,1M}$	Frequency deviation @ 1 Msps		±170		kHz
$f_{DELTA,BLE,1M}$	Frequency deviation @ BLE 1Msps		±250		kHz
$f_{DELTA,2M}$	Frequency deviation @ 2 Msps		±320		kHz
fsk_{SPS}	On-the-air data rate	1		2	Msps

21.3.2 Radio current consumption (Transmitter)

Symbol	Description	Min.	Typ.	Max.	Units
$I_{TX,PLUS6dBM,DCDC}$	TX only run current (DCDC, 3V) P_{RF} =+4 dBm		7.9		mA
$I_{TX,PLUS6dBM}$	TX only run current P_{RF} = +4 dBm		14.4		mA
$I_{TX,0dBM,DCDC}$	TX only run current (DCDC, 3V)P_{RF} = 0dBm		5.4		mA
$I_{TX,0dBM}$	TX only run current P_{RF} = 0dBm		9.6		mA
$I_{TX,MINUS4dBM,DCDC}$	TX only run current DCDC, 3V P_{RF} = -4dBm		4.4		mA
$I_{TX,MINUS4dBM}$	TX only run current P_{RF} = -4 dBm		7.4		mA
$I_{TX,MINUS8dBM,DCDC}$	TX only run current DCDC, 3V P_{RF} = -8 dBm		4.0		mA
$I_{TX,MINUS8dBM}$	TX only run current P_{RF} = -8 dBm		6.6		mA
$I_{TX,MINUS12dBM,DCDC}$	TX only run current DCDC, 3V P_{RF} = -12 dBm		3.8		mA
$I_{TX,MINUS12dBM}$	TX only run current P_{RF} = -12 dBm		6.0		mA
$I_{TX,MINUS16dBM,DCDC}$	TX only run current DCDC, 3V P_{RF} = -16 dBm		3.6		mA
$I_{TX,MINUS16dBM}$	TX only run current P_{RF} = -16 dBm		5.5		mA
$I_{TX,MINUS20dBM,DCDC}$	TX only run current DCDC, 3V P_{RF} = -20 dBm		3.4		mA
$I_{TX,MINUS20dBM}$	TX only run current P_{RF} = -20 dBm		5.2		mA
$I_{TX,MINUS40dBM,DCDC}$	TX only run current DCDC, 3V P_{RF} = whisper mode		3.0		mA
$I_{TX,MINUS40dBM}$	TX only run current P_{RF} = whisper mode		4.2		mA
$I_{START,TX,DCDC}$	TX start-up current DCDC, 3V		[b]		mA
$I_{START,TX}$	TX start-up current		7[b]		mA

21.3.3 Radio current consumption (Receiver)

Symbol	Description	Min.	Typ.	Max.	Units
$I_{RX,1M,DCDC}$	RX only run current (DCDC, 3V) 1Msps / 1Msps BLE		6.1		mA
$I_{RX,1M}$	RX only run current 1Msps / 1Msps BLE High Sensitivity Mode		10.9		mA
$I_{RX,2M,DCDC}$	RX only run current (DCDC, 3V) 2Msps Mode		6.7		mA
$I_{RX,2M}$	RX only run current 2Msps Mode		12.1		mA
$I_{START,RX,1M,DCDC}$	RX start-up current (DCDC 3V) 1Msps / 1Msps BLE				mA
$I_{START,RX,1M}$	RX start-up current 1Msps / 1Msps BLE				mA

21.3.4 Transmitter specification

Symbol	Description	Min.	Typ.	Max.	Units
P_{RF}	Maximum output power			4	dBm
P_{RFC}	RF power control range		24		dB
P_{RFCR}	RF power accuracy			±4	dB
P_{WISP}	RF Power whisper mode		-40		dBm
P_{BW1}	20 dB bandwidth for modulated carrier (1 Msps)		1000[16]		kHz
$P_{BW1,BLE}$	20 dB bandwidth for modulated carrier (1 Msps, BLE)		1100		kHz

[b] Average current consumption (at 0 dBm TX output power) for TX startup (40 µs)

[16] Normal Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Units
P_{BW2}	20 dB bandwidth for modulated carrier (2 Msps)		1600[17]		kHz
$P_{RF1,1}$	1st Adjacent Channel Transmit Power 1 MHz (1 Msps)		-23	[a]	dBc
$P_{RF2,1}$	2nd Adjacent Channel Transmit Power 2 MHz (1 Msps)		-50	[a]	dBc
$P_{RF1,2}$	1st Adjacent Channel Transmit Power 2 MHz (2 Msps)		-24	[a]	dBc
$P_{RF2,2}$	2nd Adjacent Channel Transmit Power 4 MHz (2 Msps)		-50	[a]	dBc

21.3.5 Receiver operation

Symbol	Description	Min.	Typ.	Max.	Units
$P_{RX,MAX}$	Maximum received signal strength at < 0.1% PER		0		dBm
$P_{SENS,IT,1M}$	Sensitivity, 1Msps nRF mode[e]		-93		dBm
$P_{SENS,IT,SP,1M,BLE}$	Sensitivity, 1Msps BLE ideal transmitter, <=37 bytes BER=1E-3[c]		-96		dBm
$P_{SENS,DT,SP,1M,BLE}$	Sensitivity, 1Msps BLE dirty transmitter, <=37 bytes BER=1E-3[c]		-96		dBm
$P_{SENS,IT,LP,1M,BLE}$	Sensitivity, 1Msps BLE ideal transmitter >=128 bytes BER=1E-4[d]		-95		dBm
$P_{SENS,DT,LP,1M,BLE}$	Sensitivity, 1Msps BLE dirty transmitter >=128 bytes BER=1E-4[d]		-95		dBm
$P_{SENS,IT,2M}$	Sensitivity, 2Msps nRF mode[e]		-89		dBm

21.3.6 RX selectivity

RX selectivity with equal modulation on interfering signal[18]

Symbol	Description	Min.	Typ.	Max.	Units
$C/I_{1M,co\text{-}channel}$	1Msps mode, Co-Channel interference		9		dB
$C/I_{1M,-1MHz}$	1 Msps mode, Adjacent (-1 MHz) interference		-2		dB
$C/I_{1M,+1MHz}$	1 Msps mode, Adjacent (+1 MHz) interference		-10		dB
$C/I_{1M,-2MHz}$	1 Msps mode, Adjacent (-2 MHz) interference		-19		dB
$C/I_{1M,+2MHz}$	1 Msps mode, Adjacent (+2 MHz) interference		-42		dB
$C/I_{1M,-3MHz}$	1 Msps mode, Adjacent (-3 MHz) interference		-38		dB
$C/I_{1M,+3MHz}$	1 Msps mode, Adjacent (+3 MHz) interference		-48		dB
$C/I_{1M,\pm6MHz}$	1 Msps mode, Adjacent (≥6 MHz) interference		-50		dB
$C/I_{1MBLE,co\text{-}channel}$	1 Msps BLE mode, Co-Channel interference		6		dB
$C/I_{1MBLE,-1MHz}$	1 Msps BLE mode, Adjacent (-1 MHz) interference		-2		dB
$C/I_{1MBLE,+1MHz}$	1 Msps BLE mode, Adjacent (+1 MHz) interference		-9		dB
$C/I_{1MBLE,-2MHz}$	1 Msps BLE mode, Adjacent (-2 MHz) interference		-22		dB
$C/I_{1MBLE,+2MHz}$	1 Msps BLE mode, Adjacent (+2 MHz) interference		-46		dB
$C/I_{1MBLE,>3MHz}$	1 Msps BLE mode, Adjacent (≥3 MHz) interference		-50		dB
$C/I_{1MBLE,image}$	Image frequency Interference		-22		dB
$C/I_{1MBLE,image,1MHz}$	Adjacent (1 MHz) interference to in-band image frequency		-35		dB
$C/I_{2M,co\text{-}channel}$	2Msps mode, Co-Channel interference		10		dB
$C/I_{2M,-2MHz}$	2 Msps mode, Adjacent (-2 MHz) interference		6		dB
$C/I_{2M,+2MHz}$	2 Msps mode, Adjacent (+2 MHz) interference		-19		dB
$C/I_{2M,-4MHz}$	2 Msps mode, Adjacent (-4 MHz) interference		-20		dB
$C/I_{2M,+4MHz}$	2 Msps mode, Adjacent (+4 MHz) interference		-44		dB
$C/I_{2M,-6MHz}$	2 Msps mode, Adjacent (-6 MHz) interference		-42		dB
$C/I_{2M,+6MHz}$	2 Msps mode, Adjacent (+6 MHz) interference		-42		dB
$C/I_{2M,\geq12MHz}$	2 Msps mode, Adjacent (≥12 MHz) interference		-52		dB

17 Normal Operating Conditions

e Typical sensitivity applies when ADDR0 is used for receiver address correlation. When ADDR[1...7] are used for receiver address correlation, the typical sensitivity for this mode is degraded by 3dB.

c As defined in the Bluetooth Core Specification v4.0 Volume 6: Core System Package (Low Energy Controller Volume)

d Equivalent BER limit < 10E-04

18 Wanted signal level at PIN = -67 dBm. One interferer is used, having equal modulation as the wanted signal. The input power of the interferer where the sensitivity equals BER = 0.1% is presented

21.3.7 RX intermodulation

RX intermodulation[19]

Symbol	Description	Min.	Typ.	Max.	Units
$P_{IMD,1M}$	IMD performance, 1 Msps, 3rd, 4th, and 5th offset channel		-29		dBm
$P_{IMD,1M,BLE}$	MD performance, BLE 1 Msps, 3rd, 4th, and 5th offset channel		-30		dBm
$P_{IMD,2M}$	IMD performance, 2 Msps, 3rd, 4th, and 5th offset channel		-30		dBm

21.3.8 Radio timing

Symbol	Description	Min.	Typ.	Max.	Units
t_{TXEN}	Time between TXEN task and READY event after channel FREQUECNY configured		140		us
$t_{TXEN,FAST}$	Time between TXEN task and READY event after channel FREQUECNY configured (Fast Mode)		40		us
$t_{TXDISABLE}$	Time between DISABLE task and DISABLED event when the radio was in TX and mode is set to 1Msps		6		us
$t_{TXDISABLE,2M}$	Time between DISABLE task and DISABLED event when the radio was in TX and mode is set to 2Msps		4		us
t_{RXEN}	Time between the RXEN task and READY event after channel FREQUENCY configured in default mode		140		us
$t_{RXEN,FAST}$	Time between the RXEN task and READY event after channel FREQUENCY configured in fast mode		40		us
t_{SWITCH}	The minimum time taken to switch from RX to TX or TX to RX (channel FREQUENCY unchanged)		20		us
$t_{RXDISABLE}$	Time between DISABLE task and DISABLED event when the radio was in RX		0		us
$t_{TXCHAIN}$	TX chain delay		0.6		us
$t_{RXCHAIN}$	RX chain delay		9.4		us
$t_{RXCHAIN,2M}$	RX chain delay in 2Msps mode		5		us

21.3.9 Received Signal Strength Indicator (RSSI) specifications

Symbol	Description	Min.	Typ.	Max.	Units
$RSSI_{ACC}$	RSSI Accuracy Valid range -90 to -20 dBm		-2		dB
$RSSI_{RESOLUTION}$	RSSI resolution		1		dB
$RSSI_{PERIOD}$	Sample period		8		us
$RSSI_{CURRENT}$	Current consumption in addition to IRX		0		uA

21.3.10 Jitter

Symbol	Description	Min.	Typ.	Max.	Units
$t_{DISABLEDJITTER}$	Jitter on DISABLED event relative to END event when shortcut between END and DISABLE is enabled.		0.25		us
$t_{READYJITTER}$	Jitter on READY event relative to TXEN and RXEN task.		0.25		us

21.3.11 Delay when disabling the RADIO

Symbol	Description	Min.	Typ.	Max.	Units
$t_{TXDISABLE,1M}$	Disable delay from TX. Delay between DISABLE and DISABLED for MODE = Nrf_1Mbit and MODE = Ble_1Mbit		6		us
$t_{RXDISABLE,1M}$	Disable delay from RX. Delay between DISABLE and DISABLED for MODE = Nrf_1Mbit and MODE = Ble_1Mbit		0		us

[19] Wanted signal level at PIN = -64 dBm. Two interferers with equal input power are used. The interferer closest in frequency is not modulated, the other interferer is modulated equal with the wanted signal. The input power of the interferers where the sensitivity equals BER = 0.1% is presented.

22 Timer/counter (TIMER)

The TIMER can operate in two modes: timer and counter.

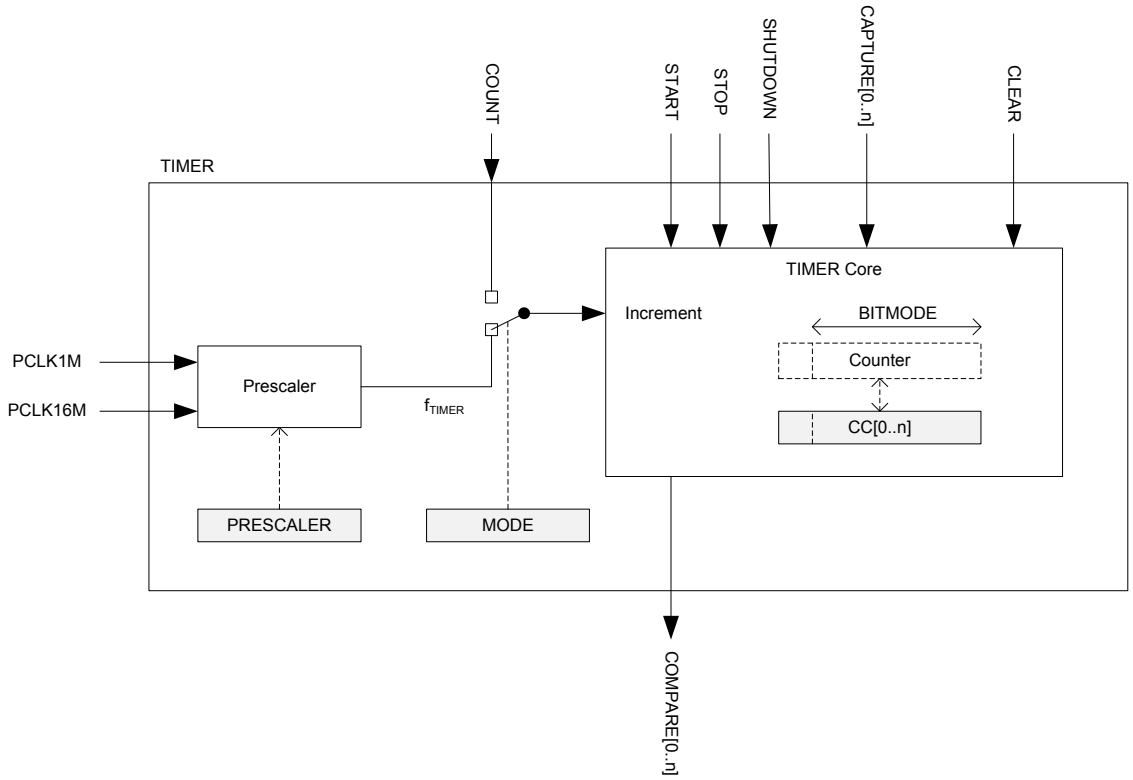

Figure 38: Block schematic for timer/counter

The timer/counter runs on the high-frequency clock source (HFCLK) and includes a four-bit (1/2X) prescaler that can divide the timers input clock from the HFCLK controller. Clock source selection between PCLK16M and PCLK1M is automatic according to TIMER base frequency set by the prescaler. The TIMER base frequency is always given as 16 MHz divided by the prescaler value.

The PPI system allows a TIMER event to to trigger a task of any other system peripheral of the device. The PPI system also enables the TIMER task/event features to generate periodic output and PWM signals to any GPIO. The number of input/outputs used at the same time is limited by the number of GPIOTE channels.

The TIMER can operate in two modes, Timer mode and Counter mode. In both modes, the TIMER is started by triggering the START task, and stopped by triggering the STOP task. After the timer is stopped the timer can resume timing/counting by triggering the START task again. When timing/counting is resumed the timer will continue from the value it had prior to being stopped.

If the timer does not need to be able to resume timing/counting after a STOP, the SHUTDOWN task could be used instead of or following the STOP task.

When the timer is shut down the internal core of the timer is switched off as illustrated in *Figure 38: Block schematic for timer/counter* on page 228. The timer must be shut down to reach the lowest power consumption in system ON mode. The startup time from shutdown state may be longer compared to starting the timer from the stopped state. See *Power management (POWER)* on page 79 for more information about power modes.

In Timer mode, the TIMER's internal Counter register is incremented by one for every tick of the timer frequency f_{TIMER} as illustrated in *Figure 38: Block schematic for timer/counter* on page 228. The

timer frequency is derived from PCLK16M as described in *Equation 1* using the values specified in the PRESCALER register:

$$f_{TIMER} = 16\ MHz\ /\ (2^{PRESCALER})$$

When f_{TIMER} <= 1 MHz the TIMER will use PCLK1M instead of PCLK16M for reduced power consumption.

In counter mode, the TIMER's internal Counter register is incremented by one each time the COUNT task is triggered, that is, the timer frequency and the prescaler are not utilized in counter mode. Similarly, the COUNT task has no effect in Timer mode.

The TIMER's maximum value is configured by changing the bit-width of the timer in the BITMODE register.

The PRESCALER register and the BITMODE register must only be updated when the timer is stopped. If these registers are updated while the TIMER is started then this may result in unpredictable behavior.

When the timer is incremented beyond its maximum value the Counter register will overflow and the TIMER will automatically start over from zero.

The Counter register can be cleared, that is, its internal value set to zero explicitly, by triggering the CLEAR task.

The TIMER implements multiple capture/compare registers.

Independent of prescaler setting the accuracy of the TIMER is equivalent to one tick of the timer frequency f_{TIMER} as illustrated in *Figure 38: Block schematic for timer/counter* on page 228.

22.1 Capture

The TIMER implements one capture task for every available capture/compare register.

Every time the CAPTURE[n] task is triggered the Counter value is copied to the CC[n] register.

22.2 Compare

The TIMER implements one COMPARE event for every available capture/compare register.

A COMPARE event is generated when the Counter is incremented and then becomes equal to the value specified in one of the capture compare registers. When the Counter value becomes equal to the value specified in a capture compare register CC[n], the corresponding compare event COMPARE[n] is generated.

BITMODE specifies how many bits of the Counter register and the capture/compare register that are used when the comparison is performed. Other bits will be ignored.

22.3 Task delays

TIMER task delays

After the TIMER is started, the CLEAR task, COUNT task and the STOP task will guarantee to take effect within one clock cycle of the PCLK16M. Depending on sub-power mode, the START task may require longer time to take effect, see *Timers Electrical Specification* on page 235. See *POWER* chapter for more information about sub-power modes.

If the TIMER is used in low power counter mode the COUNT task is not guaranteed to take effect within one clock cycle of PCLK16M. See *Timers Electrical Specification* on page 235 for information on power consumption, and response time of the COUNT task, in low power mode. The TIMER is not able to detect new COUNT tasks during the response time of a COUNT task.

22.4 Task priority

If the START task and the STOP task are triggered at the same time, that is, within the same period of PCLK16M, the STOP task will be prioritized.

22.5 Registers

Table 36: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40008000	TIMER	TIMER0	Timer 0	This timer instance has 4 CC registers
0x40009000	TIMER	TIMER1	Timer 1	This timer instance has 4 CC registers
0x4000A000	TIMER	TIMER2	Timer 2	This timer instance has 4 CC registers
0x4001A000	TIMER	TIMER3	Timer 3	This timer instance has 6 CC registers
0x4001B000	TIMER	TIMER4	Timer 4	This timer instance has 6 CC registers

Table 37: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start Timer
TASKS_STOP	0x004	Stop Timer
TASKS_COUNT	0x008	Increment Timer (Counter mode only)
TASKS_CLEAR	0x00C	Clear time
TASKS_SHUTDOWN	0x010	Shut down timer
TASKS_CAPTURE[0]	0x040	Capture Timer value to CC[0] register
TASKS_CAPTURE[1]	0x044	Capture Timer value to CC[1] register
TASKS_CAPTURE[2]	0x048	Capture Timer value to CC[2] register
TASKS_CAPTURE[3]	0x04C	Capture Timer value to CC[3] register
TASKS_CAPTURE[4]	0x050	Capture Timer value to CC[4] register
TASKS_CAPTURE[5]	0x054	Capture Timer value to CC[5] register
EVENTS_COMPARE[0]	0x140	Compare event on CC[0] match
EVENTS_COMPARE[1]	0x144	Compare event on CC[1] match
EVENTS_COMPARE[2]	0x148	Compare event on CC[2] match
EVENTS_COMPARE[3]	0x14C	Compare event on CC[3] match
EVENTS_COMPARE[4]	0x150	Compare event on CC[4] match
EVENTS_COMPARE[5]	0x154	Compare event on CC[5] match
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
MODE	0x504	Timer mode selection
BITMODE	0x508	Configure the number of bits used by the TIMER
PRESCALER	0x510	Timer prescaler register
CC[0]	0x540	Capture/Compare register 0
CC[1]	0x544	Capture/Compare register 1
CC[2]	0x548	Capture/Compare register 2
CC[3]	0x54C	Capture/Compare register 3
CC[4]	0x550	Capture/Compare register 4
CC[5]	0x554	Capture/Compare register 5

22.5.1 SHORTS

Address offset: 0x200

Shortcut register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																						L	K	J	I	H	G			F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	COMPARE0_CLEAR																																	
			Disabled	0																															
			Enabled	1																															
B	RW	COMPARE1_CLEAR																																	
			Disabled	0																															
			Enabled	1																															
C	RW	COMPARE2_CLEAR																																	
			Disabled	0																															
			Enabled	1																															
D	RW	COMPARE3_CLEAR																																	
			Disabled	0																															
			Enabled	1																															
E	RW	COMPARE4_CLEAR																																	
			Disabled	0																															
			Enabled	1																															
F	RW	COMPARE5_CLEAR																																	
			Disabled	0																															
			Enabled	1																															
G	RW	COMPARE0_STOP																																	
			Disabled	0																															
			Enabled	1																															
H	RW	COMPARE1_STOP																																	
			Disabled	0																															
			Enabled	1																															
I	RW	COMPARE2_STOP																																	
			Disabled	0																															
			Enabled	1																															
J	RW	COMPARE3_STOP																																	
			Disabled	0																															
			Enabled	1																															
K	RW	COMPARE4_STOP																																	
			Disabled	0																															
			Enabled	1																															
L	RW	COMPARE5_STOP																																	
			Disabled	0																															
			Enabled	1																															

22.5.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id														F	E	D	C	B	A																
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	COMPARE0																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	COMPARE1																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	COMPARE2																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
D	RW	COMPARE3																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
E	RW	COMPARE4																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
F	RW	COMPARE5																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															

22.5.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id														F	E	D	C	B	A																
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	COMPARE0																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	COMPARE1																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	COMPARE2																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
D	RW	COMPARE3																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
E	RW	COMPARE4																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
F	RW	COMPARE5																																	

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id													F	E	D	C	B	A																
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
			Clear								1																Disable							
			Disabled								0																Read: Disabled							
			Enabled								1																Read: Enabled							

22.5.4 MODE

Address offset: 0x504

Timer mode selection

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																	A	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	RW	MODE																									Timer mode							
			Timer								0																Select Timer mode							
			Counter								1																Select Counter mode							
			LowPowerCounter								2																Select Low Power Counter mode							

22.5.5 BITMODE

Address offset: 0x508

Configure the number of bits used by the TIMER

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																	A	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	RW	BITMODE																									Timer bit width							
			16Bit								0																16 bit timer bit width							
			08Bit								1																8 bit timer bit width							
			24Bit								2																24 bit timer bit width							
			32Bit								3																32 bit timer bit width							

22.5.6 PRESCALER

Address offset: 0x510

Timer prescaler register

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															A	A	A	A
Reset 0x00000004			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	RW	PRESCALER									[0..9]																Prescaler value							

22.5.7 CC[0]

Address offset: 0x540

Capture/Compare register 0

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	RW	CC																									Capture/Compare value							

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
					Only the number of bits indicated by BITMODE will be used by the TIMER.

22.5.8 CC[1]

Address offset: 0x544

Capture/Compare register 1

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	CC			Capture/Compare value Only the number of bits indicated by BITMODE will be used by the TIMER.

22.5.9 CC[2]

Address offset: 0x548

Capture/Compare register 2

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	CC			Capture/Compare value Only the number of bits indicated by BITMODE will be used by the TIMER.

22.5.10 CC[3]

Address offset: 0x54C

Capture/Compare register 3

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	CC			Capture/Compare value Only the number of bits indicated by BITMODE will be used by the TIMER.

22.5.11 CC[4]

Address offset: 0x550

Capture/Compare register 4

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	CC			Capture/Compare value Only the number of bits indicated by BITMODE will be used by the TIMER.

22.5.12 CC[5]

Address offset: 0x554

Capture/Compare register 5

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	CC			Capture/Compare value Only the number of bits indicated by BITMODE will be used by the TIMER.

22.6 Electrical Specification

22.6.1 Timers Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
I_{TIMER}	Timer run current without pre-scaling (i.e. running from PCLK16M)		15	30	µA
$I_{TIMER,LOWPOWER}$	Timer run current in low power counter mode	..	..	..	µA
$t_{TIMER,START}$	Time from START task is given until timer starts counting		0.25		µs
$t_{TIMER,COUNT,RESPONSE}$	Response time for the COUNT task in low power counter mode, see *MODE* on page 233 register.	..	..	..	µs

23 Real time counter (RTC)

The Real time counter (RTC) module provides a generic, low power timer on the low-frequency clock source (LFCLK).

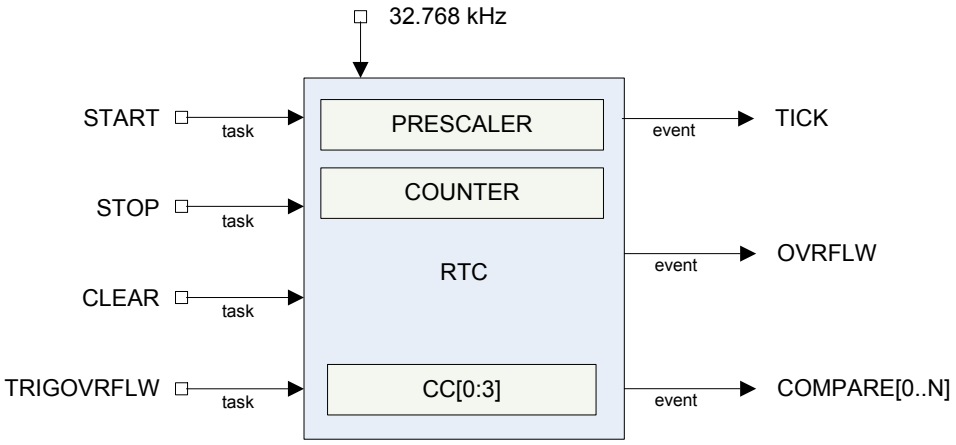

Figure 39: RTC block schematic

The RTC module features a 24-bit COUNTER, a 12-bit (1/X) prescaler, capture/compare registers, and a tick event generator for low power, tickless RTOS implementation.

23.1 Clock source

The RTC will run off the LFCLK.

The COUNTER resolution will therefore be 30.517 µs. Depending on the source, the RTC is able to run while the HFCLK is OFF and PCLK16M is not available.

See *Clock management (CLOCK)* on page 101 for more information about clock sources.

23.2 Resolution versus overflow and the PRESCALER

Counter increment frequency:

$$f_{RTC}\ [kHz] = 32.768\ /\ (PRESCALER + 1\ )$$

The PRESCALER register is read/write when the RTC is stopped. The PRESCALER register is read-only once the RTC is STARTed. Writing to the PRESCALER register when the RTC is started has no effect.

The PRESCALER is restarted on START, CLEAR and TRIGOVRFLW, that is, the prescaler value is latched to an internal register (<<PRESC>>) on these tasks.

Examples:

1. Desired COUNTER frequency 100 Hz (10 ms counter period)

   PRESCALER = round(32.768 kHz / 100 Hz) - 1 = 327

   f_{RTC} = 99.9 Hz

   10009.576 µs counter period
2. Desired COUNTER frequency 8 Hz (125 ms counter period)

PRESCALER = round (32.768 kHz / 8 Hz) – 1 = 4095

f_{RTC} = 8 Hz

125 ms counter period

Table 38: RTC resolution versus overflow

Prescaler	Counter resolution	Overflow
0	30.517 µs	512 seconds
2^8-1	7812.5 µs	131072 seconds
2^{12}-1	125 ms	582.542 hours

23.3 COUNTER register

The COUNTER increments on LFCLK when the internal PRESCALER register (<<PRESC>>) is 0x00. <<PRESC>> is reloaded from the PRESCALER register. If enabled, the TICK event occurs on each increment of the COUNTER. The TICK event is disabled by default.

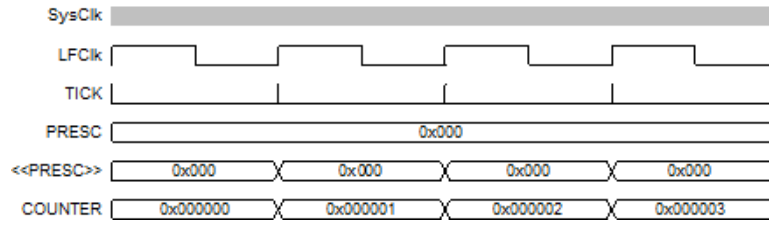

Figure 40: Timing diagram - COUNTER_PRESCALER_0

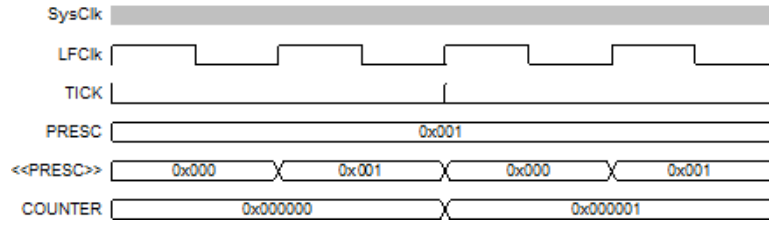

Figure 41: Timing diagram - COUNTER_PRESCALER_1

23.4 Overflow features

The TRIGOVRFLW task sets the COUNTER value to 0xFFFFF0 to allow SW test of the overflow condition.

OVRFLW occurs when COUNTER overflows from 0xFFFFFF to 0x000000.

Important: The OVRFLW event is disabled by default.

23.5 TICK event

The TICK event enables low power "tick-less" RTOS implementation as it optionally provides a regular interrupt source for a RTOS without the need to use the ARM® SysTick feature.

Using the RTC TICK event rather than the SysTick allows the CPU to be powered down while still keeping RTOS scheduling active.

Important: The TICK event is disabled by default.

23.6 Event control feature

To optimize RTC power consumption, events in the RTC can be individually disabled to prevent PCLK16M and HFCLK being requested when those events are triggered. This is managed using the EVTEN register.

For example, if the TICK event is not required for an application, this event should be disabled as it is frequently occurring and may increase power consumption if HFCLK otherwise could be powered down for long durations.

This means that the RTC implements a slightly different task and event system compared to the standard system described in *Figure 7: Tasks, events, shortcuts, and interrupts* on page 74. The RTC task and event system is illustrated in *Figure 42: Tasks, events and interrupts in the RTC* on page 238.

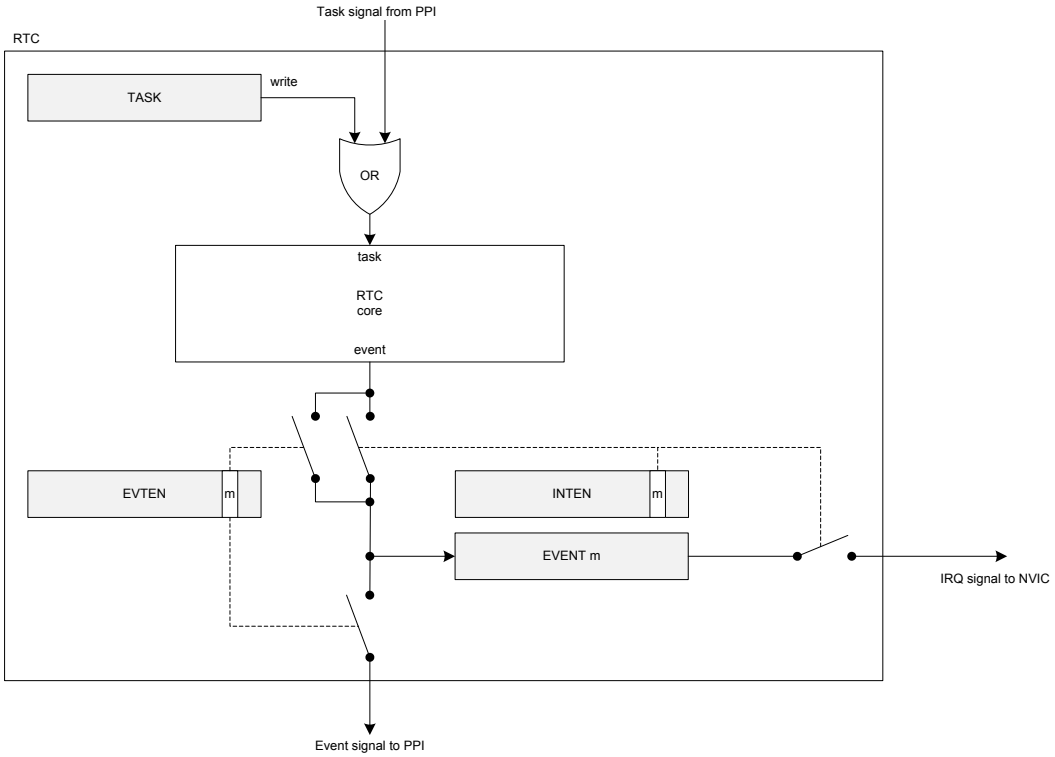

Figure 42: Tasks, events and interrupts in the RTC

23.7 Compare feature

There are a number of Compare registers.

For more information, see Table *Instances*.

When setting a compare register, the following behavior of the RTC compare event should be noted:

- If a CC register value is 0 when a CLEAR task is set, this will not trigger a COMPARE event.

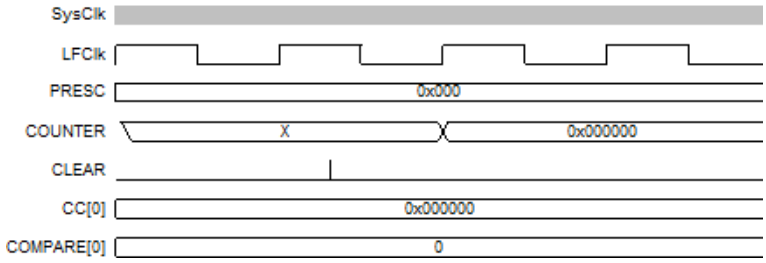

Figure 43: Timing diagram - COMPARE_CLEAR

- If a CC register is N and the COUNTER value is N when the START task is set, this will not trigger a COMPARE event.

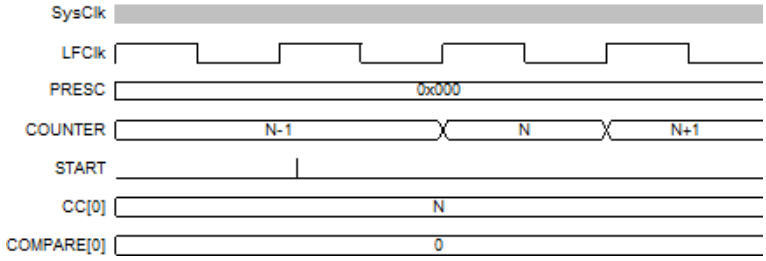

Figure 44: Timing diagram - COMPARE_START

- COMPARE occurs when a CC register is N and the COUNTER value transitions from N-1 to N.

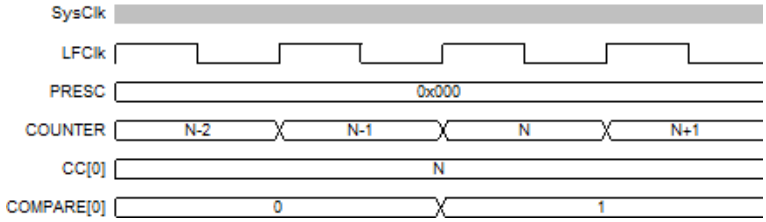

Figure 45: Timing diagram - COMPARE

- If the COUNTER is N, writing N+2 to a CC register is guaranteed to trigger a COMPARE event at N+2.

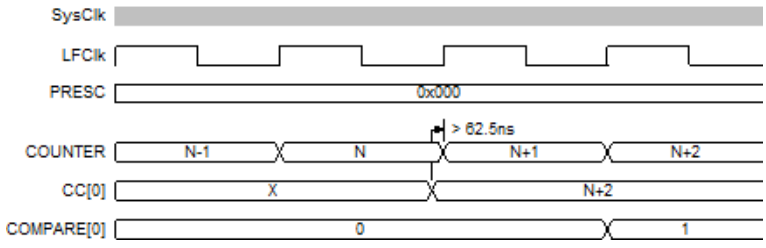

Figure 46: Timing diagram - COMPARE_N+2

- If the COUNTER is N, writing N or N+1 to a CC register may not trigger a COMPARE event.

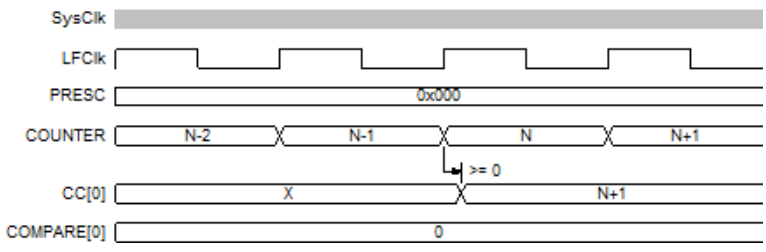

Figure 47: Timing diagram - COMPARE_N+1

- If the COUNTER is N and the current CC register value is N+1 or N+2 when a new CC value is written, a match may trigger on the previous CC value before the new value takes effect. If the current CC value greater than N+2 when the new value is written, there will be no event due to the old value.

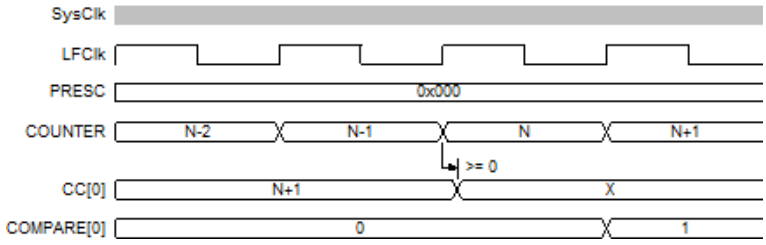

Figure 48: Timing diagram - COMPARE_N-1

23.8 TASK and EVENT jitter/delay

Jitter or delay in the RTC is due to the peripheral clock being a low frequency clock (LFCLK) which is not synchronous to the faster PCLK16M.

Registers in the peripheral interface, part of the PCLK16M domain, have a set of mirrored registers in the LFCLK domain. For example, the COUNTER value accessible from the CPU is in the PCLK16M domain and is latched on read from an internal register called COUNTER in the LFCLK domain. COUNTER is the register which is actually modified each time the RTC ticks. These registers must be synchronised between clock domains (PCLK16M and LFCLK).

The following is a summary of the jitter introduced on tasks and events. Figures illustrating jitter follow.

Table 39: RTC jitter magnitudes on tasks

Task	Delay
CLEAR, STOP, START, TRIGOVRFLOW	+15 to 46 µs

Table 40: RTC jitter magnitudes on events

Operation/Function	Jitter
START to COUNTER increment	+/- 15 µs
COMPARE to COMPARE [20]	+/- 62.5 ns

1. CLEAR and STOP (and TRIGOVRFLW; not shown) will be delayed as long as it takes for the peripheral to clock a falling edge and rising of the LFCLK. This is between 15.2585 µs and 45.7755 µs – rounded to 15 µs and 46 µs for the remainder of the section.

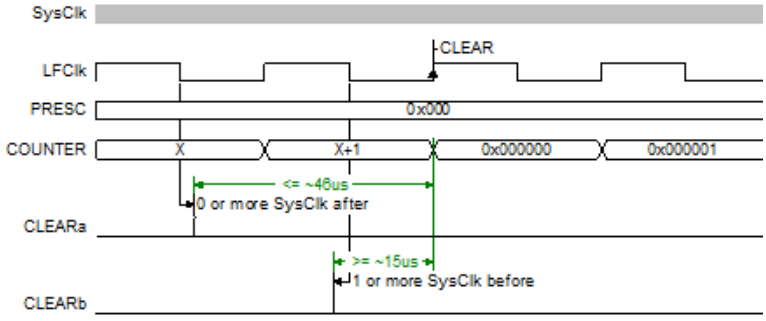

Figure 49: Timing diagram - DELAY_CLEAR

[20] Assumes RTC runs continuously between these events.

Note: 32.768 kHz clock jitter is additional to the numbers provided above.

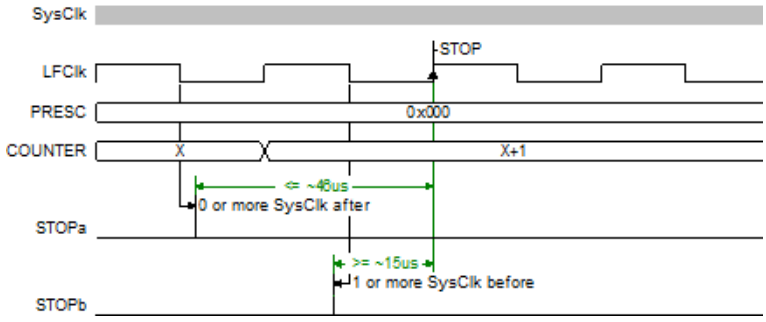

Figure 50: Timing diagram - DELAY_STOP

2. The START task will start the RTC. The first increment of COUNTER (and instance of TICK event) will be after 30.5 µs +/-15 µs, again because at least 1 falling edge must occur after the START TASK before the rising edge causes events and COUNTER increment. The figures show the smallest and largest delays to on the START task which appears as a +/-15 µs jitter on the first COUNTER increment.

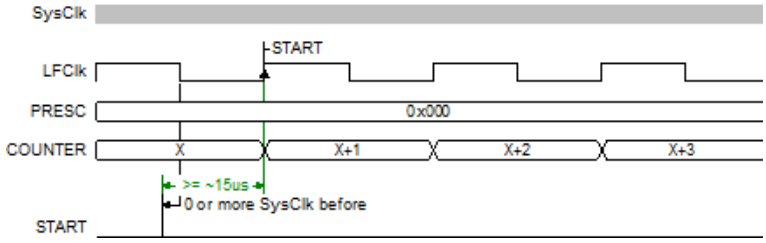

Figure 51: Timing diagram - JITTER_START-

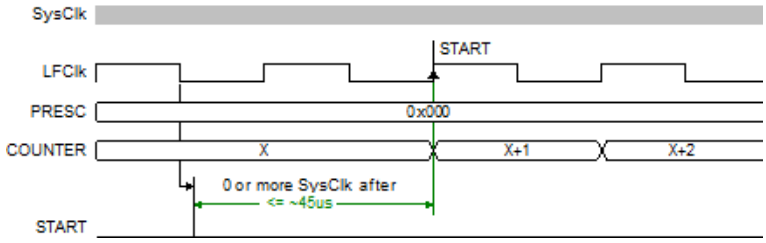

Figure 52: Timing diagram - JITTER_START+

23.9 Reading the COUNTER register

To read the COUNTER register, the internal <<COUNTER>> value is sampled.

To ensure that the <<COUNTER>> is safely sampled (considering an LFCLK transition may occur during a read), the CPU and core memory bus are halted for three cycles by lowering the core PREADY signal. The Read takes the CPU 2 cycles in addition resulting in the COUNTER register read taking a fixed five PCLK16M clock cycles.

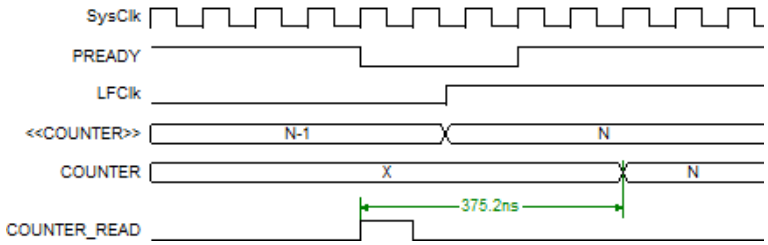

Figure 53: Timing diagram - COUNTER_READ

23.10 Registers

Table 41: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000B000	RTC	RTC0	Real time counter 0	CC[0..2] implemented, CC[3] not implemented
0x40011000	RTC	RTC1	Real time counter 1	CC[0..3] implemented
0x40024000	RTC	RTC2	Real time counter 2.	CC[0..3] implemented

Table 42: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start RTC COUNTER
TASKS_STOP	0x004	Stop RTC COUNTER
TASKS_CLEAR	0x008	Clear RTC COUNTER
TASKS_TRIGOVRFLW	0x00C	Set COUNTER to 0xFFFFF0
EVENTS_TICK	0x100	Event on COUNTER increment
EVENTS_OVRFLW	0x104	Event on COUNTER overflow
EVENTS_COMPARE[0]	0x140	Compare event on CC[0] match
EVENTS_COMPARE[1]	0x144	Compare event on CC[1] match
EVENTS_COMPARE[2]	0x148	Compare event on CC[2] match
EVENTS_COMPARE[3]	0x14C	Compare event on CC[3] match
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
EVTEN	0x340	Enable or disable event routing
EVTENSET	0x344	Enable event routing
EVTENCLR	0x348	Disable event routing
COUNTER	0x504	Current COUNTER value
PRESCALER	0x508	12 bit prescaler for COUNTER frequency (32768/(PRESCALER+1)).Must be written when RTC is stopped
CC[0]	0x540	Compare register 0
CC[1]	0x544	Compare register 1
CC[2]	0x548	Compare register 2
CC[3]	0x54C	Compare register 3

23.10.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit number																															
Id																F	E	D	C											B	A
Reset 0x00000000																**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**		**Value Id**		**Value**		**Description**																							
A	RW	TICK						Write '1' to Enable interrupt on *EVENTS_TICK* event																							
				Set		1		Enable																							

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																F	E	D	C																B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Disabled	0																															
			Enabled	1																															
B	RW	OVRFLW																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	COMPARE0																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
D	RW	COMPARE1																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
E	RW	COMPARE2																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
F	RW	COMPARE3																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															

23.10.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																F	E	D	C																B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	TICK																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	OVRFLW																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	COMPARE0																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
D	RW	COMPARE1																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
E	RW	COMPARE2																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
F	RW	COMPARE3																																	
			Clear	1																															
			Disabled	0																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																F	E	D	C																B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Enabled	1																															

23.10.3 EVTEN

Address offset: 0x340

Enable or disable event routing

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																F	E	D	C																B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	TICK																																	
			Disabled	0																															
			Enabled	1																															
B	RW	OVRFLW																																	
			Disabled	0																															
			Enabled	1																															
C	RW	COMPARE0																																	
			Disabled	0																															
			Enabled	1																															
D	RW	COMPARE1																																	
			Disabled	0																															
			Enabled	1																															
E	RW	COMPARE2																																	
			Disabled	0																															
			Enabled	1																															
F	RW	COMPARE3																																	
			Disabled	0																															
			Enabled	1																															

23.10.4 EVTENSET

Address offset: 0x344

Enable event routing

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																F	E	D	C																B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	TICK																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	OVRFLW																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	COMPARE0																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
D	RW	COMPARE1																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																F	E	D	C																B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
E	RW	COMPARE2																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
F	RW	COMPARE3																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															

23.10.5 EVTENCLR

Address offset: 0x348

Disable event routing

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																F	E	D	C																B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	TICK																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	OVRFLW																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	COMPARE0																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
D	RW	COMPARE1																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
E	RW	COMPARE2																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
F	RW	COMPARE3																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															

23.10.6 COUNTER

Address offset: 0x504

Current COUNTER value

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id									A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	R	COUNTER			Counter value

23.10.7 PRESCALER

Address offset: 0x508

12 bit prescaler for COUNTER frequency (32768/(PRESCALER+1)).Must be written when RTC is stopped

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																					A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	PRESCALER			Prescaler value

23.10.8 CC[0]

Address offset: 0x540

Compare register 0

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id									A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	COMPARE			Compare value

23.10.9 CC[1]

Address offset: 0x544

Compare register 1

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id									A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	COMPARE			Compare value

23.10.10 CC[2]

Address offset: 0x548

Compare register 2

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id									A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	COMPARE			Compare value

23.10.11 CC[3]

Address offset: 0x54C

Compare register 3

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id									A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	COMPARE			Compare value

23.11 Electrical Specification

23.11.1 RTC Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
I_{RTC}	Run current Real Time Counter (LFCLK source)		0.1		µA

24 Random number generator (RNG)

The Random number generator (RNG) generates true non-deterministic random numbers based on internal thermal noise that are suitable for cryptographic purposes. The RNG does not require a seed value.

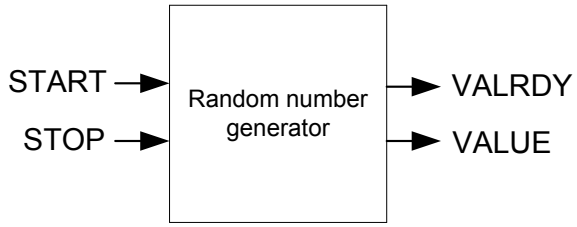

Figure 54: Random number generator

The RNG is started by triggering the START task and stopped by triggering the STOP task. When started, new random numbers are generated continuously and written to the VALUE register when ready. A VALRDY event is generated for every new random number that is written to the VALUE register. This means that after a VALRDY event is generated the CPU has the time until the next VALRDY event to read out the random number from the VALUE register before it is overwritten by a new random number.

24.1 Bias correction

A bias correction algorithm is employed on the internal bit stream to remove any bias toward '1' or '0'. The bits are then queued into an eight-bit register for parallel readout from the VALUE register.

It is possible to enable bias correction in the CONFIG register. This will result in slower value generation, but will ensure a statistically uniform distribution of the random values.

24.2 Speed

The time needed to generate one random byte of data is unpredictable, and may vary from one byte to the next. This is especially true when bias correction is enabled.

24.3 Registers

Table 43: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000D000	RNG	RNG	Random Number Generator	

Table 44: Register Overview

Register	Offset	Description
TASKS_START	0x000	Task starting the random number generator
TASKS_STOP	0x004	Task stopping the random number generator
EVENTS_VALRDY	0x100	Event being generated for every new random number written to the VALUE register
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
CONFIG	0x504	Configuration register
VALUE	0x508	Output random number

24.3.1 SHORTS

Address offset: 0x200

Shortcut register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															**Description**
A	RW	VALRDY_STOP																																	Shortcut between *EVENTS_VALRDY* event and *TASKS_STOP* task
			Disabled	0																															Disable shortcut
			Enabled	1																															Enable shortcut

24.3.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															**Description**
A	RW	VALRDY																																	Write '1' to Enable interrupt on *EVENTS_VALRDY* event
			Set	1																															Enable
			Disabled	0																															Read: Disabled
			Enabled	1																															Read: Enabled

24.3.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															**Description**
A	RW	VALRDY																																	Write '1' to Disable interrupt on *EVENTS_VALRDY* event
			Clear	1																															Disable
			Disabled	0																															Read: Disabled
			Enabled	1																															Read: Enabled

24.3.4 CONFIG

Address offset: 0x504

Configuration register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															**Description**
A	RW	DERCEN																																	Bias correction
			Disabled	0																															Disabled
			Enabled	1																															Enabled

24.3.5 VALUE

Address offset: 0x508

Output random number

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																									A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	R	VALUE		[0..255]	Generated random number

24.4 Electrical Specification

24.4.1 RNG Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
I_{RNG}	Run current.		310		µA
$t_{RNG,START}$	Time from setting the START task to generation begins. This is a one-time delay on START signal and does not apply between samples.		128		µs
$t_{RNG,RAW}$	Run time per byte without bias correction. Uniform distribution of 0 and 1 is not guaranteed.		29		µs
$t_{RNG,BC}$	Run time per byte with bias correction. Uniform distribution of 0 and 1 is guaranteed. Time to generate a byte cannot be guaranteed.		114		µs

25 Temperature sensor (TEMP)

The temperature sensor measures die temperature over the temperature range of the device. Linearity compensation can be implemented if required by the application.

Listed here are the main features for TEMP:

- Temperature range is greater than or equal to operating temperature of the device
- Resolution is 0.25 degrees

TEMP is started by triggering the START task.

When the temperature measurement is completed, a DATARDY event will be generated and the result of the measurement can be read from the TEMP register.

To achieve the measurement accuracy stated in the electrical specification, the crystal oscillator must be selected as the HFCLK source, see *Clock management (CLOCK)* on page 101 for more information.

When the temperature measurement is completed, TEMP analog electronics power down to save power.

TEMP only supports one-shot operation, meaning that every TEMP measurement has to be explicitly started using the START task.

25.1 Registers

Table 45: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000C000	TEMP	TEMP	Temperature Sensor	

Table 46: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start temperature measurement
TASKS_STOP	0x004	Stop temperature measurement
EVENTS_DATARDY	0x100	Temperature measurement complete, data ready
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
TEMP	0x508	Temperature in °C

25.1.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																														
A	RW	DATARDY			Write '1' to Enable interrupt on *EVENTS_DATARDY* event																														
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														

25.1.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	DATARDY																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															

25.1.3 TEMP

Address offset: 0x508

Temperature in °C

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	TEMP																																	

Temperature in °C

Result of temperature measurement. Die temperature in °C, 2's complement format, 0.25 °C

Decision point: DATARDY

25.2 Electrical Specification

25.2.1 Temperature Sensor Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
I_{TEMP}	Run current for Temperature sensor			300	µA
t_{TEMP}	Time required for temperature measurement		35		µs
$T_{TEMP,RANGE}$	Temperature sensor range	-40		85	°C
$T_{TEMP,ACC}$	Temperature sensor accuracy	-4		4	°C
$T_{TEMP,RES}$	Temperature sensor resolution		0.25		°C
$T_{TEMP,STB}$	Sample to sample stability at constant device temperature		+/-0.25		°C
$T_{TEMP,DIFF}$	Measurement will vary when switching between PLL locked XOSC and RNOSC system clock sources			?	°C
$T_{TEMP,OFFST}$	Sample offset at 25°C			+/-2	°C

26 AES electronic codebook mode encryption (ECB)

The AES electronic codebook mode encryption (ECB) can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption. The ECB encryption block supports 128 bit AES encryption (encryption only, not decryption).

AES ECB operates with EasyDMA access to system Data RAM for in-place operations on cleartext and ciphertext during encryption. ECB uses the same AES core as the CCM and AAR blocks and is an asynchronous operation which may not complete if the AES core is busy.

AES ECB features:

- 128 bit AES encryption
- Supports standard AES ECB block encryption
- Memory pointer support
- DMA data transfer

AES ECB performs a 128 bit AES block encrypt. At the STARTECB task, data and key is loaded into the algorithm by EasyDMA. When output data has been written back to memory, the ENDECB event is triggered.

AES ECB can be stopped by triggering the STOPECB task.

26.1 EasyDMA

The ECB implements an EasyDMA mechanism for reading and writing to the Data RAM. This DMA cannot access the program memory or any other parts of the memory area except RAM.

If the ECBDATAPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 34 for more information about the different memory regions.

The EasyDMA will have finished accessing the Data RAM when the ENDECB or ERRORECB is generated.

26.2 ECB data structure

Input to the block encrypt and output from the block encrypt are stored in the same data structure. ECBDATAPTR should point to this data structure before STARTECB is initiated.

Table 47: ECB data structure overview

Property	Address offset	Description
KEY	0	16 byte AES key
CLEARTEXT	16	16 byte AES cleartext input block
CIPHERTEXT	32	16 byte AES ciphertext output block

26.3 Shared resources

The ECB, CCM, and AAR share the same AES module. The ECB will always have lowest priority and if there is a sharing conflict during encryption, the ECB operation will be aborted and an ERRORECB event will be generated.

26.4 Registers

Table 48: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000E000	ECB	ECB	AES ECB Mode Encryption	

Table 49: Register Overview

Register	Offset	Description
TASKS_STARTECB	0x000	Start ECB block encrypt
TASKS_STOPECB	0x004	Abort a possible executing ECB operation
EVENTS_ENDECB	0x100	ECB block encrypt complete
EVENTS_ERRORECB	0x104	ECB block encrypt aborted because of a STOPECB task or due to an error
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ECBDATAPTR	0x504	ECB block encrypt memory pointers

26.4.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	ENDECB			Write '1' to Enable interrupt on *EVENTS_ENDECB* event
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
B	RW	ERRORECB			Write '1' to Enable interrupt on *EVENTS_ERRORECB* event
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

26.4.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	ENDECB			Write '1' to Disable interrupt on *EVENTS_ENDECB* event
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
B	RW	ERRORECB			Write '1' to Disable interrupt on *EVENTS_ERRORECB* event
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

26.4.3 ECBDATAPTR

Address offset: 0x504

ECB block encrypt memory pointers

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	ECBDATAPTR			Pointer to the ECB data structure (see Table 1 ECB data structure overview)

26.5 Electrical Specification

26.5.1 ECB Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
I_{ECB}	Run current for Crypto in all modes				µA
t_{ECB}	Run time per 16 byte block in all modes		6		µs

27 AES CCM mode encryption (CCM)

Cipher block chaining - message authentication code (CCM) mode is an authenticated encryption algorithm designed to provide both authentication and confidentiality during data transfer. CCM combines counter mode encryption and CBC-MAC authentication. The CCM terminology "Message authentication code (MAC)" is called the "Message integrity check (MIC)" in '*Bluetooth* terminology and also in this document.

The CCM block generates an encrypted keystream that is applied to input data using the XOR operation and generates the 4 byte MIC field in one operation. The CCM and radio can be configured to work synchronously. The CCM will encrypt in time for transmission and decrypt after receiving bytes into memory from the Radio. All operations can complete within the packet RX or TX time. CCM on this device is implemented according to *Bluetooth* requirements and the algorithm as defined in IETF RFC3610, see *http://www.ietf.org/rfc/rfc3610.txt*, and depends on the AES-128 block cipher. A description of the CCM algorithm can also be found in the NIST Special Publication 800-38C (*http://csrc.nist.gov/publications/PubsSPs.html*) The *Bluetooth* specification describes the configuration of counter mode blocks and encryption blocks to implement compliant encryption for BLE.

The CCM block uses EasyDMA to load key, counter mode blocks (including the nonce required), and to read/write plain text and cipher text.

The AES CCM supports three operations: key-stream generation, packet encryption, and packet decryption. All these operations are done in compliance with the *Bluetooth* specification.[21] A new key-stream must be generated before a new packet encryption or packet decryption operation can be started.

A key-stream is generated by triggering the KSGEN task. An ENDKSGEN event will be generated when the new key-stream has been generated. The key-stream will be stored in the AES CCM's temporary memory area, specified by the SCRATCHPTR, where it will be used in subsequent encryption and decryption operations.

Encryption is started by triggering the CRYPT task with the MODE register set to ENCRYPTION. Similarly, decryption is started by triggering the same task with MODE set to DECRYPTION. An ENDCRYPT event will be generated when packet encryption is completed as well as when packet decryption is completed, see *Figure 55: Key-stream generation followed by encryption or decryption. The shortcut is optional.* on page 256.

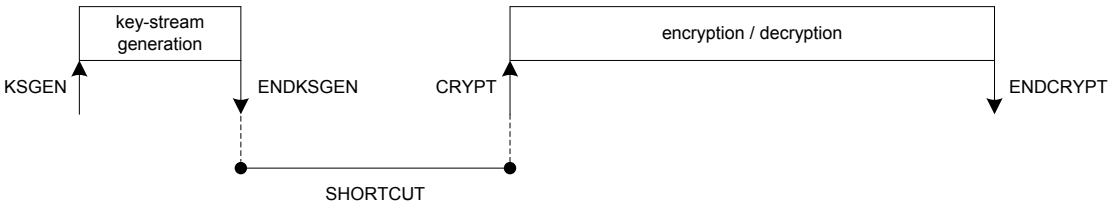

Figure 55: Key-stream generation followed by encryption or decryption. The shortcut is optional.

Key-stream generation, packet encryption, and packet decryption operations utilize the configuration specified in the data structure pointed to by the CNFPTR pointer. It is necessary to configure this pointer and its underlying data structure, and the MODE register before the KSGEN task is triggered. It is also necessary to configure the INPTR pointer and the OUTPTR pointer before the CRYPT task is triggered.

If a shortcut is used between ENDKSGEN event and CRYPT task, the INPTR pointer and the OUTPTR pointer must be configured before the KSGEN task is triggered.

The AES CCM supports different packet lengths, this is configured via the PACKETLENGTH field in the MODE register.

[21] *Bluetooth* AES CCM 128 bit block encryption, see *Bluetooth* Core specification Version 4.0.

27.1 Encryption

During packet encryption the AES CCM will read the unencrypted packet located in RAM at the address specified in the INPTR pointer, encrypt the packet and append a four byte long Message Integrity Check (MIC) field to the packet.

The AES CCM will also modify the length field of the packet to adjust for the appended MIC field, that is, add four bytes to the length, and store the resulting packet back into RAM at the address specified in the OUTPTR pointer, see *Figure 56: Encryption* on page 257.

Empty packets (length field is set to 0) will not be encrypted but instead moved unmodified through the AES CCM.

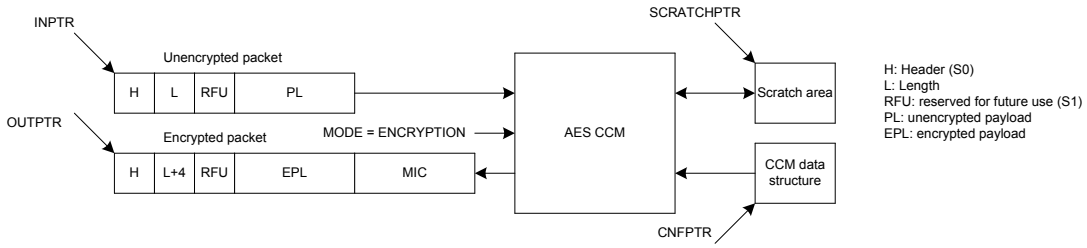

Figure 56: Encryption

27.2 Decryption

During packet decryption the AES CCM will read the encrypted packet located in RAM at the address specified in the INPTR pointer, decrypt the packet, authenticate the packet's MIC field and generate the appropriate MIC status.

The AES CCM will also modify the length field of the packet to adjust for the MIC field, that is, subtract four bytes from the length, and then store the decrypted packet into RAM at the address pointed to by the OUTPTR pointer, see *Figure 57: Decryption* on page 257.

The CCM is only able to decrypt packets that are at least 5 bytes long, that is, 1 byte or more encrypted payload (EPL) and 4 bytes of MIC. The CCM will therefore generate a MIC error for packets where the length field is set to 1, 2, 3 or 4.

Empty packets (length field is set to 0) will not be decrypted but instead moved unmodified through the AES CCM, these packets will always pass the MIC check.

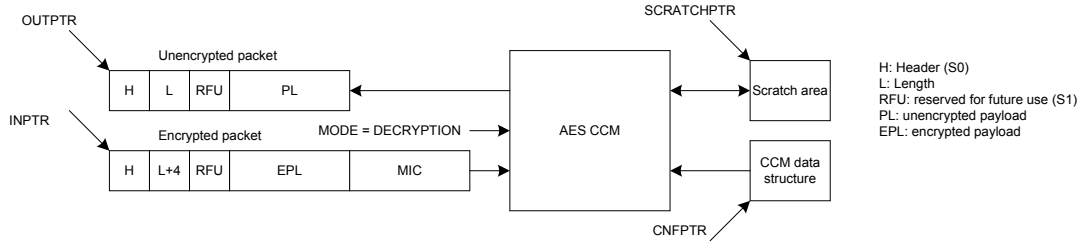

Figure 57: Decryption

27.3 AES CCM and RADIO concurrent operation

The AES CCM is designed to run in parallel with the RADIO to enable on-the-fly encryption and decryption of RADIO packets without CPU involvement. To facilitate this, the RADIO has to be configured with specific settings.

Table 50: Radio configuration settings

Radio parameter	Value	Description
PCNF0.S0LEN	1	Length of HEADER field in: *Table 52: Data structure for unencrypted packet* on page 260 and *Table 53: Data structure for encrypted packet* on page 260.
PCNF0.LFLEN	5 or 8	Length of LENGTH field in: *Table 52: Data structure for unencrypted packet* on page 260 and *Table 53: Data structure for encrypted packet* on page 260.
PCNF0.S1LEN	3 or 0	Length of the RFU field in: *Table 52: Data structure for unencrypted packet* on page 260 and *Table 53: Data structure for encrypted packet* on page 260. The combined length of LENGTH and RFU must always be 8 bit.
PCNF0.S1	Include	Always include the S1 field (RFU field) in RAM to secure that the same data structure can be used for PCNF0.S1LEN = 3 and PCNF0.S1LEN = 0: *Table 52: Data structure for unencrypted packet* on page 260 and *Table 53: Data structure for encrypted packet* on page 260.
MODE	Ble_1Mbit	Data rate. Must match CCM->MODE.DATARATE
PCNF1.BALEN	3	Length of address (32 bit)
CRCCNF.LEN	3	Length of CRC (24 bit)

27.4 Encrypting packets on-the-fly in radio transmit mode

When the AES CCM is encrypting a packet on-the-fly at the same time as the RADIO is transmitting it, the RADIO must read the encrypted packet from the same memory location as the AES CCM is writing to.

The OUTPTR pointer in the AES CCM must therefore point to the same memory location as the PACKETPTR pointer in the RADIO, see *Figure 58: Configuration of on-the-fly encryption* on page 258.

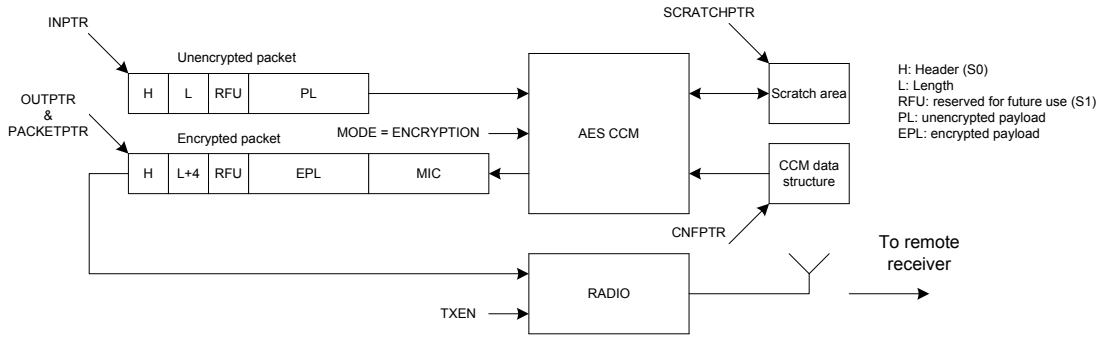

Figure 58: Configuration of on-the-fly encryption

In order to match the RADIO's timing, the KSGEN task must be triggered no later than when the START task in the RADIO is triggered, in addition the shortcut between the ENDKSGEN event and the CRYPT task must be enabled. This use-case is illustrated in *Figure 59: On-the-fly encryption using a PPI connection* on page 258 using a PPI connection between the READY event in the RADIO and the KSGEN task in the AES CCM.

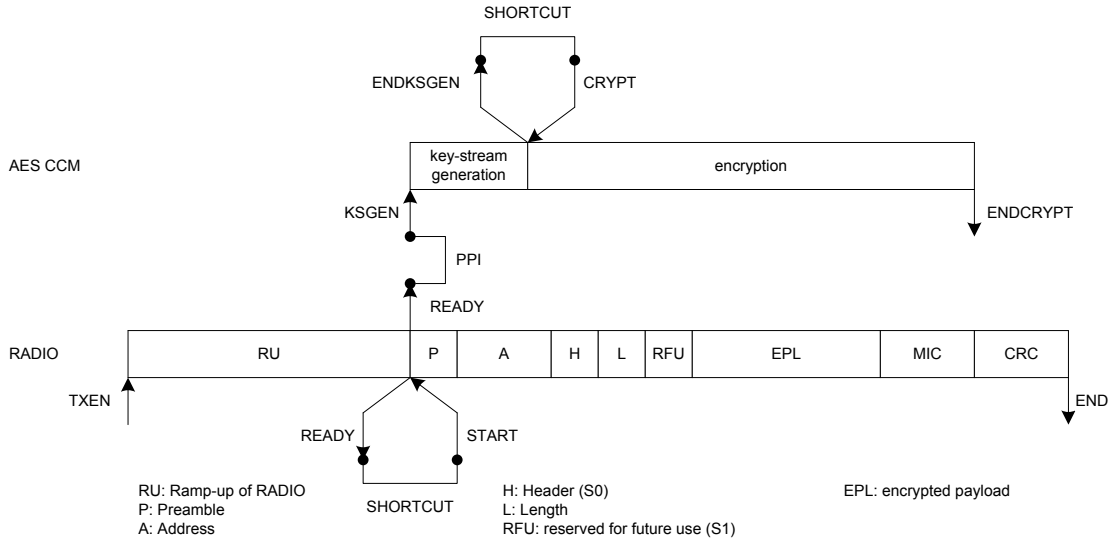

Figure 59: On-the-fly encryption using a PPI connection

27.5 Decrypting packets on-the-fly in radio receive mode

When the AES CCM is decrypting a packet on-the-fly at the same time as the RADIO is receiving it, the AES CCM must read the encrypted packet from the same memory location as the RADIO is writing to.

The INPTR pointer in the AES CCM must therefore point to the same memory location as the PACKETPTR pointer in the RADIO, see *Figure 60: Configuration of on-the-fly decryption* on page 259.

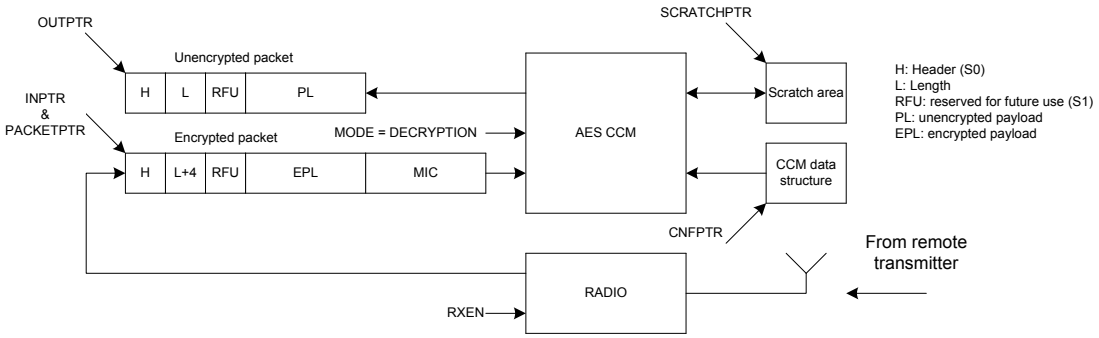

Figure 60: Configuration of on-the-fly decryption

In order to match the RADIO's timing, the KSGEN task must be triggered no later than when the START task in the RADIO is triggered. In addition, the CRYPT task must be triggered no earlier than when the ADDRESS event is generated by the RADIO.

If the CRYPT task is triggered exactly at the same time as the ADDRESS event is generated by the RADIO, the AES CCM will guarantee that the decryption is completed no later than when the END event in the RADIO is generated.

This use-case is illustrated in *Figure 61: On-the-fly decryption using a PPI connection between the READY event in the RADIO and the KSGEN task in the AES CCM* on page 259 using a PPI connection between the ADDRESS event in the RADIO and the CRYPT task in the AES CCM. The KSGEN task is triggered from the READY event in the RADIO through a PPI connection.

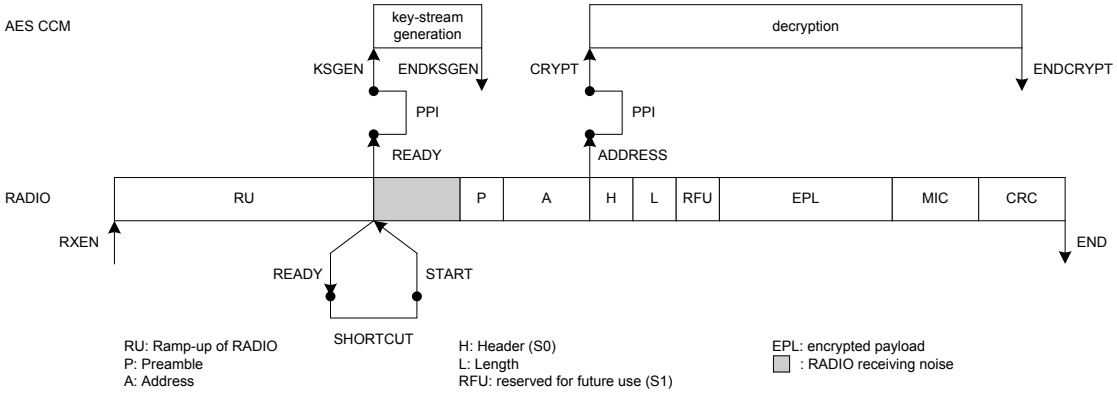

Figure 61: On-the-fly decryption using a PPI connection between the READY event in the RADIO and the KSGEN task in the AES CCM

27.6 CCM data structure

The CCM data structure is located in Data RAM at the memory location specified by the CNFPTR pointer register.

Table 51: CCM data structure overview

Property	Address offset	Description
KEY	0	16 byte AES key

Property	Address offset	Description
PKTCTR	16	Octet0 (LSO) of packet counter
	17	Octet1 of packet counter
	18	Octet2 of packet counter
	19	Octet3 of packet counter
	20	Bit 6 – Bit 0: Octet4 (7 most significant bits of packet counter, with Bit 6 being the most significant bit) Bit7: Ignored
	21	Ignored
	22	Ignored
	23	Ignored
	24	Bit 0: Direction bit Bit 7 – Bit 1: Zero padded
IV	25	8 byte initialization vector (IV) Octet0 (LSO) of IV, Octet1 of IV, … , Octet7 (MSO) of IV

The NONCE vector (as specified by the *Bluetooth* Core Specification) will be generated by hardware based on the information specified in the CCM data structure from *Table 51: CCM data structure overview* on page 259 .

Table 52: Data structure for unencrypted packet

Property	Address offset	Description
HEADER	0	Packet Header
LENGTH	1	Number of bytes in unencrypted payload
RFU	2	Reserved Future Use
PAYLOAD	3	Unencrypted payload

Table 53: Data structure for encrypted packet

Property	Address offset	Description
HEADER	0	Packet Header
LENGTH	1	Number of bytes in encrypted payload including length of MIC **Important:** LENGTH will be 0 for empty packets since the MIC is not added to empty packets
RFU	2	Reserved Future Use
PAYLOAD	3	Encrypted payload
MIC	3 + payload length	ENCRYPT: 4 bytes encrypted MIC **Important:** MIC is not added to empty packets

27.7 EasyDMA and ERROR event

The CCM implements an EasyDMA mechanism for reading and writing to the RAM.

In some scenarios where the CPU and other DMA enabled peripherals are accessing the RAM at the same time, the CCM DMA could experience some bus conflicts which may also result in an error during encryption. If this happens, the ERROR event will be generated.

The EasyDMA will have finished accessing the RAM when the ENDKSGEN and ENDCRYPT events are generated.

If the CNFPTR, SCRATCHPTR, INPTR and the OUTPTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 34 for more information about the different memory regions.

27.8 Shared resources

The CCM shares registers and other resources with other peripherals that have the same ID as the CCM. The user must therefore disable all peripherals that have the same ID as the CCM before the CCM can be configured and used.

Disabling a peripheral that have the same ID as the CCM will not reset any of the registers that are shared with the CCM. It is therefore important to configure all relevant CCM registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 36 for details on peripherals and their IDs.

27.9 Registers

Table 54: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000F000	CCM	CCM	AES CCM Mode Encryption	

Table 55: Register Overview

Register	Offset	Description
TASKS_KSGEN	0x000	Start generation of key-stream. This operation will stop by itself when completed.
TASKS_CRYPT	0x004	Start encryption/decryption. This operation will stop by itself when completed.
TASKS_STOP	0x008	Stop encryption/decryption
EVENTS_ENDKSGEN	0x100	Key-stream generation complete
EVENTS_ENDCRYPT	0x104	Encrypt/decrypt complete
EVENTS_ERROR	0x108	CCM error event
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
MICSTATUS	0x400	MIC check result
ENABLE	0x500	Enable
MODE	0x504	Operation mode
CNFPTR	0x508	Pointer to data structure holding AES key and NONCE vector
INPTR	0x50C	Input pointer
OUTPTR	0x510	Output pointer
SCRATCHPTR	0x514	Pointer to data area used for temporary storage

27.9.1 SHORTS

Address offset: 0x200

Shortcut register

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	ENDKSGEN_CRYPT			Shortcut between *EVENTS_ENDKSGEN* event and *TASKS_CRYPT* task
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut

27.9.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	ENDKSGEN			Write '1' to Enable interrupt on *EVENTS_ENDKSGEN* event
			Set	1	Enable
			Disabled	0	Read: Disabled

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
			Enabled	1	Read: Enabled
B	RW	ENDCRYPT			Write '1' to Enable interrupt on *EVENTS_ENDCRYPT* event
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
C	RW	ERROR			Write '1' to Enable interrupt on *EVENTS_ERROR* event
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

27.9.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	ENDKSGEN			Write '1' to Disable interrupt on *EVENTS_ENDKSGEN* event
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
B	RW	ENDCRYPT			Write '1' to Disable interrupt on *EVENTS_ENDCRYPT* event
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
C	RW	ERROR			Write '1' to Disable interrupt on *EVENTS_ERROR* event
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

27.9.4 MICSTATUS

Address offset: 0x400

MIC check result

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	R	MICSTATUS			The result of the MIC check performed during the previous decryption operation
			CheckFailed	0	MIC check failed
			CheckPassed	1	MIC check passed

27.9.5 ENABLE

Address offset: 0x500

Enable

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	ENABLE																																	
			Disabled	0																															
			Enabled	2																															

27.9.6 MODE

Address offset: 0x504

Operation mode

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id											C								B																A
Reset 0x00000001				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	MODE																																	
			Encryption	0																															
			Decryption	1																															
B	RW	DATARATE																																	
			1Mbit	0																															
			2Mbit	1																															
C	RW	LENGTH																																	
			Default	0																															
			Extended	1																															

27.9.7 CNFPTR

Address offset: 0x508

Pointer to data structure holding AES key and NONCE vector

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	CNFPTR																																	

Pointer to the data structure holding the AES key and the CCM NONCE vector (see Table 1 CCM data structure overview)

27.9.8 INPTR

Address offset: 0x50C

Input pointer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	INPTR																																	

Input pointer

27.9.9 OUTPTR

Address offset: 0x510

Output pointer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	OUTPTR																																	

Output pointer

27.9.10 SCRATCHPTR

Address offset: 0x514

Pointer to data area used for temporary storage

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	SCRATCHPTR			Pointer to a "scratch" data area used for temporary storage during key-stream generation, MIC generation and encryption/ decryption.The scratch area is used for temporary storage of data during key-stream generation and encryption. A space of 43 bytes must be reserved.

27.10 Electrical Specification

27.10.1 CCM Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
I_{CCM}	Run current for CCM				µA

28 Accelerated address resolver (AAR)

Accelerated address resolver is a cryptographic support function for implementing the "Resolvable Private Address Resolution Procedure" described in the *Bluetooth Core specification* v4.0. "Resolvable private address generation" should be achieved using ECB and is not supported by AAR.

The procedure allows two devices that share a secret key to generate and resolve a hash based on their device address. The AAR block enables real-time address resolution on incoming packets when configured as described in this chapter. This allows real-time packet filtering (whitelisting) using a list of known shared keys (Identity Resolving Keys (IRK) in *Bluetooth*).

28.1 Resolving a resolvable address

As per *Bluetooth* specification, a private resolvable address is composed of six bytes.

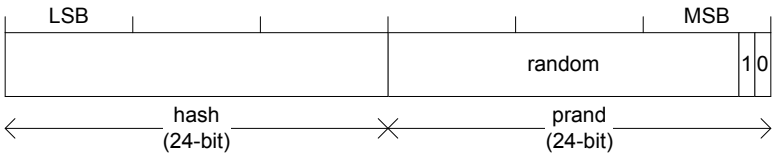

Figure 62: Resolvable address

To resolve an address the ADDRPTR register must point to the start of packet. The resolver is started by triggering the START task. A RESOLVED event is generated when the AAR manages to resolve the address using one of the Identity Resolving Keys (IRK) found in the IRK data structure. The AAR will use the IRK specified in the register IRK0 to IRK15 starting from IRK0. How many to be used is specified by the NIRK register. The AAR module will generate a NOTRESOLVED event if it is not able to resolve the address using the specified list of IRKs.

The AAR will go through the list of available IRKs in the IRK data structure and for each IRK try to resolve the address according to the Resolvable Private Address Resolution Procedure described in the *Bluetooth* Specification[22]. The time it takes to resolve an address may vary depending on where in the list the resolvable address is located. The resolution time will also be affected by RAM accesses performed by other peripherals and the CPU. See the *Electrical specifications* for more information about resolution time.

The AAR will only do a comparison of the received address to those programmed in the module. And not check what type of address it actually is.

The AAR will stop as soon as it has managed to resolve the address, or after trying to resolve the address using NIRK number of IRKs from the IRK data structure. The AAR will generate an END event after it has stopped.

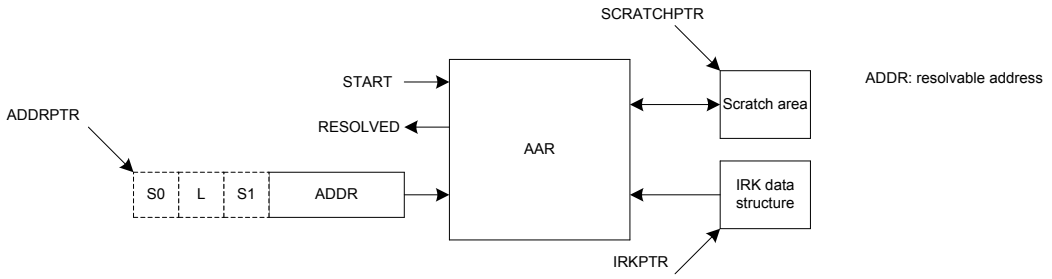

Figure 63: Address resolution with packet preloaded into RAM

[22] *Bluetooth* Specification Version 4.0 [Vol 3] chapter 10.8.2.3.

28.2 Use case example for chaining RADIO packet reception with address resolution using AAR

The AAR may be started as soon as the 6 bytes required by the AAR have been received by the RADIO and stored in RAM. The ADDRPTR pointer must point to the start of packet.

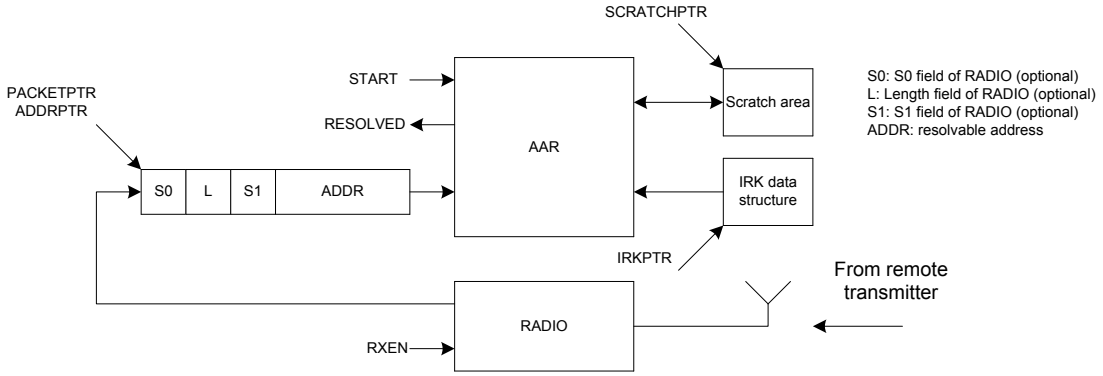

Figure 64: Address resolution with packet loaded into RAM by the RADIO

28.3 IRK data structure

The IRK data structure is located in RAM at the memory location specified by the CNFPTR pointer register.

Table 56: IRK data structure overview

Property	Address offset	Description
IRK0	0	IRK number 0 (16 - byte)
IRK1	16	IRK number 1 (16 - byte)
..	..	..
IRK15	240	IRK number 15 (16 - byte)

28.4 EasyDMA

The AAR implements EasyDMA for reading and writing to the RAM. The EasyDMA will have finished accessing the RAM when the END, RESOLVED, and NOTRESOLVED events are generated.

If the IRKPTR, ADDRPTR and the SCRATCHPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 34 for more information about the different memory regions.

28.5 Shared resources

The AAR shares registers and other resources with the peripherals that have the same ID as the AAR. The user must therefore disable all peripherals that have the same ID as the AAR before the AAR can be configured and used.

Disabling a peripheral that have the same ID as the AAR will not reset any of the registers that are shared with the AAR. It is therefore important to configure all relevant AAR registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instance table* for details on peripherals and their IDs.

28.6 Registers

Table 57: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000F000	AAR	AAR	Accelerated Address Resolver	

Table 58: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start resolving addresses based on IRKs specified in the IRK data structure
TASKS_STOP	0x008	Stop resolving addresses
EVENTS_END	0x100	Address resolution procedure complete
EVENTS_RESOLVED	0x104	Address resolved
EVENTS_NOTRESOLVED	0x108	Address not resolved
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
STATUS	0x400	Resolution status
ENABLE	0x500	Enable AAR
NIRK	0x504	Number of IRKs
IRKPTR	0x508	Pointer to IRK data structure
ADDRPTR	0x510	Pointer to the resolvable address
SCRATCHPTR	0x514	Pointer to data area used for temporary storage

28.6.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit number																																
																															C	B	A
Reset 0x00000000									**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																											
A	RW	END			Write '1' to Enable interrupt on *EVENTS_END* event																													
			Set	1	Enable																											
			Disabled	0	Read: Disabled																											
			Enabled	1	Read: Enabled																											
B	RW	RESOLVED			Write '1' to Enable interrupt on *EVENTS_RESOLVED* event																													
			Set	1	Enable																											
			Disabled	0	Read: Disabled																											
			Enabled	1	Read: Enabled																											
C	RW	NOTRESOLVED			Write '1' to Enable interrupt on *EVENTS_NOTRESOLVED* event																													
			Set	1	Enable																											
			Disabled	0	Read: Disabled																											
			Enabled	1	Read: Enabled																											

28.6.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number																																
																															C	B	A
Reset 0x00000000									**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																											
A	RW	END			Write '1' to Disable interrupt on *EVENTS_END* event																													
			Clear	1	Disable																											
			Disabled	0	Read: Disabled																											

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Enabled	1																															
B	RW	RESOLVED																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	NOTRESOLVED																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															

28.6.3 STATUS

Address offset: 0x400

Resolution status

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	STATUS		[0..15]																															

28.6.4 ENABLE

Address offset: 0x500

Enable AAR

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	ENABLE																																	
			Disabled	0																															
			Enabled	3																															

28.6.5 NIRK

Address offset: 0x504

Number of IRKs

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															A	A	A	A	A
Reset 0x00000001				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	NIRK		[1..16]																															

28.6.6 IRKPTR

Address offset: 0x508

Pointer to IRK data structure

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	IRKPTR																																	

28.6.7 ADDRPTR

Address offset: 0x510

Pointer to the resolvable address

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	ADDRPTR			Pointer to the resolvable address (6-bytes)

28.6.8 SCRATCHPTR

Address offset: 0x514

Pointer to data area used for temporary storage

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	SCRATCHPTR			Pointer to a "scratch" data area used for temporary storage during resolution.A space of minimum 3 bytes must be reserved.

28.7 Electrical Specification

28.7.1 AAR Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
I_{AAR}	Run current for AAR				µA
$t_{AAR,8}$	Time for address resolution of 8 IRKs		48		µs

29 Serial peripheral interface master (SPIM) with EasyDMA

The SPI master can communicate with multiple slaves using individual chip select signals for each of the slave devices attached to a bus.

Listed here are the main features for the SPIM

- Three SPIM instances
- SPI mode 0-3
- EasyDMA direct transfer to/from RAM for both SPI Slave and SPI Master
- Individual selection of IO pin for each SPI signal

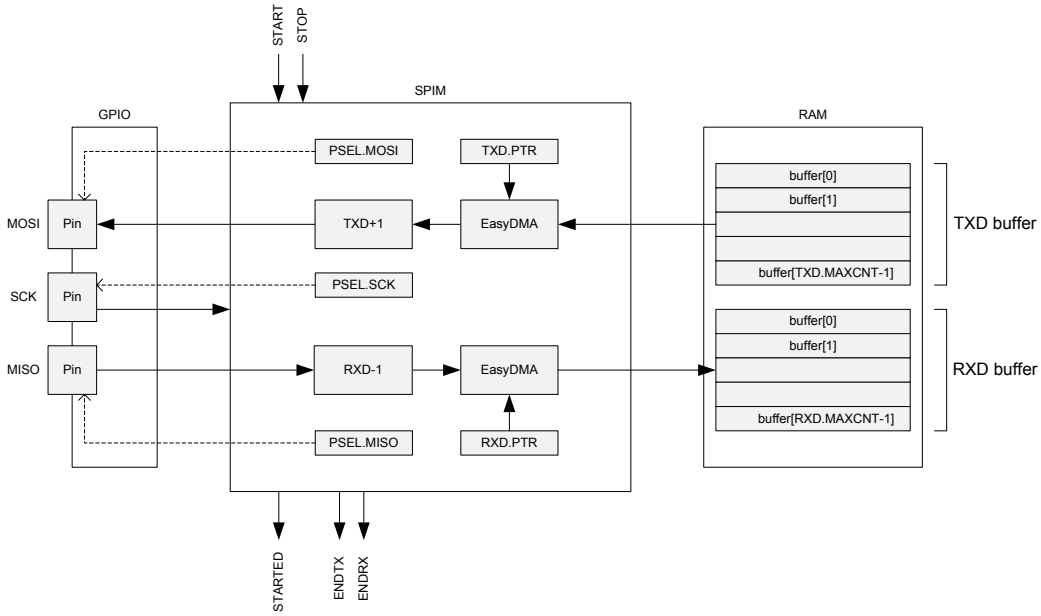

Figure 65: SPI master with EasyDMA (SPIM)

The SPIM does not implement support for chip select directly. Therefore, the CPU must use available GPIOs to select the correct slave and control this independently of the SPI master. The SPIM supports SPI modes 0 through 3. The CONFIG register allows setting CPOL and CPHA appropriately.

Table 59: SPI modes

Mode	Clock polarity CPOL	Clock phase CPHA
SPI_MODE	0 (Leading)	0 (Active High)
SPI_MODE	0 (Leading)	1 (Active Low)
SPI_MODE	1 (Trailing)	0 (Active High)
SPI_MODE	1 (Trailing)	1 (Active Low)

29.1 SPI master mode pin configuration

The different signals SCK, MOSI, and MISO associated with the SPI master are mapped to physical pins according to the configuration specified in the PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers respectively.

The PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers and their configurations are only used as long as the SPI master is enabled, and retained only as long as the device is in ON mode. PSEL.SCK, PSEL.MOSI and PSEL.MISO must only be configured when the SPI master is disabled.

To secure correct behavior in the SPI, the pins used by the SPI must be configured in the GPIO peripheral as described in *Table 60: GPIO configuration* on page 271 prior to enabling the SPI. The SCK must always be connected to a pin, and that pin's input buffer must always be connected for the SPI to work. This configuration must be retained in the GPIO for the selected IOs as long as the SPI is enabled.

Only one peripheral can be assigned to drive a particular GPIO pin at a time, failing to do so may result in unpredictable behavior.

Table 60: GPIO configuration

SPI master signal	SPI master pin	Direction	Output value
SCK	As specified in PSEL.SCK	Output	Same as CONFIG.CPOL
MOSI	As specified in PSEL.MOSI	Output	0
MISO	As specified in PSEL.MISO	Input	Not applicable

29.2 Shared resources

The SPI shares registers and other resources with other peripherals that have the same ID as the SPI. Therefore, the user must disable all peripherals that have the same ID as the SPI before the SPI can be configured and used.

Disabling a peripheral that has the same ID as the SPI will not reset any of the registers that are shared with the SPI. It is therefore important to configure all relevant SPI registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 36 for details on peripherals and their IDs.

29.3 SPI master transaction sequence

An SPI master transaction consists of a sequence started by the START task followed by a number of events, and finally the STOP task.

An SPI master transaction is started by triggering the START task. The ENDTX event will be generated when the transmitter has transmitted all bytes in the TXD buffer as specified in the TXD.MAXCNT register. The ENDRX event will be generated when the receiver has filled the RXD buffer, i.e. received the last possible byte as specified in the RXD.MAXCNT register.

Following a START task, the SPI master will generate an END event when both ENDRX and ENDTX have been generated.

The SPI master is stopped by triggering the STOP task. A STOPPED event is generated when the SPI master has stopped.

If the ENDRX event has not already been generated when the SPI master has come to a stop, the SPI master will generate the ENDRX event explicitly even though the RX buffer is not full.

If the ENDTX event has not already been generated when the SPI master has come to a stop, the SPI master will generate the ENDTX event explicitly even though all bytes in the TXD buffer, as specified in the TXD.MAXCNT register, have not been transmitted.

The SPI master is a synchronous interface, and for every byte that is sent, a different byte will be received at the same time; this is illustrated in *Figure 66: SPI master transaction* on page 272.

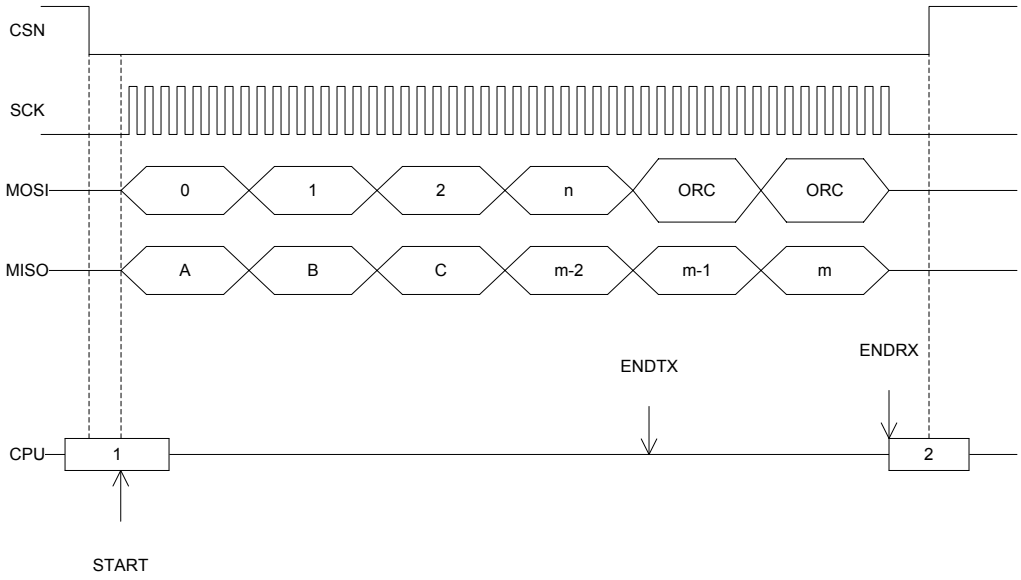

Figure 66: SPI master transaction

29.4 EasyDMA

The SPI master implements EasyDMA for reading and writing of data packets from and to the DATA RAM without CPU involvement.

The RXD.PTR and TXD.PTR point to the RXD buffer (receive buffer) and TXD buffer (transmit buffer) respectively, see *Figure 65: SPI master with EasyDMA (SPIM)* on page 270. RXD.MAXCNT and TXD.MAXCNT specify the maximum number of bytes allocated to the buffers.

The SPI master will automatically stop transmitting after TXD.MAXCNT bytes have been transmitted and RXD.MAXCNT bytes have been received. If TXD.MAXCNT is larger than RXD.MAXCNT, the superfluous received bytes will be ignored. If RXD.MAXCNT is larger than TXD.MAXCNT, the remaining transmitted bytes will contain the value defined in the ORC register.

If the RXD.PTR and the TXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 34 for more information about the different memory regions.

The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next transmission immediately after having received the STARTED event.

The ENDRX/ENDTX event indicate that EasyDMA has finished accessing respectively the RX/TX buffer in RAM. The END event gets generated when both RX and TX are finished accessing the buffers in RAM.

29.4.1 EasyDMA list

EasyDMA supports the following list types:

- Array list

EasyDMA array list

The EasyDMA array list can be represented by the data structure ArrayList_type as illustrated in the code example below. This data structure include only a buffer with size equal to Channel.MAXCNT. EasyDma will use the Channel.MAXCNT register to determine when the buffer is full. Replace 'Channel' by the specific data channel you want to use, for instance 'NRF_SPIM->RXD', 'NRF_SPIM->TXD', 'NRF_TWIM->RXD', etc.

The Channel.MAXCNT register cannot be specified larger than the actual size of the buffer. If Channel.MAXCNT is specified larger than the size of the buffer, the EasyDMA channel may overflow the buffer.

This array list does not provide a mechanism to explicitly specify where the next item in the list is located, instead it assumes that the list is organized as a linear array where items are located one after the other in RAM.

```
#define BUFFER_SIZE  4

typedef struct ArrayList
{
  uint8_t buffer[BUFFER_SIZE];
} ArrayList_type;

ArrayList_type MyArrayList[3];

//replace 'Channel' below by the specific data channel you want to use,
//         for instance 'NRF_SPIM->RXD', 'NRF_TWIM->RXD', etc.
Channel.MAXCNT = BUFFER_SIZE;
Channel.PTR = &MyArrayList;
```

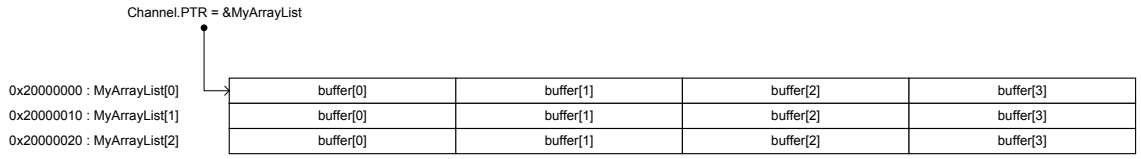

Figure 67: EasyDMA array list

29.5 Registers

Table 61: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40003000	SPIM	SPIM0	SPI master 0	
0x40004000	SPIM	SPIM1	SPI master 1	
0x40023000	SPIM	SPIM2	SPI master 2.	

Table 62: Register Overview

Register	Offset	Description
TASKS_START	0x010	Start SPI transaction
TASKS_STOP	0x014	Stop SPI transaction
TASKS_SUSPEND	0x01C	Suspend SPI transaction
TASKS_RESUME	0x020	Resume SPI transaction
EVENTS_STOPPED	0x104	SPI transaction has stopped
EVENTS_ENDRX	0x110	End of RXD buffer reached
EVENTS_END	0x118	End of RXD buffer and TXD buffer reached
EVENTS_ENDTX	0x120	End of TXD buffer reached
EVENTS_STARTED	0x14C	Transaction started
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	Enable SPIM
PSEL.SCK	0x508	Pin select for SCK
PSEL.MOSI	0x50C	Pin select for MOSI signal

Register	Offset	Description
PSEL.MISO	0x510	Pin select for MISO signal
FREQUENCY	0x524	SPI frequency
RXD.PTR	0x534	Data pointer
RXD.MAXCNT	0x538	Maximum number of buffer words to transfer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last transaction
RXD.LIST	0x540	EasyDMA list type
TXD.PTR	0x544	Data pointer
TXD.MAXCNT	0x548	Maximum number of buffer words to transfer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last transaction
TXD.LIST	0x550	EasyDMA list type
CONFIG	0x554	Configuration register
ORC	0x5C0	Over-read character. Character clocked out in case and over-read of the TXD buffer.

29.5.1 SHORTS

Address offset: 0x200

Shortcut register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		A																	
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																														
A	RW	END_START			Shortcut between EVENTS_END event and TASKS_START task																																
			Disabled	0	Disable shortcut																														
			Enabled	1	Enable shortcut																														

29.5.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																E										D		C		B			A		
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																														
A	RW	STOPPED			Write '1' to Enable interrupt on EVENTS_STOPPED event																																
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
B	RW	ENDRX			Write '1' to Enable interrupt on EVENTS_ENDRX event																																
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
C	RW	END			Write '1' to Enable interrupt on EVENTS_END event																																
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
D	RW	ENDTX			Write '1' to Enable interrupt on EVENTS_ENDTX event																																
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
E	RW	STARTED			Write '1' to Enable interrupt on EVENTS_STARTED event																																
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														

29.5.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																E											D		C		B			A	
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	STOPPED																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	ENDRX																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	END																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
D	RW	ENDTX																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
E	RW	STARTED																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															

29.5.4 ENABLE

Address offset: 0x500

Enable SPIM

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	ENABLE																																	
			Disabled	0																															
			Enabled	7																															

29.5.5 PSEL.SCK

Address offset: 0x508

Pin select for SCK

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				C																											A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PIN		[0..31]																															
C	RW	CONNECT																																	
			Disconnected	1																															
			Connected	0																															

29.5.6 PSEL.MOSI

Address offset: 0x50C

Pin select for MOSI signal

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				C																											A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PIN		[0..31]																															
C	RW	CONNECT																																	
			Disconnected	1																															
			Connected	0																															

29.5.7 PSEL.MISO

Address offset: 0x510

Pin select for MISO signal

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				C																											A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PIN		[0..31]																															
C	RW	CONNECT																																	
			Disconnected	1																															
			Connected	0																															

29.5.8 FREQUENCY

Address offset: 0x524

SPI frequency

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x04000000				**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	FREQUENCY																																	
			K125	0x02000000																															
			K250	0x04000000																															
			K500	0x08000000																															
			M1	0x10000000																															
			M2	0x20000000																															
			M4	0x40000000																															
			M8	0x80000000																															

29.5.9 RXD.PTR

Address offset: 0x534

Data pointer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PTR																																	

29.5.10 RXD.MAXCNT

Address offset: 0x538

Maximum number of buffer words to transfer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
A	RW	MAXCNT																										Maximum number of buffer words to transfer							

29.5.11 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
A	R	AMOUNT																										Number of bytes transferred in the last transaction							

29.5.12 RXD.LIST

Address offset: 0x540

EasyDMA list type

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
A	RW	LIST																										List type							
			Disabled	0																								Disable EasyDMA list							
			ArrayList	1																								Use array list							

29.5.13 TXD.PTR

Address offset: 0x544

Data pointer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
A	RW	PTR																										Data pointer							

29.5.14 TXD.MAXCNT

Address offset: 0x548

Maximum number of buffer words to transfer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
A	RW	MAXCNT																										Maximum number of buffer words to transfer							

29.5.15 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value** **Description**
A	R	AMOUNT		Number of bytes transferred in the last transaction

29.5.16 TXD.LIST

Address offset: 0x550

EasyDMA list type

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value** **Description**
A	RW	LIST		List type
			Disabled	0 Disable EasyDMA list
			ArrayList	1 Use array list

29.5.17 CONFIG

Address offset: 0x554

Configuration register

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value** **Description**
A	RW	ORDER		Bit order
			MsbFirst	0 Most significant bit shifted out first
			LsbFirst	1 Least significant bit shifted out first
B	RW	CPHA		Serial clock (SCK) phase
			Leading	0 Sample on leading edge of clock, shift serial data on trailing edge
			Trailing	1 Sample on trailing edge of clock, shift serial data on leading edge
C	RW	CPOL		Serial clock (SCK) polarity
			ActiveHigh	0 Active high
			ActiveLow	1 Active low

29.5.18 ORC

Address offset: 0x5C0

Over-read character. Character clocked out in case and over-read of the TXD buffer.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value** **Description**
A	RW	ORC		Over-read character. Character clocked out in case and over-read of the TXD buffer.

29.6 Electrical Specification

29.6.1 SPIM master interface

Symbol	Description	Min.	Typ.	Max.	Units
f_{SPIM}	Bit rates for SPIM[23]			8	Mbps
$I_{SPIM,2Mbps}$	Run current for SPIM, 2 Mbps		50		µA
$I_{SPIM,8Mbps}$	Run current for SPIM, 8 Mbps		50		µA
$I_{SPIM,IDLE}$	Idle current for SPIM (STARTed, no CSN activity)		1		µA
$t_{SPIM,START,LP}$	Time from STARTRX/STARTTX task to RX/TX active, low power mode		3		µs
$t_{SPIM,START,CL}$	Time from STARTRX/STARTTX task to RX/TX active, constant latency mode		1		µs

29.6.2 Serial Peripheral Interface Master (SPIM) electrical specifications

Symbol	Description	Min.	Typ.	Max.	Units
$t_{SPIM,CSCK,8Mbps}$	SCK period at 8Mbps		125		ns
$t_{SPIM,CSCK,4Mbps}$	SCK period at 4Mbps		250		ns
$t_{SPIM,CSCK,2Mbps}$	SCK period at 2Mbps		500		ns
$t_{SPIM,RSCK,LD}$	SCK rise time, low drive[a]			$t_{RF,25pF}$	
$t_{SPIM,RSCK,HD}$	SCK rise time, high drive[a]			$t_{HRF,25pF}$	
$t_{SPIM,FSCK,LD}$	SCK fall time, low drive[a]			$t_{RF,25pF}$	
$t_{SPIM,FSCK,HD}$	SCK fall time, high drive[a]			$t_{HRF,25pF}$	
$t_{SPIM,WHSCK}$	SCK high time[a]	$(0.5*t_{CSCK})$ – t_{RSCK}			
$t_{SPIM,WLSCK}$	SCK low time[a]	$(0.5*t_{CSCK})$ – t_{FSCK}			
$t_{SPIM,SUMI}$	MISO to CLK edge setup time	5			ns
$t_{SPIM,HMI}$	CLK edge to MISO hold time	5			ns
$t_{SPIM,VMO}$	CLK edge to MOSI valid			40	ns
$t_{SPIM,HMO}$	MOSI hold time after CLK edge	0			ns

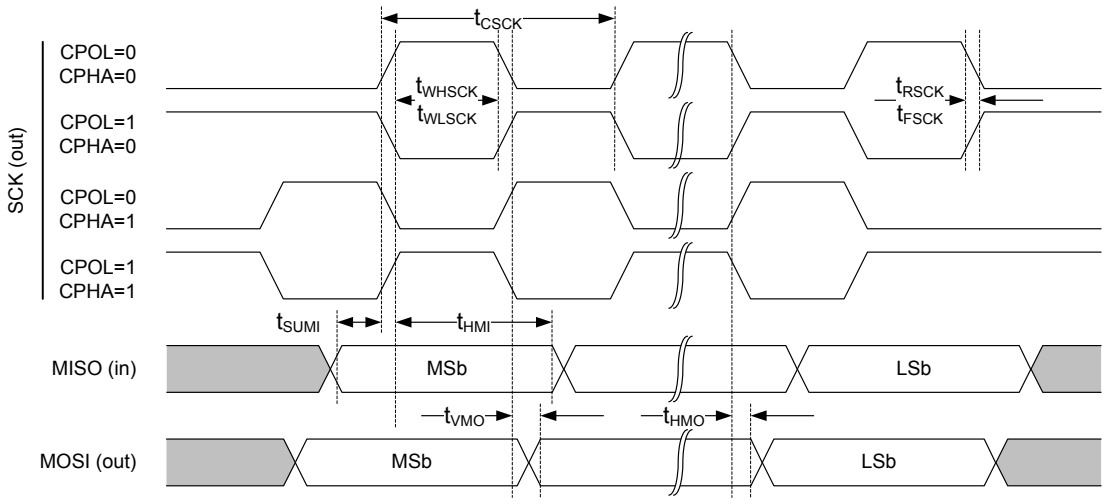

Figure 68: SPIM timing diagram

[23] Higher bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

[a] At 25pF load, including GPIO pin capacitance, see GPIO spec.

30 SPI slave (SPIS)

SPI slave (SPIS) is implemented with EasyDMA support for ultra low power serial communication from an external SPI master. EasyDMA in conjunction with hardware-based semaphore mechanisms removes all real-time requirements associated with controlling the SPI slave from a low priority CPU execution context.

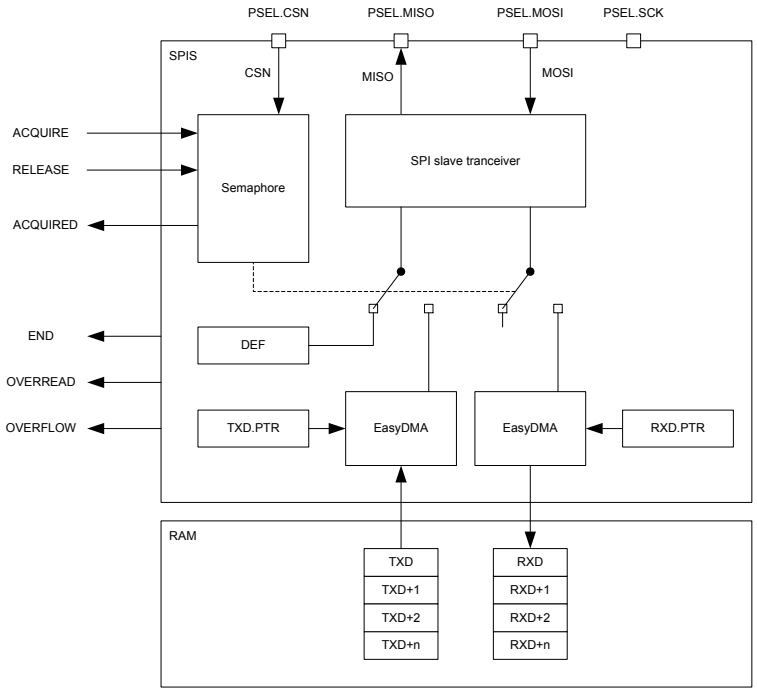

Figure 69: SPI slave

The SPIS supports SPI modes 0 through 3. The CONFIG register allows setting CPOL and CPHA appropriately.

Table 63: SPI modes

Mode	Clock polarity CPOL	Clock phase CPHA
SPI_MODE	0 (Leading)	0 (Active High)
SPI_MODE	0 (Leading)	1 (Active Low)
SPI_MODE	1 (Trailing)	0 (Active High)
SPI_MODE	1 (Trailing)	1 (Active Low)

30.1 Pin configuration

The different signals CSN, SCK, MOSI, and MISO associated with the SPI slave are mapped to physical pins according to the configuration specified in the PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers respectively. If the CONNECT field of any of these registers is set to Disconnected, the associated SPI slave signal will not be connected to any physical pins.

The PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers and their configurations are only used as long as the SPI slave is enabled, and retained only as long as the device is in System ON mode, see *POWER* chapter for more information about power modes. PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO must only be configured when the SPI slave is disabled.

To secure correct behavior in the SPI slave, the pins used by the SPI slave must be configured in the GPIO peripheral as described in *Table 64: Pin configuration* on page 281 prior to enabling the SPI slave. This is to secure that the pins used by the SPI slave are driven correctly if the SPI slave itself is temporarily disabled or the device temporarily enters System OFF. This configuration must be retained in the GPIO for the selected I/Os as long as the SPI slave is to be recognized by an external SPI master.

The MISO line is set in high impedance as long as the SPI slave is not selected with CSN.

Only one peripheral can be assigned to drive a particular GPIO pin at a time, failing to do so may result in unpredictable behavior.

Table 64: Pin configuration

SPI signal	SPI pin	Direction	Output value	Comment
CSN	As specified in PSEL.CSN	Input	Not applicable	
SCK	As specified in PSEL.SCK	Input	Not applicable	
MOSI	As specified in PSEL.MOSI	Input	Not applicable	
MISO	As specified in PSEL.MISO	Input	Not applicable	Emulates that the SPI slave is not selected.

30.2 Shared resources

The SPI slave shares registers and other resources with other peripherals that have the same ID as the SPI slave. Therefore, you must disable all peripherals that have the same ID as the SPI slave before the SPI slave can be configured and used.

Disabling a peripheral that has the same ID as the SPI slave will not reset any of the registers that are shared with the SPI slave. It is important to configure all relevant SPI slave registers explicitly to secure that it operates correctly.

The Instantiation table in *Instantiation* on page 36 shows which peripherals have the same ID as the SPI slave.

30.3 EasyDMA

The SPI slave implements EasyDMA for reading and writing to and from the RAM. The END event indicates that EasyDMA has finished accessing the buffer in RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 34 for more information about the different memory regions.

30.4 SPI slave operation

SPI slave uses two memory pointers, RXD.PTR and TXD.PTR, that point to the RXD buffer (receive buffer) and TXD buffer (transmit buffer) respectively. Since these buffers are located in RAM, which can be accessed by both the SPI slave and the CPU, a hardware based semaphore mechanism is implemented to enable safe sharing.

See *Figure 70: SPI transaction when shortcut between END and ACQUIRE is enabled* on page 283.

Before the CPU can safely update the RXD.PTR and TXD.PTR pointers it must first acquire the SPI semaphore. The CPU can acquire the semaphore by triggering the ACQUIRE task and then receiving the ACQUIRED event. When the CPU has updated the RXD.PTR and TXD.PTR pointers the CPU must release the semaphore before the SPI slave will be able to acquire it. The CPU releases the semaphore by triggering the RELEASE task. This is illustrated in *Figure 70: SPI transaction when shortcut between END and ACQUIRE is enabled* on page 283. Triggering the RELEASE task when the semaphore is not granted to the CPU will have no effect.

The semaphore mechanism does not, at any time, prevent the CPU from performing read or write access to the RXD.PTR register, the TXD.PTR registers, or the RAM that these pointers are pointing to. The semaphore is only telling when these can be updated by the CPU so that safe sharing is achieved.

The semaphore is by default assigned to the CPU after the SPI slave is enabled. No ACQUIRED event will be generated for this initial semaphore handover. An ACQUIRED event will be generated immediately if the ACQUIRE task is triggered while the semaphore is assigned to the CPU.

The SPI slave will try to acquire the semaphore when CSN goes low. If the SPI slave does not manage to acquire the semaphore at this point, the transaction will be ignored. This means that all incoming data on

MOSI will be discarded, and the DEF (default) character will be clocked out on the MISO line throughout the whole transaction. This will also be the case even if the semaphore is released by the CPU during the transaction. In case of a race condition where the CPU and the SPI slave try to acquire the semaphore at the same time, as illustrated in lifeline item 2 in *Figure 70: SPI transaction when shortcut between END and ACQUIRE is enabled* on page 283, the semaphore will be granted to the CPU.

If the SPI slave acquires the semaphore, the transaction will be granted. The incoming data on MOSI will be stored in the RXD buffer and the data in the TXD buffer will be clocked out on MISO.

When a granted transaction is completed and CSN goes high, the SPI slave will automatically release the semaphore and generate the END event.

As long as the semaphore is available the SPI slave can be granted multiple transactions one after the other. If the CPU is not able to reconfigure the TXD.PTR and RXD.PTR between granted transactions, the same TX data will be clocked out and the RX buffers will be overwritten. To prevent this from happening, the END_ACQUIRE shortcut can be used. With this shortcut enabled the semaphore will be handed over to the CPU automatically after the granted transaction has completed, giving the CPU the ability to update the TXPTR and RXPTR between every granted transaction.

If the CPU tries to acquire the semaphore while it is assigned to the SPI slave, an immediate handover will not be granted. However, the semaphore will be handed over to the CPU as soon as the SPI slave has released the semaphore after the granted transaction is completed. If the END_ACQUIRE shortcut is enabled and the CPU has triggered the ACQUIRE task during a granted transaction, only one ACQUIRE request will be served following the END event.

The MAXRX register specifies the maximum number of bytes the SPI slave can receive in one granted transaction. If the SPI slave receives more than MAXRX number of bytes, an OVERFLOW will be indicated in the STATUS register and the incoming bytes will be discarded.

The MAXTX parameter specifies the maximum number of bytes the SPI slave can transmit in one granted transaction. If the SPI slave is forced to transmit more than MAXTX number of bytes, an OVERREAD will be indicated in the STATUS register and the ORC character will be clocked out.

The RXD.AMOUNT and TXD.AMOUNT registers are updated when a granted transaction is completed. The TXD.AMOUNT register indicates how many bytes were read from the TX buffer in the last transaction, that is, ORC (over-read) characters are not included in this number. Similarly, the RXD.AMOUNT register indicates how many bytes were written into the RX buffer in the last transaction.

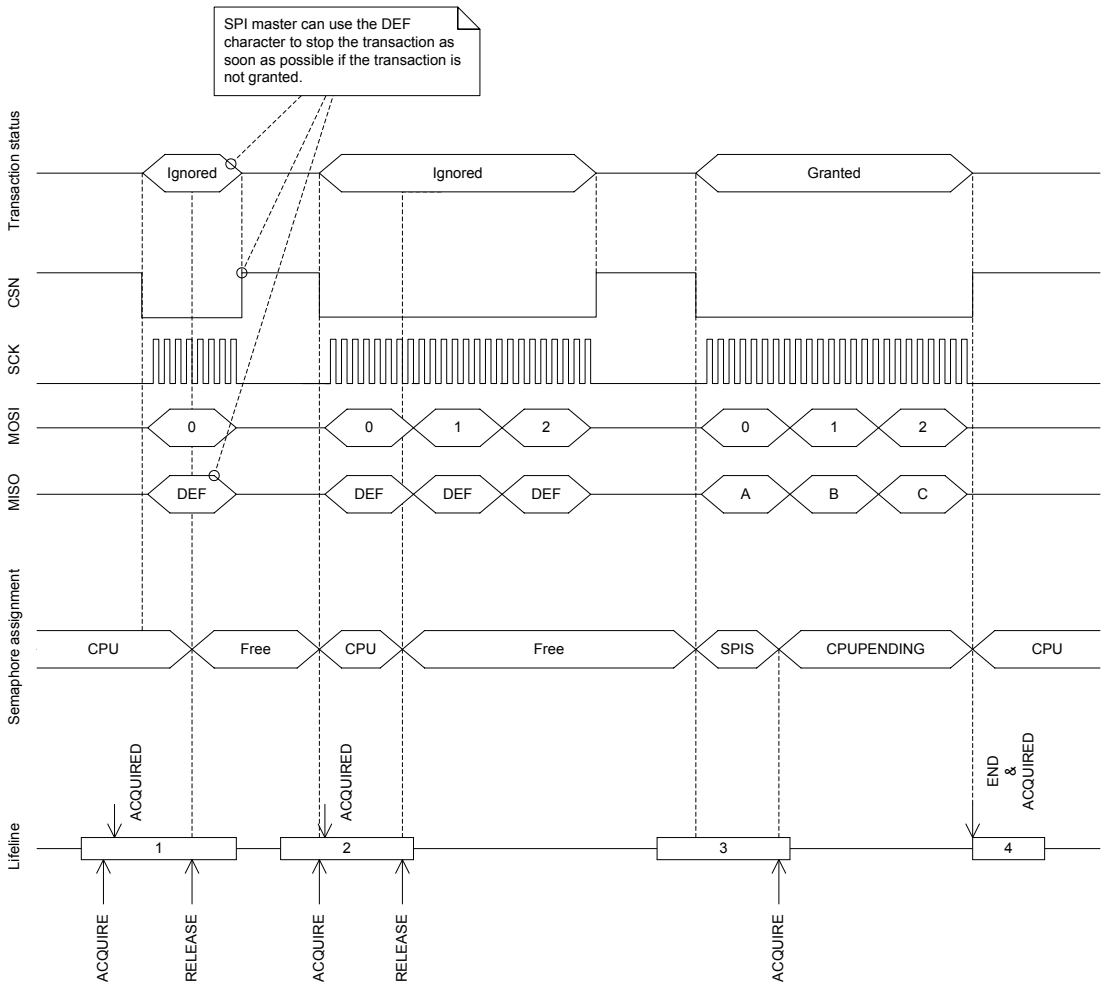

Figure 70: SPI transaction when shortcut between END and ACQUIRE is enabled

30.5 Registers

Table 65: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40003000	SPIS	SPIS0	SPI slave 0.	
0x40004000	SPIS	SPIS1	SPI slave 1	
0x40023000	SPIS	SPIS2	SPI slave 2.	

Table 66: Register Overview

Register	Offset	Description	
TASKS_ACQUIRE	0x024	Acquire SPI semaphore	
TASKS_RELEASE	0x028	Release SPI semaphore, enabling the SPI slave to acquire it	
EVENTS_END	0x104	Granted transaction completed	
EVENTS_ACQUIRED	0x128	Semaphore acquired	
SHORTS	0x200	Shortcut register	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
SEMSTAT	0x400	Semaphore status register	
STATUS	0x440	Status from last transaction	
ENABLE	0x500	Enable SPI slave	
PSELSCK	0x508	Pin select for SCK	Deprecated
PSELMISO	0x50C	Pin select for MISO	Deprecated

Register	Offset	Description	
PSELMOSI	0x510	Pin select for MOSI	Deprecated
PSELCSN	0x514	Pin select for CSN	Deprecated
PSEL.SCK	0x508	Pin select for SCK	
PSEL.MISO	0x50C	Pin select for MISO signal	
PSEL.MOSI	0x510	Pin select for MOSI signal	
PSEL.CSN	0x514	Pin select for CSN signal	
RXDPTR	0x534	RXD data pointer	Deprecated
MAXRX	0x538	Maximum number of bytes in receive buffer	Deprecated
AMOUNTRX	0x53C	Number of bytes received in last granted transaction	Deprecated
RXD.PTR	0x534	RXD data pointer	
RXD.MAXCNT	0x538	Maximum number of bytes in receive buffer	
RXD.AMOUNT	0x53C	Number of bytes received in last granted transaction	
TXDPTR	0x544	TXD data pointer	Deprecated
MAXTX	0x548	Maximum number of bytes in transmit buffer	Deprecated
AMOUNTTX	0x54C	Number of bytes transmitted in last granted transaction	Deprecated
TXD.PTR	0x544	TXD data pointer	
TXD.MAXCNT	0x548	Maximum number of bytes in transmit buffer	
TXD.AMOUNT	0x54C	Number of bytes transmitted in last granted transaction	
CONFIG	0x554	Configuration register	
DEF	0x55C	Default character. Character clocked out in case of an ignored transaction.	
ORC	0x5C0	Over-read character	

30.5.1 SHORTS

Address offset: 0x200

Shortcut register

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																														A		
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	END_ACQUIRE			Shortcut between EVENTS_END event and TASKS_ACQUIRE task
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut

30.5.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																						B									A	
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	END			Write '1' to Enable interrupt on EVENTS_END event
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
B	RW	ACQUIRED			Write '1' to Enable interrupt on EVENTS_ACQUIRED event
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

30.5.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																									B										A	
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	END																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	ACQUIRED																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															

30.5.4 SEMSTAT

Address offset: 0x400

Semaphore status register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		A	A
Reset 0x00000001				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	SEMSTAT																																	
			Free	0																															
			CPU	1																															
			SPIS	2																															
			CPUPending	3																															

30.5.5 STATUS

Address offset: 0x440

Status from last transaction

Individual bits are cleared by writing a '1' to the bits that shall be cleared

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	OVERREAD																																	
			NotPresent	0																															
			Present	1																															
			Clear	1																															
B	RW	OVERFLOW																																	
			NotPresent	0																															
			Present	1																															
			Clear	1																															

30.5.6 ENABLE

Address offset: 0x500

Enable SPI slave

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	ENABLE																																	
			Disabled	0																															

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															A	A	A	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
			Enabled								2																Enable SPI slave							

30.5.7 PSELSCK (Deprecated)

Address offset: 0x508

Pin select for SCK

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF			**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	RW	PSELSCK									[0..31]																Pin number configuration for SPI SCK signal							
			Disconnected								0xFFFFFFFF																Disconnect							

30.5.8 PSELMISO (Deprecated)

Address offset: 0x50C

Pin select for MISO

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF			**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	RW	PSELMISO									[0..31]																Pin number configuration for SPI MISO signal							
			Disconnected								0xFFFFFFFF																Disconnect							

30.5.9 PSELMOSI (Deprecated)

Address offset: 0x510

Pin select for MOSI

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF			**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	RW	PSELMOSI									[0..31]																Pin number configuration for SPI MOSI signal							
			Disconnected								0xFFFFFFFF																Disconnect							

30.5.10 PSELCSN (Deprecated)

Address offset: 0x514

Pin select for CSN

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF			**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	RW	PSELCSN									[0..31]																Pin number configuration for SPI CSN signal							
			Disconnected								0xFFFFFFFF																Disconnect							

30.5.11 PSEL.SCK

Address offset: 0x508

Pin select for SCK

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				C																											A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PIN		[0..31]																															
C	RW	CONNECT																																	
			Disconnected	1																															
			Connected	0																															

30.5.12 PSEL.MISO

Address offset: 0x50C

Pin select for MISO signal

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				C																											A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PIN		[0..31]																															
C	RW	CONNECT																																	
			Disconnected	1																															
			Connected	0																															

30.5.13 PSEL.MOSI

Address offset: 0x510

Pin select for MOSI signal

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				C																											A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PIN		[0..31]																															
C	RW	CONNECT																																	
			Disconnected	1																															
			Connected	0																															

30.5.14 PSEL.CSN

Address offset: 0x514

Pin select for CSN signal

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				C																											A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PIN		[0..31]																															
C	RW	CONNECT																																	
			Disconnected	1																															
			Connected	0																															

30.5.15 RXDPTR (Deprecated)

Address offset: 0x534

RXD data pointer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	RXDPTR			RXD data pointer

30.5.16 MAXRX (Deprecated)

Address offset: 0x538

Maximum number of bytes in receive buffer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																									A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	MAXRX			Maximum number of bytes in receive buffer

30.5.17 AMOUNTRX (Deprecated)

Address offset: 0x53C

Number of bytes received in last granted transaction

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																									A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	R	AMOUNTRX			Number of bytes received in the last granted transaction

30.5.18 RXD.PTR

Address offset: 0x534

RXD data pointer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	PTR			RXD data pointer

30.5.19 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																									A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	MAXCNT			Maximum number of bytes in receive buffer

30.5.20 RXD.AMOUNT

Address offset: 0x53C

Number of bytes received in last granted transaction

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																									A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	R	AMOUNT			Number of bytes received in the last granted transaction

30.5.21 TXDPTR (Deprecated)

Address offset: 0x544

TXD data pointer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TXDPTR			TXD data pointer

30.5.22 MAXTX (Deprecated)

Address offset: 0x548

Maximum number of bytes in transmit buffer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																									A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	MAXTX			Maximum number of bytes in transmit buffer

30.5.23 AMOUNTTX (Deprecated)

Address offset: 0x54C

Number of bytes transmitted in last granted transaction

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																									A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	R	AMOUNTTX			Number of bytes transmitted in last granted transaction

30.5.24 TXD.PTR

Address offset: 0x544

TXD data pointer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	PTR			TXD data pointer

30.5.25 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																									A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	MAXCNT			Maximum number of bytes in transmit buffer

30.5.26 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transmitted in last granted transaction

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	R	AMOUNT			Number of bytes transmitted in last granted transaction

30.5.27 CONFIG

Address offset: 0x554

Configuration register

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	ORDER			Bit order
			MsbFirst	0	Most significant bit shifted out first
			LsbFirst	1	Least significant bit shifted out first
B	RW	CPHA			Serial clock (SCK) phase
			Leading	0	Sample on leading edge of clock, shift serial data on trailing edge
			Trailing	1	Sample on trailing edge of clock, shift serial data on leading edge
C	RW	CPOL			Serial clock (SCK) polarity
			ActiveHigh	0	Active high
			ActiveLow	1	Active low

30.5.28 DEF

Address offset: 0x55C

Default character. Character clocked out in case of an ignored transaction.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	DEF			Default character. Character clocked out in case of an ignored transaction.

30.5.29 ORC

Address offset: 0x5C0

Over-read character

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	ORC			Over-read character. Character clocked out after an over-read of the transmit buffer.

30.6 Electrical Specification

30.6.1 SPIS slave interface electrical specifications

Symbol	Description	Min.	Typ.	Max.	Units
f_{SPIS}	Bit rates for SPIS[24]			8	Mbps
$I_{SPIS,2Mbps}$	Run current for SPIS, 2 Mbps		45		µA
$I_{SPIS,8Mbps}$	Run current for SPIS, 8 Mbps		45		µA
$I_{SPIS,IDLE}$	Idle current for SPIS (STARTed, no CSN activity)		1		µA
$t_{SPIS,LP,START}$	Time from RELEASE task to RX/TX active, Low power mode		3		µs
$t_{SPIS,CL,START}$	Time from RELEASE task to RX/TX active, Constant latency mode		1		µs

30.6.2 Serial Peripheral Interface Slave (SPIS) timing specifications

Symbol	Description	Min.	Typ.	Max.	Units
$t_{SPIS,CSCKIN,8Mbps}$	SCK input period at 8Mbps		125		ns
$t_{SPIS,CSCKIN,4Mbps}$	SCK input period at 4Mbps		250		ns
$t_{SPIS,CSCKIN,2Mbps}$	SCK input period at 2Mbps		500		ns
$t_{SPIS,RFSCKIN}$	SCK input rise/fall time			30	ns
$t_{SPIS,WHSCKIN}$	SCK input high time	30			ns
$t_{SPIS,WLSCKIN}$	SCK input low time	30			ns
$t_{SPIS,SUCSN,LP}$	CSN to CLK setup time, Low power mode	7000			ns
$t_{SPIS,SUCSN,CL}$	CSN to CLK setup time, Constant latency mode	2000			ns
$t_{SPIS,HCSN}$	CLK to CSN hold time	2000			ns
$t_{SPIS,ASO}$	CSN to MISO driven[a]			60	ns
$t_{SPIS,DISSO}$	CSN to MISO disabled[a]			60	ns
$t_{SPIS,CWH}$	CSN inactive time	300			ns
$t_{SPIS,VSO}$	CLK edge to MISO valid			30	ns
$t_{SPIS,HSO}$	MISO hold time after CLK edge	5[25]			ns
$t_{SPIS,SUSI}$	MOSI to CLK edge setup time	20			ns
$t_{SPIS,HSI}$	CLK edge to MOSI hold time	20			ns

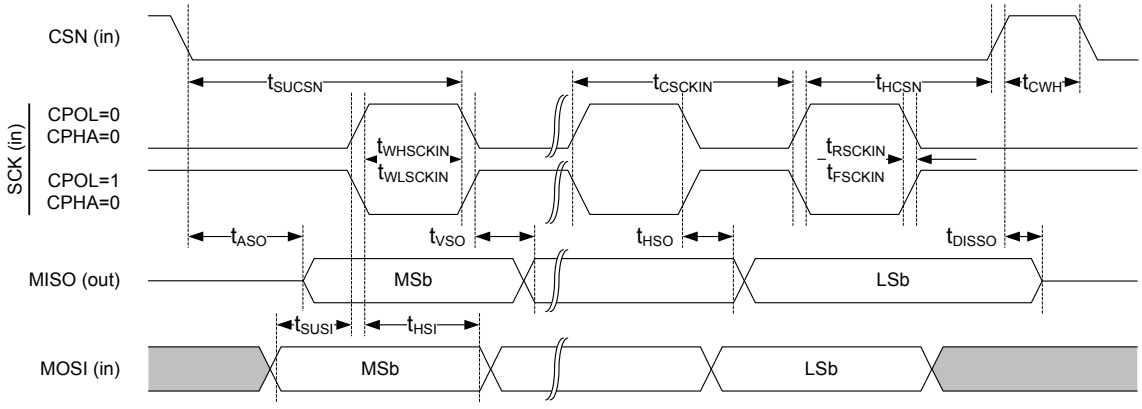

Figure 71: SPIS timing diagram

[24] Higher bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

[a] At 25pF load, including GPIO capacitance, see GPIO spec.

[25] This is to ensure compatibility to SPI masters sampling MISO on the same edge as MOSI is output

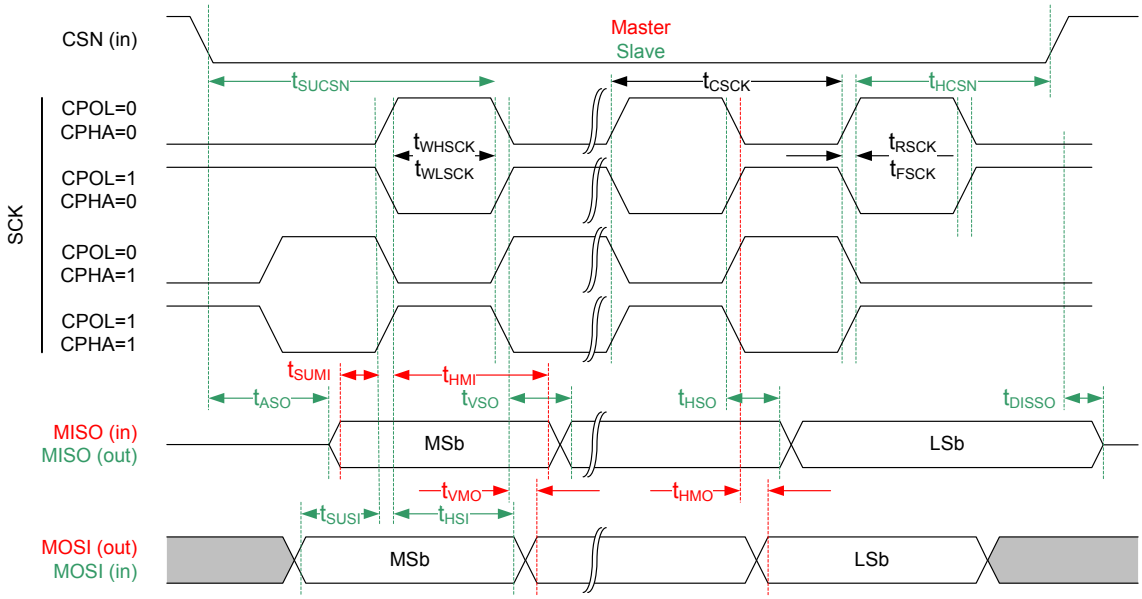

Figure 72: Common SPIM and SPIS timing diagram

31 I2C compatible two-wire interface master with EasyDMA (TWIM)

TWI master with EasyDMA (TWIM) is a two wire half-duplex master which can communicate with multiple slave devices connected to the same bus

Listed here are the main features for TWIM:

- I2C compatible
- 100 kbps, 250 kbps, or 400 kbps
- Support for clock stretching
- EasyDMA

The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. TWIM is not compatible with CBUS.

The GPIOs used for each two-wire interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of board space and signal routing.

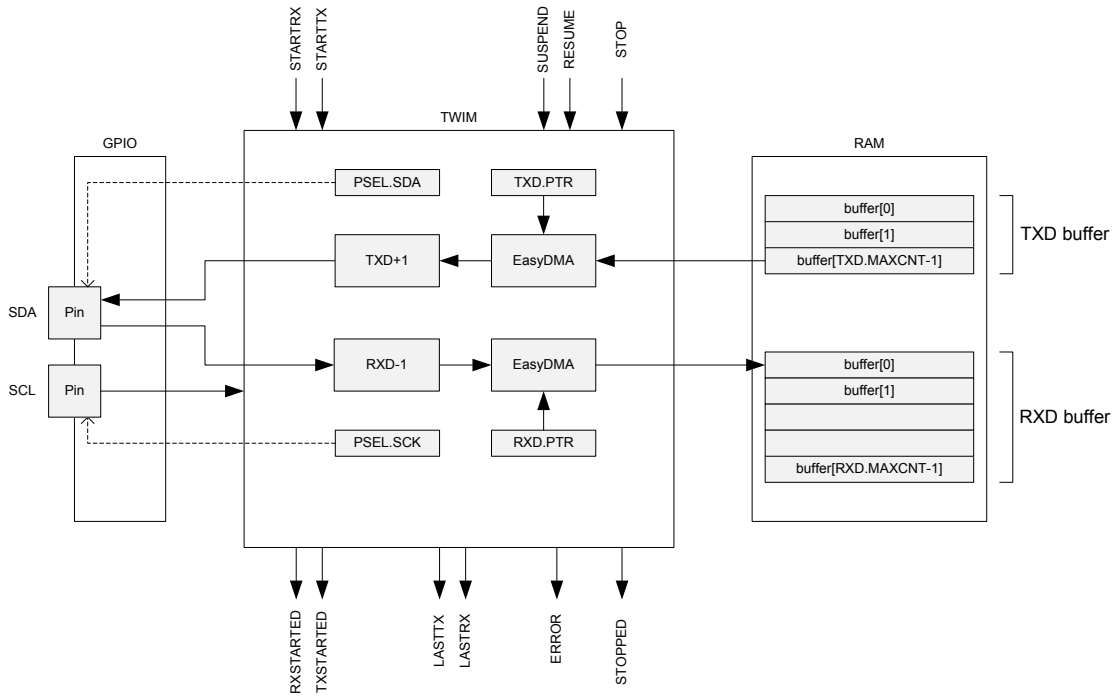

Figure 73: TWI master with EasyDMA

A TWI setup comprising one master and three slaves is illustrated in *Figure 74: A typical TWI setup comprising one master and three slaves* on page 293. This TWIM is only able to operate as a single master on the TWI bus. Multi-master bus configuration is not supported.

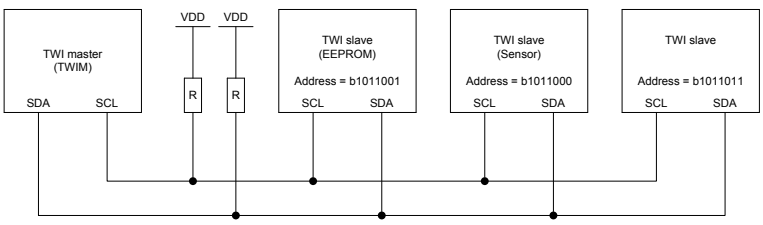

Figure 74: A typical TWI setup comprising one master and three slaves

This TWI master supports clock stretching performed by the slaves. The TWI master is started by triggering the STARTTX or STARTRX tasks, and stopped by triggering the STOP task. The TWI master will generate a STOPPED event when it has stopped following a STOP task.

After the TWI master is started, the STARTTX task or the STARTRX task should not be triggered again before the TWI master has stopped, i.e. following a LASTRX, LASTTX or STOPPED event.

If a NACK is clocked in from the slave, the TWI master will generate an ERROR event.

31.1 Master mode pin configuration

The different signals SCL and SDA associated with the TWI master are mapped to physical pins according to the configuration specified in the PSEL.SCL and PSEL.SDA registers respectively.

The PSEL.SCL and PSEL.SDA registers and their configurations are only used as long as the TWI master is enabled, and retained only as long as the device is in ON mode. PSEL.SCL, PSEL.SDA must only be configured when the TWI master is disabled.

To secure correct signal levels on the pins used by the TWI master when the system is in OFF mode, and when the TWI master is disabled, these pins must be configured in the GPIO peripheral as described in *Table 67: GPIO configuration* on page 294.

Only one peripheral can be assigned to drive a particular GPIO pin at a time, failing to do so may result in unpredictable behavior.

Table 67: GPIO configuration

TWI master signal	TWI master pin	Direction	Drive strength	Output value
SCL	As specified in PSEL.SCL	Input	S0D1	Not applicable
SDA	As specified in PSEL.SDA	Input	S0D1	Not applicable

31.2 Shared resources

The TWI master shares registers and other resources with other peripherals that have the same ID as the TWI master. Therefore, you must disable all peripherals that have the same ID as the TWI master before the TWI master can be configured and used.

Disabling a peripheral that has the same ID as the TWI master will not reset any of the registers that are shared with the TWI master. It is therefore important to configure all relevant registers explicitly to secure that the TWI master operates correctly.

The Instantiation table in *Instantiation* on page 36 shows which peripherals have the same ID as the TWI.

31.3 EasyDMA

The TWI master implements EasyDMA for reading and writing to and from the RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 34 for more information about the different memory regions.

The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next RX/TX transmission immediately after having received the RXSTARTED/TXSTARTED event.

The STOPPED event indicates that EasyDMA has finished accessing the buffer in RAM.

31.3.1 EasyDMA list

EasyDMA supports the following list types:

- Array list

EasyDMA array list

The EasyDMA array list can be represented by the data structure ArrayList_type as illustrated in the code example below. This data structure include only a buffer with size equal to Channel.MAXCNT. EasyDma will use the Channel.MAXCNT register to determine when the buffer is full. Replace 'Channel' by the specific data channel you want to use, for instance 'NRF_SPIM->RXD', 'NRF_SPIM->TXD', 'NRF_TWIM->RXD', etc.

The Channel.MAXCNT register cannot be specified larger than the actual size of the buffer. If Channel.MAXCNT is specified larger than the size of the buffer, the EasyDMA channel may overflow the buffer.

This array list does not provide a mechanism to explicitly specify where the next item in the list is located, instead it assumes that the list is organized as a linear array where items are located one after the other in RAM.

```
#define BUFFER_SIZE  4

typedef struct ArrayList
{
  uint8_t buffer[BUFFER_SIZE];
} ArrayList_type;

ArrayList_type MyArrayList[3];

//replace 'Channel' below by the specific data channel you want to use,
//         for instance 'NRF_SPIM->RXD', 'NRF_TWIM->RXD', etc.
Channel.MAXCNT = BUFFER_SIZE;
Channel.PTR = &MyArrayList;
```

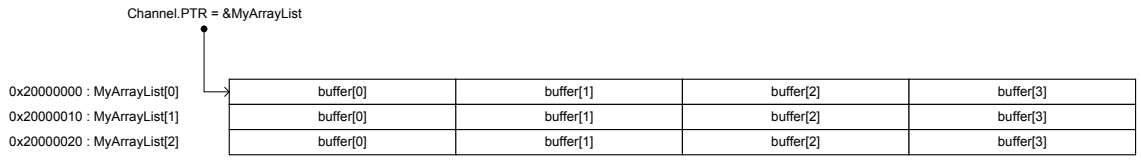

Figure 75: EasyDMA array list

31.4 Master write sequence

A TWI master write sequence is started by triggering the STARTTX task. After the STARTTX task has been triggered, the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 0 (WRITE=0, READ=1).

The address must match the address of the slave device that the master wants to write to. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) generated by the slave.

After receiving the ACK bit, the TWI master will clock out the data bytes found in the transmit buffer located in RAM at the address specified in the TXD.PTR register. Each byte clocked out from the master will be followed by an ACK/NACK bit clocked in from the slave.

A typical TWI master write sequence is illustrated in *Figure 76: TWI master writing data to a slave* on page 296. Occurrence 2 in the figurte illustrates clock stretching performed by the TWI master following a SUSPEND task.

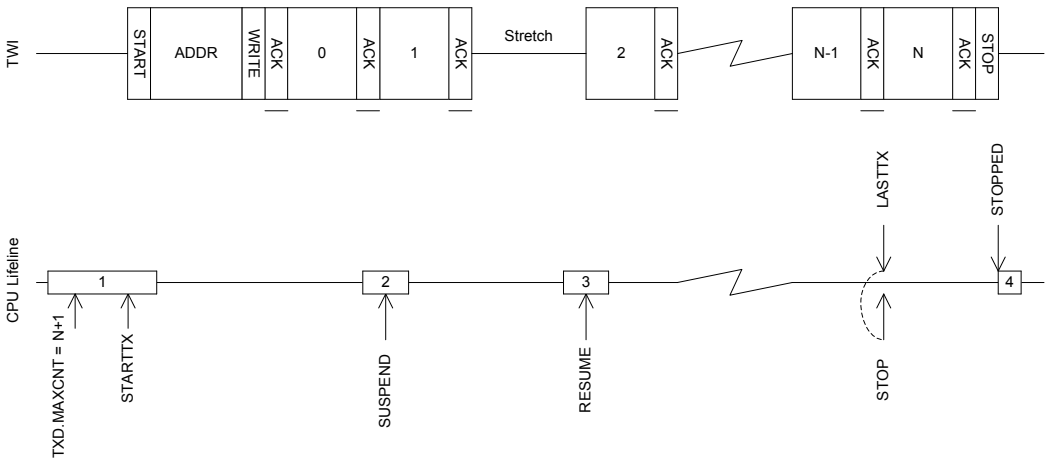

Figure 76: TWI master writing data to a slave

The TWI master will generate a LASTTX event when it starts to transmit the last byte, this is illustrated in *Figure 76: TWI master writing data to a slave* on page 296

The TWI master is stopped by triggering the STOP task, this task should be triggered during the transmission of the last byte to secure that the TWI will stop as fast as possible after sending the last byte. It is safe to use the shortcut between LASTTX and STOP to accomplish this.

Note that the TWI master does not stop by itself when the whole RAM buffer has been sent, or when an error occurs. The STOP task must be issued, through the use of a local or PPI shortcut, or in software as part of the error handler.

31.5 Master read sequence

A TWI master read sequence is started by triggering the STARTRX task. After the STARTRX task has been triggered the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 1 (WRITE = 0, READ = 1). The address must match the address of the slave device that the master wants to read from. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK = 1) generated by the slave.

After having sent the ACK bit the TWI slave will send data to the master using the clock generated by the master.

Data received will be stored in RAM at the address specified in the RXD.PTR register. The TWI master will generate an ACK after all but the last byte received from the slave. The TWI master will generate a NACK after the last byte received to indicate that the read sequence shall stop.

A typical TWI master read sequence is illustrated in *Figure 77: The TWI master reading data from a slave* on page 297. Occurrence 2 in the figure illustrates clock stretching performed by the TWI master following a SUSPEND task.

The TWI master will generate a LASTRX event when it is ready to receive the last byte, this is illustrated in *Figure 77: The TWI master reading data from a slave* on page 297. If RXD.MAXCNT > 1 the LASTRX event is generated after sending the ACK of the previously received byte. If RXD.MAXCNT = 1 the LASTRX event is generated after receiving the ACK following the address and READ bit.

The TWI master is stopped by triggering the STOP task, this task must be triggered before the NACK bit is supposed to be transmitted. The STOP task can be triggered at any time during the reception of the last byte. It is safe to use the shortcut between LASTRX and STOP to accomplish this.

Note that the TWI master does not stop by itself when the RAM buffer is full, or when an error occurs. The STOP task must be issued, through the use of a local or PPI shortcut, or in software as part of the error handler.

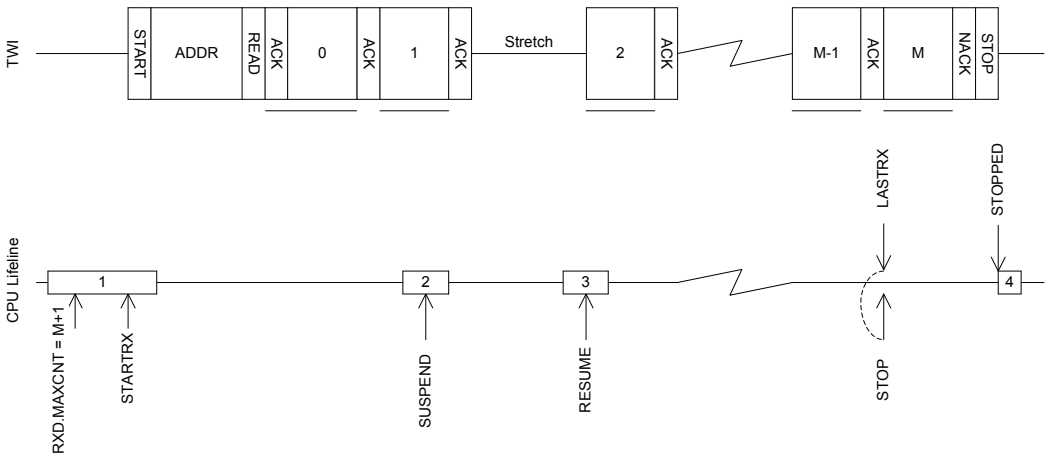

Figure 77: The TWI master reading data from a slave

31.6 Master repeated start sequence

A typical repeated start sequence is one in which the TWI master writes two bytes to the slave followed by reading four bytes from the slave. This example uses shortcuts to perform the simplest type of repeated start sequence, i.e. one write followed by one read. The same approach can be used to perform a repeated start sequence where the sequence is read followed by write.

The figure *Figure 78: A repeated start sequence, where the TWI master writes two bytes followed by reading 4 bytes from the slave* on page 297 illustrates this:

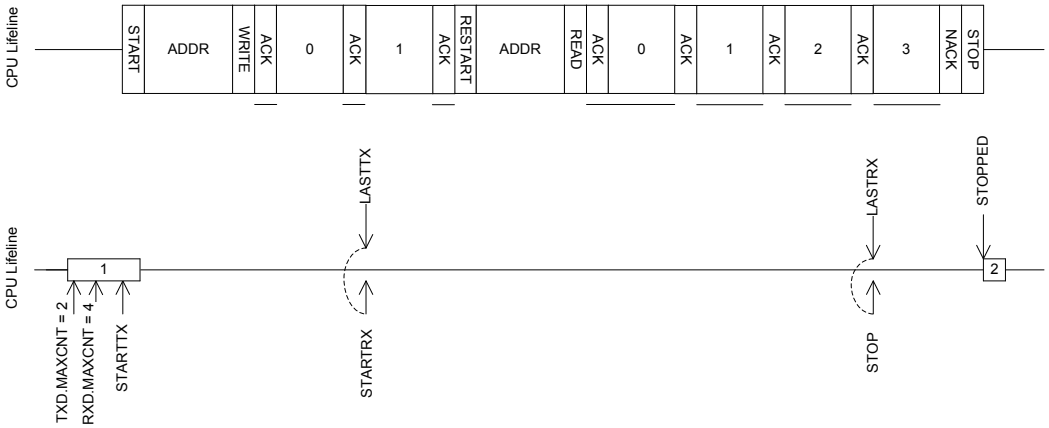

Figure 78: A repeated start sequence, where the TWI master writes two bytes followed by reading 4 bytes from the slave

If a more complex repeated start sequence is needed and the TWI firmware drive is serviced in a low priority interrupt it may be necessary to use the SUSPEND task to guarantee that the correct tasks are generated at the correct time. This is illustrated in *Figure 79: A double repeated start sequence using the SUSPEND task to secure safe operation in low priority interrupts* on page 298.

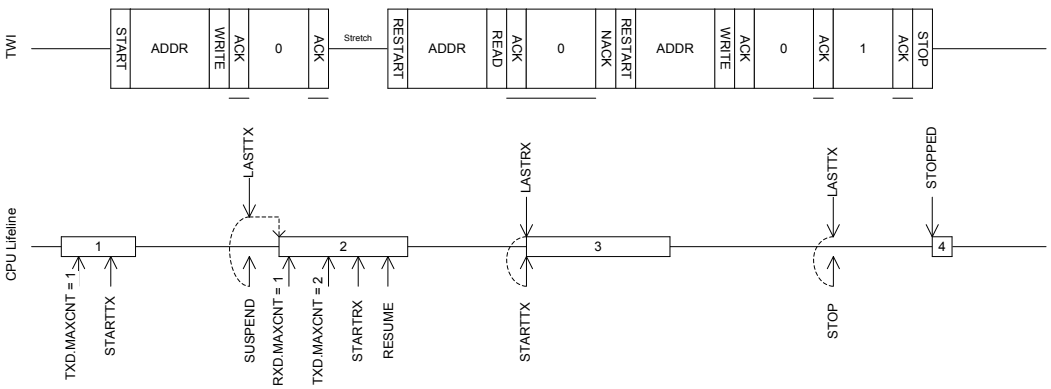

Figure 79: A double repeated start sequence using the SUSPEND task to secure safe operation in low priority interrupts

31.7 Registers

Table 68: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40003000	TWIM	TWIM0	Two-wire interface master 0	
0x40004000	TWIM	TWIM1	Two-wire interface master 1	

Table 69: Register Overview

Register	Offset	Description
TASKS_STARTRX	0x000	Start TWI receive sequence
TASKS_STARTTX	0x008	Start TWI transmit sequence
TASKS_STOP	0x014	Stop TWI transaction
TASKS_SUSPEND	0x01C	Suspend TWI transaction
TASKS_RESUME	0x020	Resume TWI transaction
EVENTS_STOPPED	0x104	TWI stopped
EVENTS_ERROR	0x124	TWI error
EVENTS_RXSTARTED	0x14C	Receive sequence started
EVENTS_TXSTARTED	0x150	Transmit sequence started
EVENTS_LASTRX	0x15C	Byte boundary, starting to receive the last byte
EVENTS_LASTTX	0x160	Byte boundary, starting to transmit the last byte
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x4C4	Error source
ENABLE	0x500	Enable TWIM
PSEL.SCL	0x508	Pin select for SCL signal
PSEL.SDA	0x50C	Pin select for SDA signal
FREQUENCY	0x524	TWI frequency
RXD.PTR	0x534	Data pointer
RXD.MAXCNT	0x538	Maximum number of buffer words to transfer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last transaction
RXD.LIST	0x540	EasyDMA list type
TXD.PTR	0x544	Data pointer
TXD.MAXCNT	0x548	Maximum number of buffer words to transfer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last transaction
TXD.LIST	0x550	EasyDMA list type
ADDRESS	0x588	Address used in the TWI transfer

31.7.1 SHORTS

Address offset: 0x200

Shortcut register

Bit number					31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																								F		D	C	B	A							
Reset 0x00000000					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																															
A	RW	LASTTX_STARTRX			Shortcut between *EVENTS_LASTTX* event and *TASKS_STARTRX* task																																	
			Disabled	0	Disable shortcut																															
			Enabled	1	Enable shortcut																															
B	RW	LASTTX_SUSPEND			Shortcut between *EVENTS_LASTTX* event and *TASKS_SUSPEND* task																																	
			Disabled	0	Disable shortcut																															
			Enabled	1	Enable shortcut																															
C	RW	LASTTX_STOP			Shortcut between *EVENTS_LASTTX* event and *TASKS_STOP* task																																	
			Disabled	0	Disable shortcut																															
			Enabled	1	Enable shortcut																															
D	RW	LASTRX_STARTTX			Shortcut between *EVENTS_LASTRX* event and *TASKS_STARTTX* task																																	
			Disabled	0	Disable shortcut																															
			Enabled	1	Enable shortcut																															
F	RW	LASTRX_STOP			Shortcut between *EVENTS_LASTRX* event and *TASKS_STOP* task																																	
			Disabled	0	Disable shortcut																															
			Enabled	1	Enable shortcut																															

31.7.2 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number					31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id												I	H			G	F									D								A	
Reset 0x00000000					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																															
A	RW	STOPPED			Enable or disable interrupt on *EVENTS_STOPPED* event																																	
			Disabled	0	Disable																															
			Enabled	1	Enable																															
D	RW	ERROR			Enable or disable interrupt on *EVENTS_ERROR* event																																	
			Disabled	0	Disable																															
			Enabled	1	Enable																															
F	RW	RXSTARTED			Enable or disable interrupt on *EVENTS_RXSTARTED* event																																	
			Disabled	0	Disable																															
			Enabled	1	Enable																															
G	RW	TXSTARTED			Enable or disable interrupt on *EVENTS_TXSTARTED* event																																	
			Disabled	0	Disable																															
			Enabled	1	Enable																															
H	RW	LASTRX			Enable or disable interrupt on *EVENTS_LASTRX* event																																	
			Disabled	0	Disable																															
			Enabled	1	Enable																															
I	RW	LASTTX			Enable or disable interrupt on *EVENTS_LASTTX* event																																	
			Disabled	0	Disable																															
			Enabled	1	Enable																															

31.7.3 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id											I	H			G	F										D								A	
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																						**Description**									
A	RW	STOPPED																								Write '1' to Enable interrupt on *EVENTS_STOPPED* event									
			Set	1																						Enable									
			Disabled	0																						Read: Disabled									
			Enabled	1																						Read: Enabled									
D	RW	ERROR																								Write '1' to Enable interrupt on *EVENTS_ERROR* event									
			Set	1																						Enable									
			Disabled	0																						Read: Disabled									
			Enabled	1																						Read: Enabled									
F	RW	RXSTARTED																								Write '1' to Enable interrupt on *EVENTS_RXSTARTED* event									
			Set	1																						Enable									
			Disabled	0																						Read: Disabled									
			Enabled	1																						Read: Enabled									
G	RW	TXSTARTED																								Write '1' to Enable interrupt on *EVENTS_TXSTARTED* event									
			Set	1																						Enable									
			Disabled	0																						Read: Disabled									
			Enabled	1																						Read: Enabled									
H	RW	LASTRX																								Write '1' to Enable interrupt on *EVENTS_LASTRX* event									
			Set	1																						Enable									
			Disabled	0																						Read: Disabled									
			Enabled	1																						Read: Enabled									
I	RW	LASTTX																								Write '1' to Enable interrupt on *EVENTS_LASTTX* event									
			Set	1																						Enable									
			Disabled	0																						Read: Disabled									
			Enabled	1																						Read: Enabled									

31.7.4 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id											I	H			G	F										D								A	
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																						**Description**									
A	RW	STOPPED																								Write '1' to Disable interrupt on *EVENTS_STOPPED* event									
			Clear	1																						Disable									
			Disabled	0																						Read: Disabled									
			Enabled	1																						Read: Enabled									
D	RW	ERROR																								Write '1' to Disable interrupt on *EVENTS_ERROR* event									
			Clear	1																						Disable									
			Disabled	0																						Read: Disabled									
			Enabled	1																						Read: Enabled									
F	RW	RXSTARTED																								Write '1' to Disable interrupt on *EVENTS_RXSTARTED* event									
			Clear	1																						Disable									
			Disabled	0																						Read: Disabled									
			Enabled	1																						Read: Enabled									
G	RW	TXSTARTED																								Write '1' to Disable interrupt on *EVENTS_TXSTARTED* event									
			Clear	1																						Disable									
			Disabled	0																						Read: Disabled									
			Enabled	1																						Read: Enabled									
H	RW	LASTRX																								Write '1' to Disable interrupt on *EVENTS_LASTRX* event									
			Clear	1																						Disable									
			Disabled	0																						Read: Disabled									

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id											I	H			G	F										D								A	
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																						**Description**									
			Enabled	1																						Read: Enabled									
I	RW	LASTTX																								Write '1' to Disable interrupt on *EVENTS_LASTTX* event									
			Clear	1																						Disable									
			Disabled	0																						Read: Disabled									
			Enabled	1																						Read: Enabled									

31.7.5 ERRORSRC

Address offset: 0x4C4

Error source

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																	B	A	
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																						**Description**									
A	RW	ANACK																								NACK received after sending the address (write '1' to clear)									
			NotReceived	0																						Error did not occur									
			Received	1																						Error occurred									
B	RW	DNACK																								NACK received after sending a data byte (write '1' to clear)									
			NotReceived	0																						Error did not occur									
			Received	1																						Error occurred									

31.7.6 ENABLE

Address offset: 0x500

Enable TWIM

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																						**Description**									
A	RW	ENABLE																								Enable or disable TWIM									
			Disabled	0																						Disable TWIM									
			Enabled	6																						Enable TWIM									

31.7.7 PSEL.SCL

Address offset: 0x508

Pin select for SCL signal

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				C																										A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																						**Description**									
A	RW	PIN		[0..31]																						Pin number									
C	RW	CONNECT																								Connection									
			Disconnected	1																						Disconnect									
			Connected	0																						Connect									

31.7.8 PSEL.SDA

Address offset: 0x50C

Pin select for SDA signal

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				C																												A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PIN		[0..31]																															
C	RW	CONNECT																																	
			Disconnected	1																															
			Connected	0																															

31.7.9 FREQUENCY

Address offset: 0x524

TWI frequency

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x04000000				**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	FREQUENCY																																	
			K100	0x01980000																															
			K250	0x04000000																															
			K400	0x06400000																															

31.7.10 RXD.PTR

Address offset: 0x534

Data pointer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PTR																																	

31.7.11 RXD.MAXCNT

Address offset: 0x538

Maximum number of buffer words to transfer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	MAXCNT		[1..255]																															

31.7.12 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	AMOUNT																																	
				Number of bytes transferred in the last transaction. In case of NACK error, includes the NACK'ed byte.																																	

31.7.13 RXD.LIST

Address offset: 0x540

EasyDMA list type

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	LIST																																	
			Disabled	0																															
			ArrayList	1																															

31.7.14 TXD.PTR

Address offset: 0x544

Data pointer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PTR																																	

31.7.15 TXD.MAXCNT

Address offset: 0x548

Maximum number of buffer words to transfer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	MAXCNT		[1..255]																															
				Maximum number of buffer words to transfer																															

31.7.16 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	AMOUNT																																	
				Number of bytes transferred in the last transaction. In case of NACK error, includes the NACK'ed byte.																																	

31.7.17 TXD.LIST

Address offset: 0x550

EasyDMA list type

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	LIST																																	
			Disabled	0																															
			ArrayList	1																															

31.7.18 ADDRESS

Address offset: 0x588

Address used in the TWI transfer

Bit number																																
Id																											A	A	A	A	A	A	A
Reset 0x00000000																											**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																											
A	RW	ADDRESS			Address used in the TWI transfer																											

31.8 Electrical Specification

31.8.1 TWIM interface electrical specifications

Symbol	Description	Min.	Typ.	Max.	Units
f_{TWIM}	Bit rates for TWIM[26]	100		400	kbps
$I_{TWIM,100kbps}$	Run current for TWIM, 100 kbps		50		µA
$I_{TWIM,400kbps}$	Run current for TWIM, 400 kbps		50		µA
$t_{TWIM,START,LP}$	Time from STARTRX/STARTTX task to RX/TX active, Low power mode		3		µs
$t_{TWIM,START,CL}$	Time from STARTRX/STARTTX task to RX/TX active, Constant latency mode		1		µs

31.8.2 Two Wire Interface Master (TWIM) timing specifications

Symbol	Description	Min.	Typ.	Max.	Units
$f_{TWIM,SCL,100kbps}$	SCL clock frequency, 100 kbps		100		kHz
$f_{TWIM,SCL,250kbps}$	SCL clock frequency, 250 kbps		250		kHz
$f_{TWIM,SCL,400kbps}$	SCL clock frequency, 400 kbps		400		kHz
t_{TWIM,SU_DAT}	Data setup time before positive edge on SCL – all modes	300			ns
t_{TWIM,HD_DAT}	Data hold time after negative edge on SCL – all modes	300			ns
$t_{TWIM,HD\_STA,100kbps}$	TWIM master hold time for START and repeated START condition, 100 kbps	5200			ns
$t_{TWIM,HD\_STA,250kbps}$	TWIM master hold time for START and repeated START condition, 250kbps				ns
$t_{TWIM,HD\_STA,400kbps}$	TWIM master hold time for START and repeated START condition, 400 kbps	1300			ns
$t_{TWIM,SU\_STO,100kbps}$	TWIM master setup time from SCL high to STOP condition, 100 kbps	5200			ns
$t_{TWIM,SU\_STO,250kbps}$	TWIM master setup time from SCL high to STOP condition, 250 kbps				ns
$t_{TWIM,SU\_STO,400kbps}$	TWIM master setup time from SCL high to STOP condition, 400 kbps	1300			ns
$t_{TWIM,BUF,100kbps}$	TWIM master bus free time between STOP and START conditions, 100 kbps	4700			ns
$t_{TWIM,BUF,250kbps}$	TWIM master bus free time between STOP and START conditions, 250 kbps				ns
$t_{TWIM,BUF,400kbps}$	TWIM master bus free time between STOP and START conditions, 400 kbps	1300			ns

[26] Higher bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see GPIO chapter for more details.

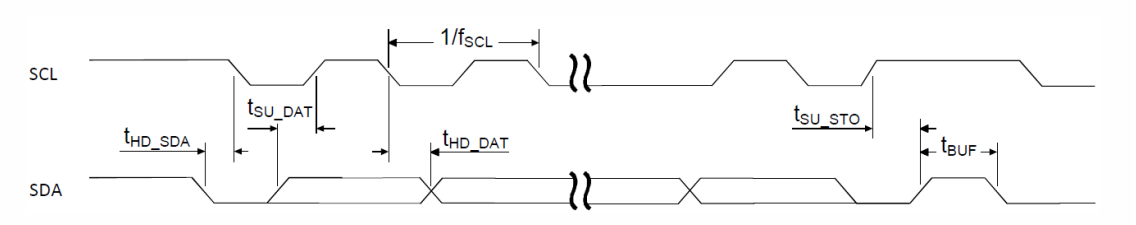

Figure 80: TWIM timing diagram, 1 byte transaction

32 I2C compatible two-wire interface slave with EasyDMA (TWIS)

TWI slave with EasyDMA (TWIS) is compatible with I2C operating at 100 kHz and 400 kHz. The TWI transmitter and receiver implement EasyDMA.

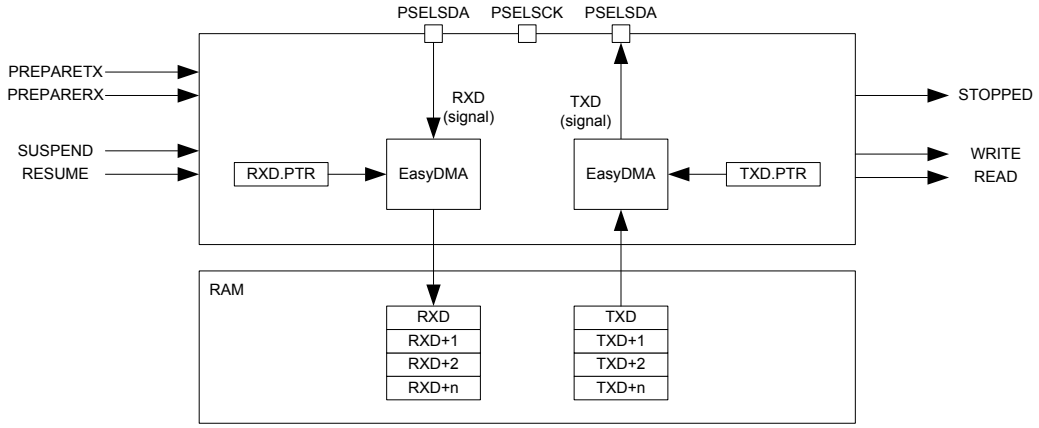

Figure 81: TWI slave with EasyDMA

A typical TWI setup consists of one master and one or more slaves. For an example, see *Figure 82: A typical TWI setup comprising one master and three slaves* on page 306. TWIS is only able to operate with a single master on the TWI bus.

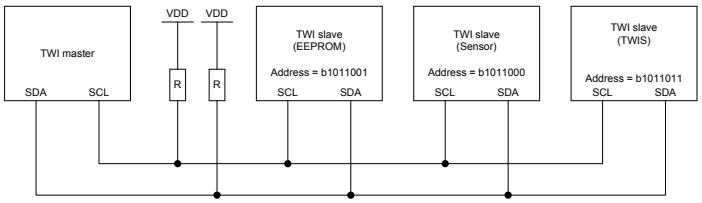

Figure 82: A typical TWI setup comprising one master and three slaves

The TWI slave state machine is illustrated in *Figure 83: TWI slave state machine* on page 307 and *Table 70: TWI slave state machine symbols* on page 307 is explaining the different symbols used in the state machine.

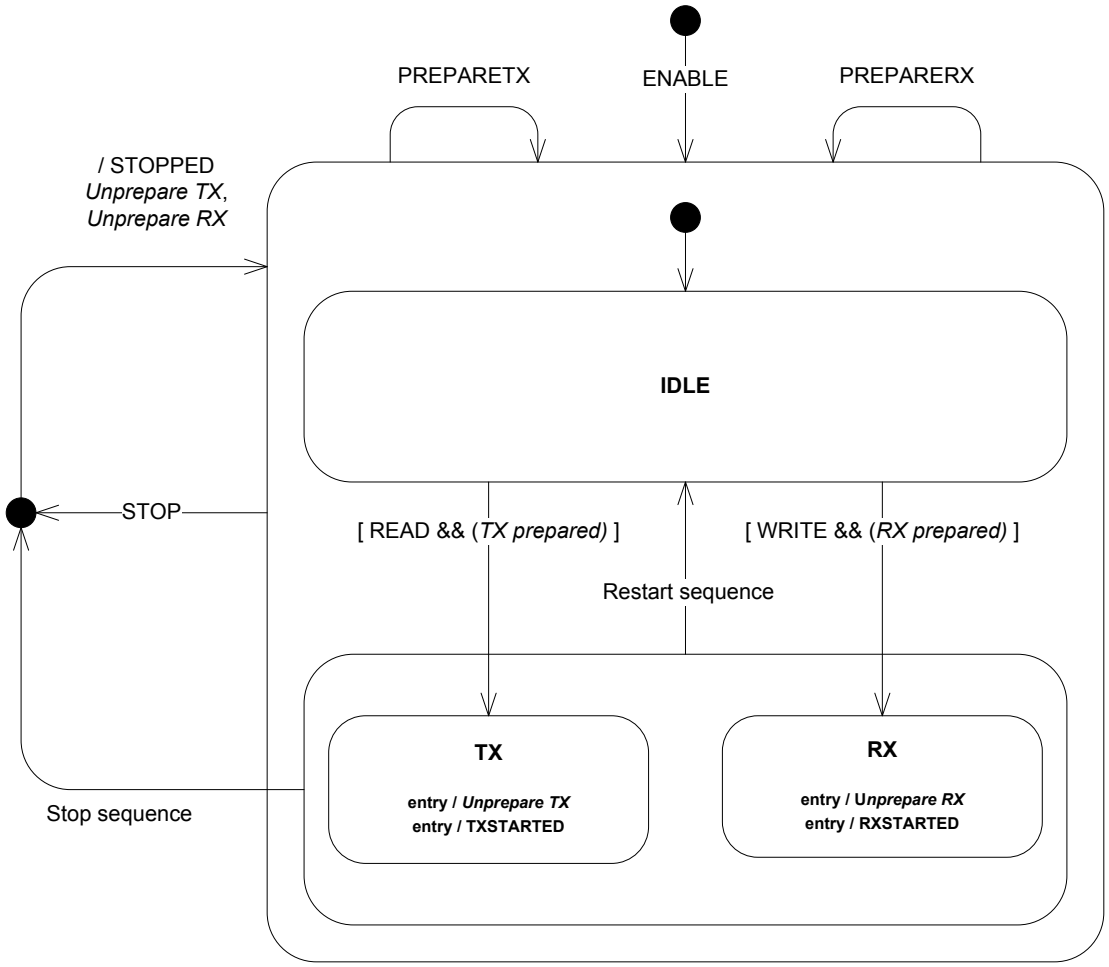

Figure 83: TWI slave state machine

Table 70: TWI slave state machine symbols

Symbol	Type	Description
ENABLE	Register	The TWI slave has been enabled via the *ENABLE* register
PREPARETX	Task	The *TASKS_PREPARETX* task has been triggered
STOP	Task	The *TASKS_STOP* task has been triggered
PREPARERX	Task	The *TASKS_PREPARERX* task has been triggered
STOPPED	Event	The *EVENTS_STOPPED* event was generated
RXSTARTED	Event	The *EVENTS_RXSTARTED* event was generated
TXSTARTED	Event	The *EVENTS_TXSTARTED* event was generated
TX prepared	Internal	Internal flag indicating that a *TASKS_PREPARETX* task has been triggered. This flag is not visible to the user.
RX prepared	Internal	Internal flag indicating that a *TASKS_PREPARERX* task has been triggered. This flag is not visible to the user.
Unprepare TX	Internal	Clears the internal 'TX prepared' flag until next *TASKS_PREPARETX* task.
Unprepare RX	Internal	Clears the internal 'RX prepared' flag until next *TASKS_PREPARERX* task.
Stop sequence	TWI protocol	A TWI stop sequence was detected
Restart sequence	TWI protocol	A TWI restart sequence was detected

The TWI slave supports clock stretching performed by the master.

The TWI slave operates in a low power mode while waiting for a TWI master to initiate a transfer. As long as the TWI slave is not addressed, it will remain in this low power mode.

To secure correct behaviour of the TWI slave, PSEL.SCL, PSEL.SDA, CONFIG and the ADDRESS[n] registers, must be configured prior to enabling the TWI slave through the ENABLE register. Similarly, changing these settings must be performed while the TWI slave is disabled. Failing to do so may result in unpredictable behaviour.

32.1 Slave mode pin configuration

The SCL and SDA signals associated with the TWI slave are mapped to physical pins according to the configuration specified in the PSEL.SCL and PSEL.SDA registers respectively.

The PSEL.SCL and PSEL.SDA registers and their configurations are only used as long as the TWI slave is enabled, and retained only as long as the device is in ON mode. PSEL.SCL and PSEL.SDA must only be configured when the TWI slave is disabled.

To secure correct signal levels on the pins used by the TWI slave when the system is in OFF mode, and when the TWI slave is disabled, these pins must be configured in the GPIO peripheral as described in *Table 71: GPIO configuration* on page 308.

Only one peripheral can be assigned to drive a particular GPIO pin at a time, failing to do so may result in unpredictable behavior.

Table 71: GPIO configuration

TWI slave signal	TWI slave pin	Direction	Drive strength	Output value
SCL	As specified in PSEL.SCL	Input	S0D1	Not applicable
SDA	As specified in PSEL.SDA	Input	S0D1	Not applicable

32.2 Shared resources

The TWI slave shares registers and other resources with other peripherals that have the same ID as the TWI slave.

Therefore, you must disable all peripherals that have the same ID as the TWI slave before the TWI slave can be configured and used. Disabling a peripheral that has the same ID as the TWI slave will not reset any of the registers that are shared with the TWI slave. It is therefore important to configure all relevant registers explicitly to secure that the TWI slave operates correctly.

The Instantiation table in *Instantiation* on page 36 shows which peripherals have the same ID as the TWI slave.

32.3 EasyDMA

The TWI slave implements EasyDMA for reading and writing to and from the RAM.

The STOPPED event indicates that EasyDMA has finished accessing the buffer in RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 34 for more information about the different memory regions.

32.4 TWI slave responding to a read command

Before the TWI slave can respond to a read command the TWI slave must be configured correctly and enabled via the ENABLE register. When enabled the TWI slave will be in its IDLE state where it will consume I_{IDLE} .

A read command is started when the TWI master generates a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 1 (WRITE=0, READ=1). The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) response from the TWI slave.

The TWI slave is able to listen for up to two addresses at the same time. Which addresses to listen for is configured in the ADDRESS registers and the CONFIG register.

The TWI slave will only acknowledge (ACK) the read command if the address presented by the master matches one of the addresses the slave is configured to listen for. The TWI slave will generate a READ event when it acknowledges the read command.

The TWI slave is only able to detect a read command from the IDLE state.

The TWI slave will set an internal 'TX prepared' flag when the PREPARETX task is triggered.

When the read command is received the TWI slave will enter the TX state if the internal 'TX prepared' flag is set.

If the internal 'TX prepared' flag is not set when the read command is received, the TWI slave will stretch the master's clock until the PREPARETX task is triggered and the internal 'TX prepared' flag is set.

The TWI slave will generate the TXSTARTED event and clear the 'TX prepared' flag ('unprepare TX') when it enters the TX state. In this state the TWI slave will send the data bytes found in the transmit buffer to the master using the master's clock. The TWI slave will consume I_{TX} in this mode.

The TWI slave will go back to the IDLE state if the TWI slave receives a restart command when it is in the TX state.

The TWI slave is stopped when it receives the stop condition from the TWI master. A STOPPED event will be generated when the transaction has stopped. The TWI slave will clear the 'TX prepared' flag ('unprepare TX') and go back to the IDLE state when it has stopped.

The transmit buffer is located in RAM at the address specified in the TXD.PTR register. The TWI slave will only be able to send TXD.MAXCNT bytes from the transmit buffer for each transaction. If the TWI master forces the slave to send more than TXD.MAXCNT bytes, the slave will send the byte specified in the ORC register to the master instead. If this happens, an ERROR event will be generated.

The EasyDMA configuration registers, see TXD.PTR etc., are latched when the TXSTARTED event is generated.

The TWI slave can be forced to stop by triggering the STOP task. A STOPPED event will be generated when the TWI slave has stopped. The TWI slave will clear the 'TX prepared' flag and go back to the IDLE state when it has stopped, see also *Terminating an ongoing TWI transaction* on page 311.

Each byte sent from the slave will be followed by an ACK/NACK bit sent from the master. The TWI master will generate a NACK following the last byte that it wants to receive to tell the slave to release the bus so that the TWI master can generate the stop condition. The TXD.AMOUNT register can be queried after a transaction to see how many bytes were sent.

A typical TWI slave read command response is illustrated in *Figure 84: The TWI slave responding to a read command* on page 309. Occurrence 2 in the figure illustrates clock stretching performed by the TWI slave following a SUSPEND task.

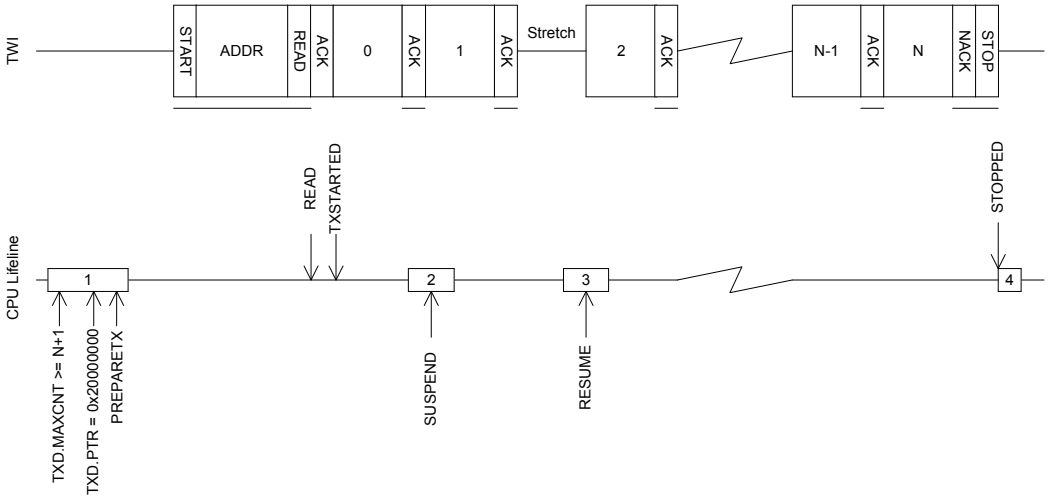

Figure 84: The TWI slave responding to a read command

32.5 TWI slave responding to a write command

Before the TWI slave can respond to a write command the TWI slave must be configured correctly and enabled via the ENABLE register. When enabled the TWI slave will be in its IDLE state where it will consume I_{IDLE}.

A write command is started when the TWI master generates a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 0 (WRITE=0, READ=1). The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) response from the slave.

The TWI slave is able to listen for up to two addresses at the same time. Which addresses to listen for is configured in the ADDRESS registers and the CONFIG register.

The TWI slave will only acknowledge (ACK) the write command if the address presented by the master matches one of the addresses the slave is configured to listen for. The TWI slave will generate a WRITE event if it acknowledges the write command.

The TWI slave is only able to detect a write command from the IDLE state.

The TWI slave will set an internal 'RX prepared' flag when the PREPARERX task is triggered.

When the write command is received the TWI slave will enter the RX state if the internal 'RX prepared' flag is set.

If the internal 'RX prepared' flag is not set when the write command is received, the TWI slave will stretch the master's clock until the PREPARERX task is triggered and the internal 'RX prepared' flag is set.

The TWI slave will generate the RXSTARTED event and clear the internal 'RX prepared' flag ('unprepare RX') when it enters the RX state. In this state the TWI slave will be able to receive the bytes sent by the TWI master. The TWI slave will consume I_{RX} in this mode.

The TWI slave will go back to the IDLE state if the TWI slave receives a restart command when it is in the RX state.

The TWI slave is stopped when it receives the stop condition from the TWI master. A STOPPED event will be generated when the transaction has stopped. The TWI slave will clear the internal 'RX prepared' flag ('unprepare RX') and go back to the IDLE state when it has stopped.

The receive buffer is located in RAM at the address specified in the TXD.PTR register. The TWI slave will only be able to receive as many bytes as specified in the RXD.MAXCNT register. If the TWI master tries to send more bytes to the slave than the slave is able to receive,these bytes will be discarded and the bytes will be NACKed by the slave. If this happens, an ERROR event will be generated.

The EasyDMA configuration registers, see RXD.PTR etc., are latched when the RXSTARTED event is generated.

The TWI slave can be forced to stop by triggering the STOP task. A STOPPED event will be generated when the TWI slave has stopped. The TWI slave will clear the internal 'RX prepared' flag and go back to the IDLE state when it has stopped, see also *Terminating an ongoing TWI transaction* on page 311.

The TWI slave will generate an ACK after every byte received from the master. The RXD.AMOUNT register can be queried after a transaction to see how many bytes were received.

A typical TWI slave write command response is illustrated in *Figure 85: The TWI slave responding to a write command* on page 311. Occurrence 2 in the figure illustrates clock stretching performed by the TWI slave following a SUSPEND task.

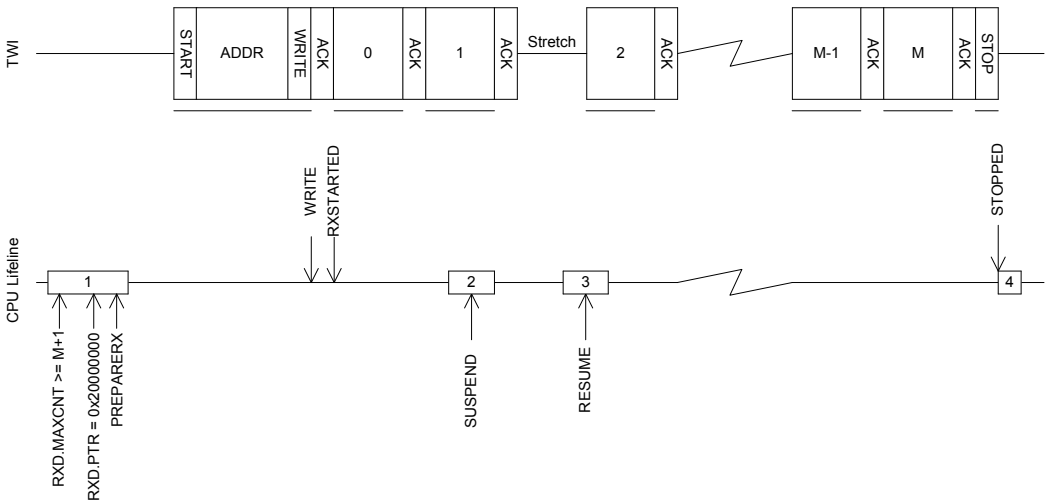

Figure 85: The TWI slave responding to a write command

32.6 Master repeated start sequence

An example of a repeated start sequence is one in which the TWI master writes two bytes to the slave followed by reading four bytes from the slave.

This is illustrated in *Figure 86: A repeated start sequence, where the TWI master writes two bytes followed by reading four bytes from the slave* on page 311.

It is here assumed that the receiver does not know in advance what the master wants to read, and that this information is provided in the first two bytes received in the write part of the repeated start sequence. To guarantee that the CPU is able to process the received data before the TWI slave starts to reply to the read command, the SUSPEND task is triggered via a shortcut from the READ event generated when the read command is received. When the CPU has processed the incoming data and prepared the correct data response, the CPU will resume the transaction by triggering the RESUME task.

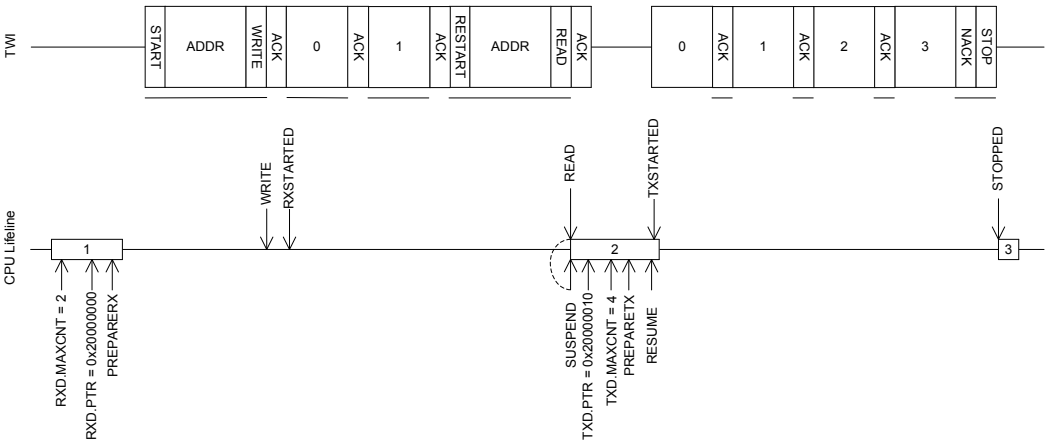

Figure 86: A repeated start sequence, where the TWI master writes two bytes followed by reading four bytes from the slave

32.7 Terminating an ongoing TWI transaction

In some situations, e.g. if the external TWI master is not responding correctly, it may be required to terminate an ongoing transaction.

This can be achieved by triggering the STOP task. In this situation a STOPPED event will be generated when the TWI has stopped independent of whether or not a STOP condition has been generated on the TWI bus. The TWI slave will release the bus when it has stopped and go back to its IDLE state.

32.8 Registers

Table 72: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40003000	TWIS	TWIS0	Two-wire interface slave 0	
0x40004000	TWIS	TWIS1	Two-wire interface slave 1	

Table 73: Register Overview

Register	Offset	Description
TASKS_STOP	0x014	Stop TWI transaction
TASKS_SUSPEND	0x01C	Suspend TWI transaction
TASKS_RESUME	0x020	Resume TWI transaction
TASKS_PREPARERX	0x030	Prepare the TWI slave to respond to a write command
TASKS_PREPARETX	0x034	Prepare the TWI slave to respond to a read command
EVENTS_STOPPED	0x104	TWI stopped
EVENTS_ERROR	0x124	TWI error
EVENTS_RXSTARTED	0x14C	Receive sequence started
EVENTS_TXSTARTED	0x150	Transmit sequence started
EVENTS_WRITE	0x164	Write command received
EVENTS_READ	0x168	Read command received
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x4D0	Error source
MATCH	0x4D4	Status register indicating which address had a match
ENABLE	0x500	Enable TWIS
PSEL.SCL	0x508	Pin select for SCL signal
PSEL.SDA	0x50C	Pin select for SDA signal
RXD.PTR	0x534	RXD Data pointer
RXD.MAXCNT	0x538	Maximum number of bytes in RXD buffer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last RXD transaction
TXD.PTR	0x544	TXD Data pointer
TXD.MAXCNT	0x548	Maximum number of bytes in TXD buffer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last TXD transaction
ADDRESS[0]	0x588	TWI slave address 0
ADDRESS[1]	0x58C	TWI slave address 1
CONFIG	0x594	Configuration register for the address match mechanism
ORC	0x5C0	Over-read character. Character sent out in case of an over-read of the transmit buffer.

32.8.1 SHORTS

Address offset: 0x200

Shortcut register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																					B	A													
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																														
A	RW	WRITE_SUSPEND			Shortcut between *EVENTS_WRITE* event and *TASKS_SUSPEND* task																																
			Disabled	0	Disable shortcut																														

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																					B	A													
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Enabled	1																															
B	RW	READ_SUSPEND																																	
			Disabled	0																															
			Enabled	1																															

32.8.2 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id									H	G					F	E										B							A		
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	STOPPED																																	
			Disabled	0																															
			Enabled	1																															
B	RW	ERROR																																	
			Disabled	0																															
			Enabled	1																															
E	RW	RXSTARTED																																	
			Disabled	0																															
			Enabled	1																															
F	RW	TXSTARTED																																	
			Disabled	0																															
			Enabled	1																															
G	RW	WRITE																																	
			Disabled	0																															
			Enabled	1																															
H	RW	READ																																	
			Disabled	0																															
			Enabled	1																															

32.8.3 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id									H	G					F	E										B							A		
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	STOPPED																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	ERROR																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
E	RW	RXSTARTED																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id									H	G					F	E										B								A	
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																						**Description**									
F	RW	TXSTARTED																								Write '1' to Enable interrupt on *EVENTS_TXSTARTED* event									
			Set	1																						Enable									
			Disabled	0																						Read: Disabled									
			Enabled	1																						Read: Enabled									
G	RW	WRITE																								Write '1' to Enable interrupt on *EVENTS_WRITE* event									
			Set	1																						Enable									
			Disabled	0																						Read: Disabled									
			Enabled	1																						Read: Enabled									
H	RW	READ																								Write '1' to Enable interrupt on *EVENTS_READ* event									
			Set	1																						Enable									
			Disabled	0																						Read: Disabled									
			Enabled	1																						Read: Enabled									

32.8.4 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id									H	G					F	E										B								A	
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																						**Description**									
A	RW	STOPPED																								Write '1' to Disable interrupt on *EVENTS_STOPPED* event									
			Clear	1																						Disable									
			Disabled	0																						Read: Disabled									
			Enabled	1																						Read: Enabled									
B	RW	ERROR																								Write '1' to Disable interrupt on *EVENTS_ERROR* event									
			Clear	1																						Disable									
			Disabled	0																						Read: Disabled									
			Enabled	1																						Read: Enabled									
E	RW	RXSTARTED																								Write '1' to Disable interrupt on *EVENTS_RXSTARTED* event									
			Clear	1																						Disable									
			Disabled	0																						Read: Disabled									
			Enabled	1																						Read: Enabled									
F	RW	TXSTARTED																								Write '1' to Disable interrupt on *EVENTS_TXSTARTED* event									
			Clear	1																						Disable									
			Disabled	0																						Read: Disabled									
			Enabled	1																						Read: Enabled									
G	RW	WRITE																								Write '1' to Disable interrupt on *EVENTS_WRITE* event									
			Clear	1																						Disable									
			Disabled	0																						Read: Disabled									
			Enabled	1																						Read: Enabled									
H	RW	READ																								Write '1' to Disable interrupt on *EVENTS_READ* event									
			Clear	1																						Disable									
			Disabled	0																						Read: Disabled									
			Enabled	1																						Read: Enabled									

32.8.5 ERRORSRC

Address offset: 0x4D0

Error source

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																C	B		A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	OVERFLOW																																	
			NotDetected	0																															
			Detected	1																															
B	RW	DNACK																																	
			NotReceived	0																															
			Received	1																															
C	RW	OVERREAD																																	
			NotDetected	0																															
			Detected	1																															

32.8.6 MATCH

Address offset: 0x4D4

Status register indicating which address had a match

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	MATCH		[0..1]																															
				Which of the addresses in {ADDRESS} matched the incoming address																															

32.8.7 ENABLE

Address offset: 0x500

Enable TWIS

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	ENABLE																																	
			Disabled	0																															
			Enabled	9																															

32.8.8 PSEL.SCL

Address offset: 0x508

Pin select for SCL signal

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				C																											A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PIN		[0..31]																															
				Pin number																															
C	RW	CONNECT																																	
				Connection																															
			Disconnected	1																															
			Connected	0																															
				Connect																															

32.8.9 PSEL.SDA

Address offset: 0x50C

Pin select for SDA signal

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				C																												A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																						**Description**									
A	RW	PIN		[0..31]																						Pin number									
C	RW	CONNECT																								Connection									
			Disconnected	1																						Disconnect									
			Connected	0																						Connect									

32.8.10 RXD.PTR

Address offset: 0x534

RXD Data pointer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																						**Description**									
A	RW	PTR																								RXD Data pointer									

32.8.11 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in RXD buffer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																						**Description**									
A	RW	MAXCNT																								Maximum number of bytes in RXD buffer									

32.8.12 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last RXD transaction

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																						**Description**									
A	R	AMOUNT																								Number of bytes transferred in the last RXD transaction									

32.8.13 TXD.PTR

Address offset: 0x544

TXD Data pointer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																						**Description**									
A	RW	PTR																								TXD Data pointer									

32.8.14 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in TXD buffer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
A	RW	MAXCNT																										Maximum number of bytes in TXD buffer							

32.8.15 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last TXD transaction

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
A	R	AMOUNT																										Number of bytes transferred in the last TXD transaction							

32.8.16 ADDRESS[0]

Address offset: 0x588

TWI slave address 0

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																													A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
A	RW	ADDRESS																										TWI slave address							

32.8.17 ADDRESS[1]

Address offset: 0x58C

TWI slave address 1

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																													A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
A	RW	ADDRESS																										TWI slave address							

32.8.18 CONFIG

Address offset: 0x594

Configuration register for the address match mechanism

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		B	A
Reset 0x00000001				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
A	RW	ADDRESS0																										Enable or disable address matching on ADDRESS[0]							
			Disabled	0																								Disabled							
			Enabled	1																								Enabled							
B	RW	ADDRESS1																										Enable or disable address matching on ADDRESS[1]							
			Disabled	0																								Disabled							
			Enabled	1																								Enabled							

32.8.19 ORC

Address offset: 0x5C0

Over-read character. Character sent out in case of an over-read of the transmit buffer.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																									A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	ORC			Over-read character. Character sent out in case of an over-read of the transmit buffer.

32.9 Electrical Specification

32.9.1 TWIS slave interface electrical specifications

Symbol	Description	Min.	Typ.	Max.	Units
f_{TWIS}	Bit rates for TWIS[27]	100		400	kbps
$I_{TWIS,100kbps}$	Run current for TWIS (Average current to receive and transfer a byte to RAM), 100 kbps		45		µA
$I_{TWIS,400kbps}$	Run current for TWIS (Average current to receive and transfer a byte to RAM), 400 kbps		45		µA
$I_{TWIS,IDLE}$	Idle current for TWIS		1		µA
$t_{TWIS,START,LP}$	Time from STARTRX/STARTTX task to RX/TX active, Low power mode		3		µs
$t_{TWIS,START,CL}$	Time from STARTRX/STARTTX task to RX/TX active, Constant latency mode		1		µs

32.9.2 TWIS slave timing specifications

Symbol	Description	Min.	Typ.	Max.	Units
$f_{TWIS,SCL,100kbps}$	SCL clock frequency, 100 kbps			100	kHz
$f_{TWIS,SCL,250kbps}$	SCL clock frequency, 250 kbps			250	kHz
$f_{TWIS,SCL,400kbps}$	SCL clock frequency, 400 kbps			400	kHz
t_{TWIS,SU_DAT}	Data setup time before positive edge on SCL – all modes	300			ns
t_{TWIS,HD_DAT}	Data hold time after negative edge on SCL – all modes	300			ns
$t_{TWIS,HD\_STA,100kbps}$	TWI slave hold time from for START condition (SDA low to SCL low), 100 kbps	5200			ns
$t_{TWIS,HD\_STA,250kbps}$	TWI slave hold time from for START condition (SDA low to SCL low), 250kbps				ns
$t_{TWIS,HD\_STA,400kbps}$	TWI slave hold time from for START condition (SDA low to SCL low), 400 kbps	1300			ns
$t_{TWIS,SU\_STO,100kbps}$	TWI slave setup time from SCL high to STOP condition, 100 kbps	5200			ns
$t_{TWIS,SU\_STO,250kbps}$	TWI slave setup time from SCL high to STOP condition, 250 kbps				ns
$t_{TWIS,SU\_STO,400kbps}$	TWI slave setup time from SCL high to STOP condition, 400 kbps	1300			ns
$t_{TWIS,BUF,100kbps}$	TWI slave bus free time between STOP and START conditions, 100 kbps		4700		ns
$t_{TWIS,BUF,250kbps}$	TWI slave bus free time between STOP and START conditions, 250 kbps				ns
$t_{TWIS,BUF,400kbps}$	TWI slave bus free time between STOP and START conditions, 400 kbps		1300		ns

[27] Higher bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see GPIO chapter for more details.

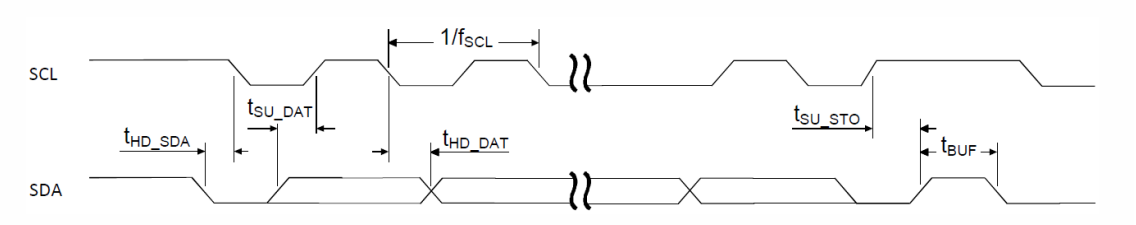

Figure 87: TWIS timing diagram, 1 byte transaction

33 Universal asynchronous receiver/transmitter with EasyDMA (UARTE)

The Universal asynchronous receiver/transmitter (UART) offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS) support in hardware at a rate up to 1 Mbps. The UARTE is supported by EasyDMA.

Listed here are the main features for UARTE:

- Full-duplex operation
- Automatic hardware flow control
- Parity checking and generation for the 9th data bit
- EasyDMA
- Up to 1 Mbps baudrate
- Return to IDLE between transactions supported (when using HW flow control)
- Least significant bit (LSB) first

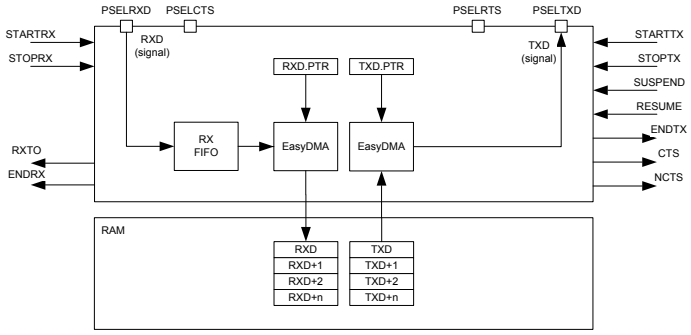

Figure 88: UARTE configuration

The GPIOs used for each UART interface can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of board space and signal routing.

33.1 Pin configuration

The different signals RXD, CTS (Clear To Send, active low), RTS (Request To Send, active low), and TXD associated with the UARTE are mapped to physical pins according to the configuration specified in the PSEL.RXD, PSEL.CTS, PSEL.RTS, and PSEL.TXD registers respectively.

The PSEL.RXD, PSEL.CTS, PSEL.RTS, and PSEL.TXD registers and their configurations are only used as long as the UARTE is enabled, and retained only for the duration the device is in ON mode. PSEL.RXD, PSEL.RTS, PSEL.RTS and PSEL.TXD must only be configured when the UARTE is disabled.

To secure correct signal levels on the pins by the UARTE when the system is in OFF mode, the pins must be configured in the GPIO peripheral as described in *Table 74: GPIO configuration* on page 320.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 74: GPIO configuration

UARTE pin	Direction	Output value
RXD	Input	Not applicable
CTS	Input	Not applicable
RTS	Output	1

UARTE pin	Direction	Output value
TXD	Output	1

33.2 Shared resources

The UARTE shares registers and other resources with other peripherals that have the same ID as the UARTE.

Therefore, you must disable all peripherals that have the same ID as the UARTE before the UARTE can be configured and used. Disabling a peripheral that has the same ID as the UARTE will not reset any of the registers that are shared with the UARTE. It is therefore important to configure all relevant UARTE registers explicitly to ensure that it operates correctly.

See the Instantiation table in *Instantiation* on page 36 for details on peripherals and their IDs.

33.3 EasyDMA

The UARTE implements EasyDMA for reading and writing to and from the RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 34 for more information about the different memory regions.

The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next RX/TX transmission immediately after having received the RXSTARTED/TXSTARTED event.

The ENDRX/ENDTX event indicates that EasyDMA has finished accessing respectively the RX/TX buffer in RAM.

33.4 Transmission

The first step of a DMA transmission is storing bytes in the transmit buffer and configuring EasyDMA. This is achieved by writing the initial address pointer to TXD.PTR, and the number of bytes in the RAM buffer to TXD.MAXCNT. The UARTE transmission is started by triggering the STARTTX task.

When all bytes in the TXD buffer, as specified in the TXD.MAXCNT register, have been transmitted, the UARTE transmission will end automatically and an ENDTX event will be generated.

A UARTE transmission sequence is stopped by triggering the STOPTX task, a TXSTOPPED event will be generated when the UARTE transmitter has stopped.

If the ENDTX event has not already been generated when the UARTE transmitter has come to a stop, the UARTE will generate the ENDTX event explicitly even though all bytes in the TXD buffer, as specified in the TXD.MAXCNT register, have not been transmitted.

If flow control is enabled, a transmission will be automatically suspended when CTS is deactivated and resumed when CTS is activated again, as illustrated in *Figure 89: UARTE transmission* on page 322.
A byte that is in transmission when CTS is deactivated will be fully transmitted before the transmission is suspended.

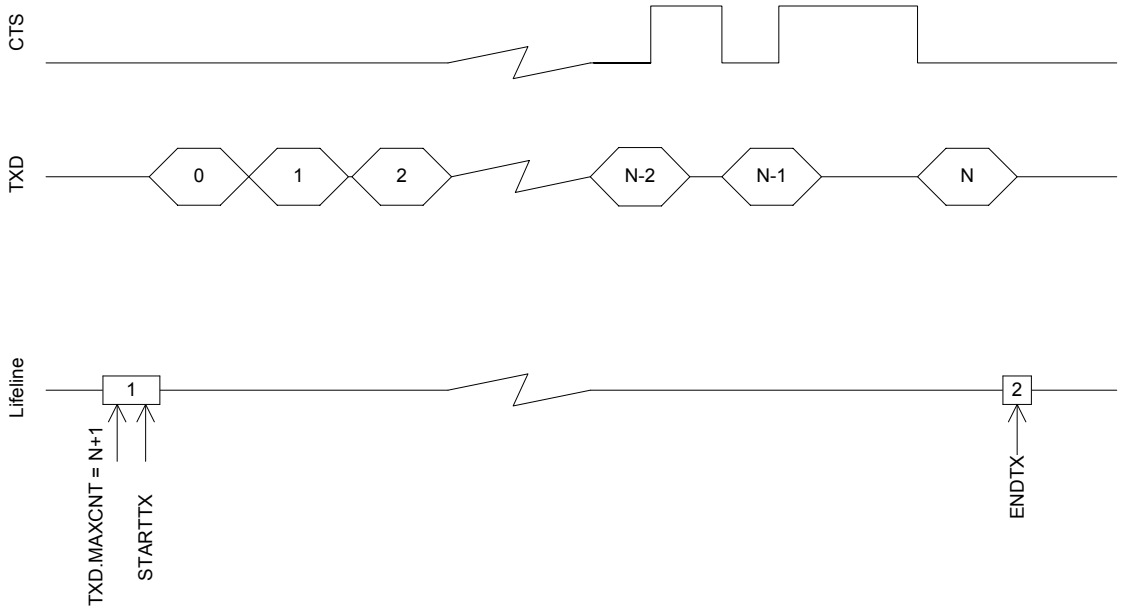

Figure 89: UARTE transmission

The UARTE transmitter will be in its lowest activity level, and consume the least amount of energy, when it is stopped, i.e. before it is started via STARTTX or after it has been stopped via STOPTX and the TXSTOPPED event has been generated. See *Power management (POWER)* on page 79 for more information about power modes.

33.5 Reception

The UARTE receiver is started by triggering the STARTRX task. The UARTE receiver is using EasyDMA to store incoming data in an RX buffer in RAM.

The RX buffer is located at the address specified in the RXD.PTR register. The RXD.PTR register is double-buffered and it can be updated and prepared for the next STARTRX task immediately after the RXSTARTED event is generated. The size of the RX buffer is specified in the RXD.MAXCNT register and the UARTE will generate an ENDRX event when it has filled up the RX buffer, see *Figure 90: UARTE reception* on page 323.

The RXD.AMOUNT register can be queried following an ENDRX event to see how many new bytes have been transferred to the RX buffer in RAM since the previous ENDRX event.

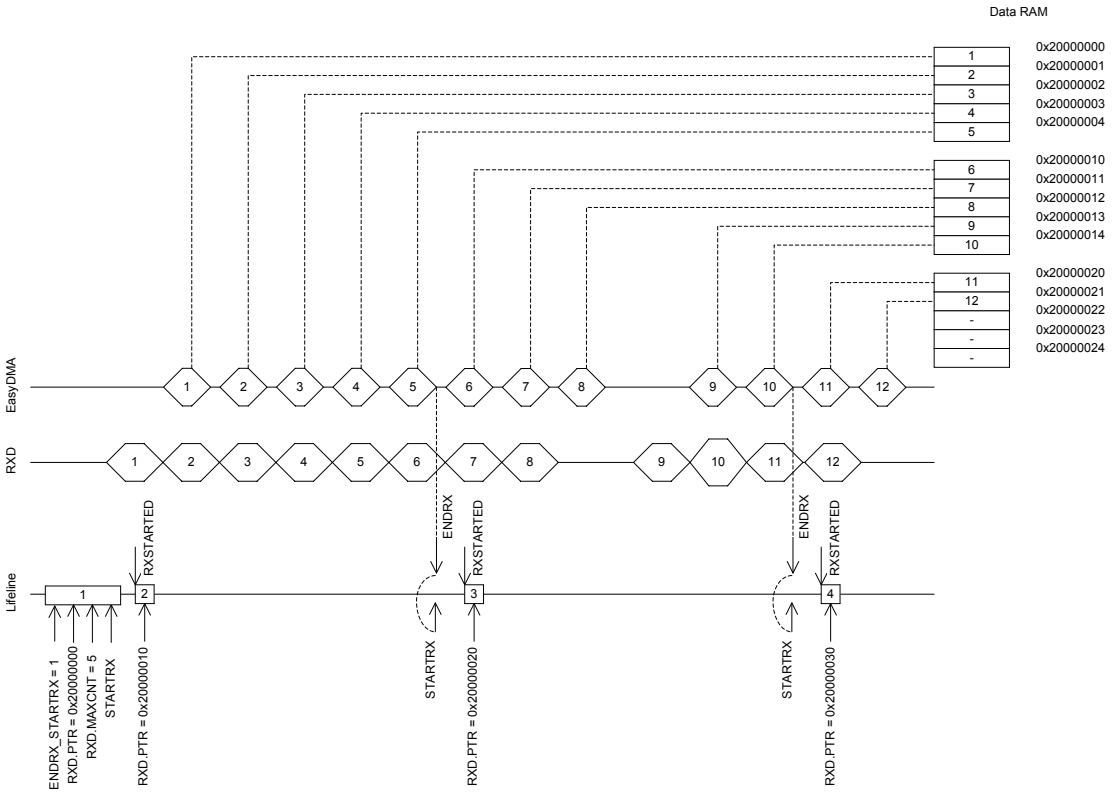

Figure 90: UARTE reception

The UARTE receiver is stopped by triggering the STOPRX task. An RXTO event is generated when the UARTE has stopped. The UARTE will make sure that an impending ENDRX event will be generated before the RXTO event is generated. This means that the UARTE will guarantee that no ENDRX event will be generated after RXTO, unless the UARTE is restarted or a FLUSHRX command is issued after the RXTO event is generated.

> **Important:** If the ENDRX event has not already been generated when the UARTE receiver has come to a stop, which implies that all pending content in the RX FIFO has been moved to the RX buffer, the UARTE will generate the ENDRX event explicitly even though the RX buffer is not full. In this scenario the ENDRX event will be generated before the RXTO event is generated.

To be able to know how many bytes have actually been received into the RX buffer, the CPU can query the RXD.AMOUNT register following the ENDRX event or the RXTO event.

The UARTE is able to receive up to four bytes after the STOPRX task has been triggered as long as these are sent in succession immediately after the RTS signal is deactivated. This is possible because after the RTS is deactivated the UARTE is able to receive bytes for an extended period equal to the time it takes to send 4 bytes on the configured baud rate.

After the RXTO event is generated the internal RX FIFO may still contain data, and to move this data to RAM the FLUSHRX task must be triggered. To make sure that this data does not overwrite data in the RX buffer, the RX buffer should be emptied or the RXD.PTR should be updated before the FLUSHRX task is triggered. To make sure that all data in the RX FIFO is moved to the RX buffer, the RXD.MAXCNT register must be set to RXD.MAXCNT > 4, see *Figure 91: UARTE reception with forced stop via STOPRX* on page 324. The UARTE will generate the ENDRX event after completing the FLUSHRX task even if the RX FIFO was empty or if the RX buffer does not get filled up. To be able to know how many bytes have actually been received into the RX buffer in this case, the CPU can query the RXD.AMOUNT register following the ENDRX event.

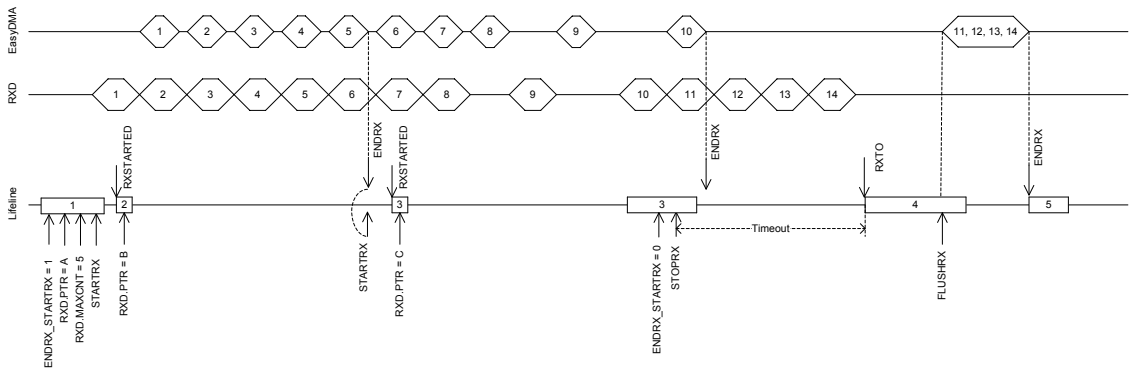

Figure 91: UARTE reception with forced stop via STOPRX

If HW flow control is enabled the RTS signal will be deactivated when the receiver is stopped via the STOPRX task or when the UARTE is only able to receive four more bytes in its internal RX FIFO.

With flow control disabled, the UARTE will function in the same way as when the flow control is enabled except that the RTS line will not be used. This means that no signal will be generated when the UARTE has reached the point where it is only able to receive four more bytes in its internal RX FIFO. Data received when the internal RX FIFO is filled up, will be lost.

The UARTE receiver will be in its lowest activity level, and consume the least amount of energy, when it is stopped, i.e. before it is started via STARTRX or after it has been stopped via STOPRX and the RXTO event has been generated. See *Power management (POWER)* on page 79 for more information about power modes.

33.6 Error conditions

An ERROR event, in the form of a framing error, will be generated if a valid stop bit is not detected in a frame. Another ERROR event, in the form of a break condition, will be generated if the RXD line is held active low for longer than the length of a data frame. Effectively, a framing error is always generated before a break condition occurs.

An ERROR event will not stop reception. If the error was a parity error, the received byte will still be transferred into Data RAM, and so will following incoming bytes. If there was a framing error (wrong stop bit), that specific byte will NOT be stored into Data RAM, but following incoming bytes will.

33.7 Using the UARTE without flow control

If flow control is not enabled, the interface will behave as if the CTS and RTS lines are kept active all the time.

33.8 Parity configuration

When parity is enabled, the parity will be generated automatically from the even parity of TXD and RXD for transmission and reception respectively.

33.9 Registers

Table 75: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40002000	UARTE	UARTE0	Universal Asynchronous Receiver/ Transmitter with EasyDMA	

Table 76: Register Overview

Register	Offset	Description
TASKS_STARTRX	0x000	Start UART receiver
TASKS_STOPRX	0x004	Stop UART receiver
TASKS_STARTTX	0x008	Start UART transmitter
TASKS_STOPTX	0x00C	Stop UART transmitter
TASKS_FLUSHRX	0x02C	Flush RX FIFO into RX buffer
EVENTS_CTS	0x100	CTS is activated (set low). Clear To Send.
EVENTS_NCTS	0x104	CTS is deactivated (set high). Not Clear To Send.
EVENTS_ENDRX	0x110	Receive buffer is filled up
EVENTS_ENDTX	0x120	Last TX byte transmitted
EVENTS_ERROR	0x124	Error detected
EVENTS_RXTO	0x144	Receiver timeout
EVENTS_RXSTARTED	0x14C	UART receiver has started
EVENTS_TXSTARTED	0x150	UART transmitter has started
EVENTS_TXSTOPPED	0x158	Transmitter stopped
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x480	Error source
ENABLE	0x500	Enable UART
PSEL.RTS	0x508	Pin select for RTS signal
PSEL.TXD	0x50C	Pin select for TXD signal
PSEL.CTS	0x510	Pin select for CTS signal
PSEL.RXD	0x514	Pin select for RXD signal
BAUDRATE	0x524	Baud rate
RXD.PTR	0x534	Data pointer
RXD.MAXCNT	0x538	Maximum number of bytes in buffer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last transaction
TXD.PTR	0x544	Data pointer
TXD.MAXCNT	0x548	Maximum number of bytes in buffer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last transaction
CONFIG	0x56C	Configuration of parity and hardware flow control

33.9.1 SHORTS

Address offset: 0x200

Shortcut register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																													D	C					
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																														
C	RW	ENDRX_STARTRX			Shortcut between *EVENTS_ENDRX* event and *TASKS_STARTRX* task																																
			Disabled	0	Disable shortcut																														
			Enabled	1	Enable shortcut																														
D	RW	ENDRX_STOPRX			Shortcut between *EVENTS_ENDRX* event and *TASKS_STOPRX* task																																
			Disabled	0	Disable shortcut																														
			Enabled	1	Enable shortcut																														

33.9.2 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id													J		H	G		F								E	D				C			B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	CTS																																	
			Disabled	0																															
			Enabled	1																															
B	RW	NCTS																																	
			Disabled	0																															
			Enabled	1																															
C	RW	ENDRX																																	
			Disabled	0																															
			Enabled	1																															
D	RW	ENDTX																																	
			Disabled	0																															
			Enabled	1																															
E	RW	ERROR																																	
			Disabled	0																															
			Enabled	1																															
F	RW	RXTO																																	
			Disabled	0																															
			Enabled	1																															
G	RW	RXSTARTED																																	
			Disabled	0																															
			Enabled	1																															
H	RW	TXSTARTED																																	
			Disabled	0																															
			Enabled	1																															
J	RW	TXSTOPPED																																	
			Disabled	0																															
			Enabled	1																															

33.9.3 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id													J		H	G		F								E	D				C			B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	CTS																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	NCTS																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	ENDRX																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
D	RW	ENDTX																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
E	RW	ERROR																																	
			Set	1																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id													J		H	G		F								E	D				C			B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Disabled	0																															
			Enabled	1																															
F	RW	RXTO																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
G	RW	RXSTARTED																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
H	RW	TXSTARTED																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
J	RW	TXSTOPPED																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															

33.9.4 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id													J		H	G		F								E	D				C			B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	CTS																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	NCTS																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	ENDRX																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
D	RW	ENDTX																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
E	RW	ERROR																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
F	RW	RXTO																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
G	RW	RXSTARTED																																	
			Clear	1																															
			Disabled	0																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id													J		H	G		F								E	D				C			B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Enabled	1																															
H	RW	TXSTARTED																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
J	RW	TXSTOPPED																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															

33.9.5 ERRORSRC

Address offset: 0x480

Error source

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	OVERRUN																																	
				A start bit is received while the previous data still lies in RXD. (Previous data is lost.)																																	
			NotPresent	0																															
			Present	1																															
B	RW	PARITY																																	
				A character with bad parity is received, if HW parity check is enabled.																																	
			NotPresent	0																															
			Present	1																															
C	RW	FRAMING																																	
				A valid stop bit is not detected on the serial data input after all bits in a character have been received.																																	
			NotPresent	0																															
			Present	1																															
D	RW	BREAK																																	
				The serial data input is '0' for longer than the length of a data frame. (The data frame length is 10 bits without parity bit, and 11 bits with parity bit.).																																	
			NotPresent	0																															
			Present	1																															

33.9.6 ENABLE

Address offset: 0x500

Enable UART

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	ENABLE																																	
			Disabled	0																															
			Enabled	8																															

33.9.7 PSEL.RTS

Address offset: 0x508

Pin select for RTS signal

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				C																											A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PIN		[0..31]																															
C	RW	CONNECT																																	
			Disconnected	1																															
			Connected	0																															

33.9.8 PSEL.TXD

Address offset: 0x50C

Pin select for TXD signal

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				C																											A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PIN		[0..31]																															
C	RW	CONNECT																																	
			Disconnected	1																															
			Connected	0																															

33.9.9 PSEL.CTS

Address offset: 0x510

Pin select for CTS signal

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				C																											A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PIN		[0..31]																															
C	RW	CONNECT																																	
			Disconnected	1																															
			Connected	0																															

33.9.10 PSEL.RXD

Address offset: 0x514

Pin select for RXD signal

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				C																											A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PIN		[0..31]																															
C	RW	CONNECT																																	
			Disconnected	1																															
			Connected	0																															

33.9.11 BAUDRATE

Address offset: 0x524

Baud rate

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x04000000			**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	RW	BAUDRATE																									Baud-rate							
			Baud1200								0x0004F000																1200 baud (actual rate: 1205)							
			Baud2400								0x0009D000																2400 baud (actual rate: 2396)							
			Baud4800								0x0013B000																4800 baud (actual rate: 4808)							
			Baud9600								0x00275000																9600 baud (actual rate: 9598)							
			Baud14400								0x003AF000																14400 baud (actual rate: 14401)							
			Baud19200								0x004EA000																19200 baud (actual rate: 19208)							
			Baud28800								0x0075C000																28800 baud (actual rate: 28777)							
			Baud38400								0x009D0000																38400 baud (actual rate: 38369)							
			Baud57600								0x00EB0000																57600 baud (actual rate: 57554)							
			Baud76800								0x013A9000																76800 baud (actual rate: 76923)							
			Baud115200								0x01D60000																115200 baud (actual rate: 115108)							
			Baud230400								0x03B00000																230400 baud (actual rate: 231884)							
			Baud250000								0x04000000																250000 baud							
			Baud460800								0x07400000																460800 baud (actual rate: 457143)							
			Baud921600								0x0F000000																921600 baud (actual rate: 941176)							
			Baud1M								0x10000000																1Mega baud							

33.9.12 RXD.PTR

Address offset: 0x534

Data pointer

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	RW	PTR																									Data pointer							

33.9.13 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in buffer

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																											A	A	A	A	A	A	A	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	RW	MAXCNT																									Maximum number of bytes in buffer							

33.9.14 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																											A	A	A	A	A	A	A	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	R	AMOUNT																									Number of bytes transferred in the last transaction							

33.9.15 TXD.PTR

Address offset: 0x544

Data pointer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PTR																																	
				Data pointer																															

33.9.16 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in buffer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	MAXCNT																																	
				Maximum number of bytes in buffer																															

33.9.17 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	AMOUNT																																	
				Number of bytes transferred in the last transaction																															

33.9.18 CONFIG

Address offset: 0x56C

Configuration of parity and hardware flow control

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																B	B	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	HWFC																																	
			Disabled	0																															
			Enabled	1																															
B	RW	PARITY																																	
			Excluded	0x0																															
			Included	0x7																															

33.10 Electrical Specification

33.10.1 UARTE electrical specification

Symbol	Description	Min.	Typ.	Max.	Units
f_{UARTE}	Baud rate for UARTE[28].			1000	kbps
$I_{UARTE1M}$	Run current at max baud rate.		55		µA
$I_{UARTE115k}$	Run current at 115200 bps.		55		µA
$I_{UARTE1k2}$	Run current at 1200 bps.		55		µA
$I_{UARTE,IDLE}$	Idle current for UARTE (STARTed, no XXX activity)		1		µA
$t_{UARTE,CTSH}$	CTS high time	1			µs

[28] Higher baud rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

Symbol	Description	Min.	Typ.	Max.	Units
$t_{UARTE,START,LP}$	Time from STARTRX/STARTTX task to RX/TX active, low power mode		3		µs
$t_{UARTE,START,CL}$	Time from STARTRX/STARTTX task to RX/TX active, constant latency mode		1		µs

34 Quadrature decoder (QDEC)

The Quadrature decoder (QDEC) provides buffered decoding of quadrature-encoded sensor signals. It is suitable for mechanical and optical sensors.

The sample period and accumulation are configurable to match application requirements. The QDEC provides the following:

- Decoding of digital waveform from off-chip quadrature encoder.
- Sample accumulation eliminating hard real-time requirements to be enforced on application.
- Optional input de-bounce filters.
- Optional LED output signal for optical encoders.

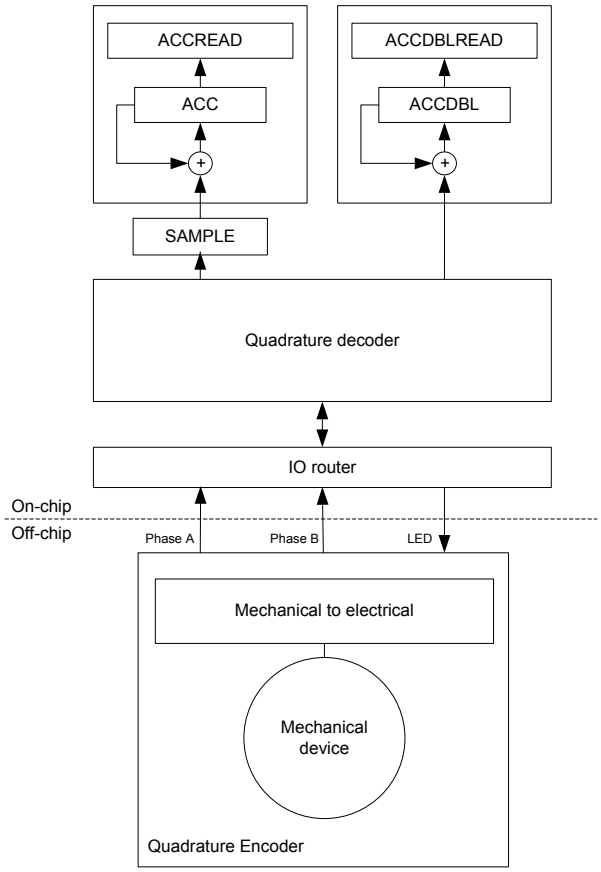

Figure 92: Quadrature decoder configuration

34.1 Sampling and decoding

The QDEC decodes the output from an incremental motion encoder by sampling the QDEC phase input pins (A and B).

The off-chip quadrature encoder is an incremental motion encoder outputting two waveforms, phase A and phase B. The two output waveforms are always 90 degrees out of phase, meaning that one always changes level before the other. The direction of movement is indicated by which of these two waveforms that changes level first. Invalid transitions may occur, that is when the two waveforms switch simultaneously. This may occur if the wheel rotates too fast relative to the sample rate set for the decoder.

The QDEC decodes the output from the off-chip encoder by sampling the QDEC phase input pins (A and B) at a fixed rate as specified in the SAMPLEPER register.

If the SAMPLEPER value needs to be changed, the QDEC shall be stopped using the STOP task. SAMPLEPER can be then changed upon receiving the STOPPED event, and QDEC can be restarted using the START task. Failing to do so may result in unpredictable behaviour.

When started, the decoder continuously samples the two input waveforms and decodes these by comparing the current sample pair (n) with the previous sample pair (n-1).

The decoding of the sample pairs is described in the table below.

Table 77: Sampled value encoding

Previous sample pair(n - 1)		Current samples pair(n)		SAMPLE register	ACC operation	ACCDBL operation	Description
A	B	A	B				
0	0	0	0	0	No change	No change	No movement
0	0	0	1	1	Increment	No change	Movement in positive direction
0	0	1	0	-1	Decrement	No change	Movement in negative direction
0	0	1	1	2	No change	Increment	Error: Double transition
0	1	0	0	-1	Decrement	No change	Movement in negative direction
0	1	0	1	0	No change	No change	No movement
0	1	1	0	2	No change	Increment	Error: Double transition
0	1	1	1	1	Increment	No change	Movement in positive direction
1	0	0	0	1	Increment	No change	Movement in positive direction
1	0	0	1	2	No change	Increment	Error: Double transition
1	0	1	0	0	No change	No change	No movement
1	0	1	1	-1	Decrement	No change	Movement in negative direction
1	1	0	0	2	No change	Increment	Error: Double transition
1	1	0	1	-1	Decrement	No change	Movement in negative direction
1	1	1	0	1	Increment	No change	Movement in positive direction
1	1	1	1	0	No change	No change	No movement

34.2 LED output

The LED output follows the sample period, and the LED is switched on a given period prior to sampling and switched off immediately after the inputs are sampled. The period the LED is switched on prior to sampling is given in the LEDPRE register.

The LED output pin polarity is specified in the LEDPOL register.

For using off-chip mechanical encoders not requiring a LED, the LED output can be disabled by writing value 'Disconnected' to the CONNECT field of the PSEL.LED register. In this case the QDEC will not acquire access to a LED output pin and the pin can be used for other purposes by the CPU.

34.3 Pin configuration

The different signals: Phase A, Phase B, and LED, are mapped to physical pins according to the configuration specified in the PSEL.A, PSEL.B, and PSEL.LED registers respectively.

If the CONNECT field value 'Disconnected' is specified in any of these registers, the associated signal will not be connected to any physical pin. The PSEL.A, PSEL.B, and PSEL.LED registers and their configurations are only used as long as the QDEC is enabled, and retained only as long as the device is in ON mode.

To secure correct behavior in the QDEC, the pins used by the QDEC must be configured in the GPIO peripheral as described in *Table 78: GPIO configuration* on page 334 prior to enabling the QDEC. This configuration must be retained in the GPIO for the selected IOs as long as the QDEC is enabled.

Only one peripheral can be assigned to drive a particular GPIO pin at a time, failing to do so may result in unpredictable behavior.

Table 78: GPIO configuration

QDEC signal	QDEC pin	Direction	Output value
Phase A	As specified in PSEL.A	Input	Not applicable

QDEC signal	QDEC pin	Direction	Output value
Phase B	As specified in PSEL.B	Input	Not applicable
LED	As specified in PSEL.LED	Input	Not applicable

34.4 Debounce filters

Each of the two phase inputs have digital debounce filters.

When enabled through the DBFEN register, the filter inputs are sampled at a fixed 1 MHz frequency during the entire sample period (which is specified in the SAMPLEPER register), and the filters require all of the samples within this sample period to equal before the input signal is accepted and transferred to the output of the filter.

As a result, only input signal with a steady state longer than twice the period specified in SAMPLEPER are guaranteed to pass through the filter, and any signal with a steady state shorter than SAMPLEPER will always be suppressed by the filter. (This is assumed that the frequency during the debounce period never exceeds 500 kHz (as required by the Nyquist theorem when using a 1 MHz sample frequency).

The LED will always be ON when the debounce filters are enabled, as the inputs in this case will be sampled continuously.

34.5 Accumulators

The quadrature decoder contains two accumulator registers, ACC and ACCDBL, that accumulate respectively valid motion sample values and the number of detected invalid samples (double transitions).

The ACC register will accumulate all valid values (1/-1) written to the SAMPLE register. This can be useful for preventing hard real-time requirements from being enforced on the application. When using the ACC register the application does not need to read every single sample from the SAMPLE register, but can instead fetch the ACC register whenever it fits the application. The ACC register will always hold the relative movement of the external mechanical device since the previous clearing of the ACC register. Sample values indicating a double transition (2) will not be accumulated in the ACC register.

An ACCOF event will be generated if the ACC receives a SAMPLE value that would cause the register to overflow or underflow. Any SAMPLE value that would cause an ACC overflow or underflow will be discarded, but any samples not causing the ACC to overflow or underflow will still be accepted.

The accumulator ACCDBL accumulates the number of detected double transitions since the previous clearing of the ACCDBL register.

The ACC and ACCDBL registers can be cleared by the READCLRACC and subsequently read using the ACCREAD and ACCDBLREAD registers.

The ACC register can be separately cleared by the RDCLRACC and subsequently read using the ACCREAD registers.

The ACCDBL register can be separately cleared by the RDCLRDBL and subsequently read using the ACCDBLREAD registers.

The REPORTPER register allows automating the capture of several samples before it can send out a REPORTRDY event in case a non-null displacement has been captured and accumulated, and a DBLRDY event in case one or more double-displacements have been captured and accumulated. The REPORTPER field in this register selects after how many samples the accumulators contents are evaluated to send (or not) REPORTRDY and DBLRDY events.

Using the RDCLRACC task (manually sent upon receiving the event, or using the DBLRDY_RDCLRACC shortcut), ACCREAD can then be read.

In case at least one double transition has been captured and accumulated, a DBLRDY event is sent. Using the RDCLRDBL task (manually sent upon receiving the event, or using the DBLRDY_RDCLRDBL shortcut), ACCDBLREAD can then be read.

34.6 Output/input pins

The QDEC uses a three-pin interface to the off-chip quadrature encoder.

These pins will be acquired when the QDEC is enabled in the ENABLE register. The pins acquired by the QDEC cannot be written by the CPU, but they can still be read by the CPU.

The pin numbers to be used for the QDEC are selected using the PSEL.n registers.

34.7 Registers

Table 79: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40012000	QDEC	QDEC	Quadrature decoder	

Table 80: Register Overview

Register	Offset	Description
TASKS_START	0x000	Task starting the quadrature decoder
TASKS_STOP	0x004	Task stopping the quadrature decoder
TASKS_READCLRACC	0x008	Read and clear ACC and ACCDBL
TASKS_RDCLRACC	0x00C	Read and clear ACC
TASKS_RDCLRDBL	0x010	Read and clear ACCDBL
EVENTS_SAMPLERDY	0x100	Event being generated for every new sample value written to the SAMPLE register
EVENTS_REPORTRDY	0x104	Non-null report ready
EVENTS_ACCOF	0x108	ACC or ACCDBL register overflow
EVENTS_DBLRDY	0x10C	Double displacement(s) detected
EVENTS_STOPPED	0x110	QDEC has been stopped
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	Enable the quadrature decoder
LEDPOL	0x504	LED output pin polarity
SAMPLEPER	0x508	Sample period
SAMPLE	0x50C	Motion sample value
REPORTPER	0x510	Number of samples to be taken before REPORTRDY and DBLRDY events can be generated
ACC	0x514	Register accumulating the valid transitions
ACCREAD	0x518	Snapshot of the ACC register, updated by the READCLRACC or RDCLRACC task
PSEL.LED	0x51C	Pin select for LED signal
PSEL.A	0x520	Pin select for A signal
PSEL.B	0x524	Pin select for B signal
DBFEN	0x528	Enable input debounce filters
LEDPRE	0x540	Time period the LED is switched ON prior to sampling
ACCDBL	0x544	Register accumulating the number of detected double transitions
ACCDBLREAD	0x548	Snapshot of the ACCDBL, updated by the READCLRACC or RDCLRDBL task

34.7.1 SHORTS

Address offset: 0x200

Shortcut register

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																										G	F	E	D	C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	REPORTRDY_READCLRACC			Shortcut between *EVENTS_REPORTRDY* event and *TASKS_READCLRACC* task

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																													G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																									**Description**						
			Disabled	0																									Disable shortcut						
			Enabled	1																									Enable shortcut						
B	RW	SAMPLERDY_STOP																											Shortcut between *EVENTS_SAMPLERDY* event and *TASKS_STOP* task						
			Disabled	0																									Disable shortcut						
			Enabled	1																									Enable shortcut						
C	RW	REPORTRDY_RDCLRACC																											Shortcut between *EVENTS_REPORTRDY* event and *TASKS_RDCLRACC* task						
			Disabled	0																									Disable shortcut						
			Enabled	1																									Enable shortcut						
D	RW	REPORTRDY_STOP																											Shortcut between *EVENTS_REPORTRDY* event and *TASKS_STOP* task						
			Disabled	0																									Disable shortcut						
			Enabled	1																									Enable shortcut						
E	RW	DBLRDY_RDCLRDBL																											Shortcut between *EVENTS_DBLRDY* event and *TASKS_RDCLRDBL* task						
			Disabled	0																									Disable shortcut						
			Enabled	1																									Enable shortcut						
F	RW	DBLRDY_STOP																											Shortcut between *EVENTS_DBLRDY* event and *TASKS_STOP* task						
			Disabled	0																									Disable shortcut						
			Enabled	1																									Enable shortcut						
G	RW	SAMPLERDY_READCLRACC																											Shortcut between *EVENTS_SAMPLERDY* event and *TASKS_READCLRACC* task						
			Disabled	0																									Disable shortcut						
			Enabled	1																									Enable shortcut						

34.7.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																									**Description**						
A	RW	SAMPLERDY																											Write '1' to Enable interrupt on *EVENTS_SAMPLERDY* event						
			Set	1																									Enable						
			Disabled	0																									Read: Disabled						
			Enabled	1																									Read: Enabled						
B	RW	REPORTRDY																											Write '1' to Enable interrupt on *EVENTS_REPORTRDY* event						
			Set	1																									Enable						
			Disabled	0																									Read: Disabled						
			Enabled	1																									Read: Enabled						
C	RW	ACCOF																											Write '1' to Enable interrupt on *EVENTS_ACCOF* event						
			Set	1																									Enable						
			Disabled	0																									Read: Disabled						
			Enabled	1																									Read: Enabled						
D	RW	DBLRDY																											Write '1' to Enable interrupt on *EVENTS_DBLRDY* event						
			Set	1																									Enable						
			Disabled	0																									Read: Disabled						
			Enabled	1																									Read: Enabled						
E	RW	STOPPED																											Write '1' to Enable interrupt on *EVENTS_STOPPED* event						
			Set	1																									Enable						
			Disabled	0																									Read: Disabled						
			Enabled	1																									Read: Enabled						

34.7.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	SAMPLERDY																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	REPORTRDY																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	ACCOF																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
D	RW	DBLRDY																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
E	RW	STOPPED																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															

34.7.4 ENABLE

Address offset: 0x500

Enable the quadrature decoder

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	ENABLE																																	
			Disabled	0																															
			Enabled	1																															

34.7.5 LEDPOL

Address offset: 0x504

LED output pin polarity

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	LEDPOL																																	
			ActiveLow	0																															
			ActiveHigh	1																															

34.7.6 SAMPLEPER

Address offset: 0x508

Sample period

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	SAMPLEPER																																	
				Sample period. The SAMPLE register will be updated for every new sample																															
			128us	0																															
				128 us																															
			256us	1																															
				256 us																															
			512us	2																															
				512 us																															
			1024us	3																															
				1024 us																															
			2048us	4																															
				2048 us																															
			4096us	5																															
				4096 us																															
			8192us	6																															
				8192 us																															
			16384us	7																															
				16384 us																															
			32ms	8																															
				32768 us																															
			65ms	9																															
				65536 us																															
			131ms	10																															
				131072 us																															

34.7.7 SAMPLE

Address offset: 0x50C

Motion sample value

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	SAMPLE		[-1..2]																															
				The value is a 2's complement value, and the sign gives the direction of the motion. The value '2' indicates a double transition.																															

34.7.8 REPORTPER

Address offset: 0x510

Number of samples to be taken before REPORTRDY and DBLRDY events can be generated

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	REPORTPER																																	
				Specifies the number of samples to be accumulated in the ACC register before the REPORTRDY and DBLRDY events can be generated																															
				The report period in [us] is given as: RPUS = SP * RP Where RPUS is the report period in [us/report], SP is the sample period in [us/sample] specified in SAMPLEPER, and RP is the report period in [samples/report] specified in REPORTPER .																															
			10Smpl	0																															
				10 samples / report																															
			40Smpl	1																															
				40 samples / report																															
			80Smpl	2																															
				80 samples / report																															
			120Smpl	3																															
				120 samples / report																															
			160Smpl	4																															
				160 samples / report																															

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A
Reset 0x00000000			**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**Value Id**	**Value**	**Description**
	200Smpl	5	200 samples / report
	240Smpl	6	240 samples / report
	280Smpl	7	280 samples / report
	1Smpl	8	1 sample / report

34.7.9 ACC

Address offset: 0x514

Register accumulating the valid transitions

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000			**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**Value Id**	**Value**	**Description**
A		[-1024..1023]	Register accumulating all valid samples (not double transition) read from the SAMPLE register Double transitions (SAMPLE = 2) will not be accumulated in this register. The value is a 32 bit 2's complement value. If a sample that would cause this register to overflow or underflow is received, the sample will be ignored and an overflow event (ACCOF) will be generated. The ACC register is cleared by triggering the READCLRACC or the RDCLRACC task.

34.7.10 ACCREAD

Address offset: 0x518

Snapshot of the ACC register, updated by the READCLRACC or RDCLRACC task

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000			**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**Value Id**	**Value**	**Description**
A		[-1024..1023]	Snapshot of the ACC register. The ACCREAD register is updated when the READCLRACC or RDCLRACC task is triggered

34.7.11 PSEL.LED

Address offset: 0x51C

Pin select for LED signal

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			C A A A A
Reset 0xFFFFFFFF			**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Id	**Value Id**	**Value**	**Description**
A		[0..31]	Pin number
C			Connection
	Disconnected	1	Disconnect
	Connected	0	Connect

34.7.12 PSEL.A

Address offset: 0x520

Pin select for A signal

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				C A A A A A
Reset 0xFFFFFFFF				**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	PIN		[0..31]	Pin number
C	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

34.7.13 PSEL.B

Address offset: 0x524

Pin select for B signal

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				C A A A A A
Reset 0xFFFFFFFF				**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	PIN		[0..31]	Pin number
C	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

34.7.14 DBFEN

Address offset: 0x528

Enable input debounce filters

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	DBFEN			Enable input debounce filters
			Disabled	0	Debounce input filters disabled
			Enabled	1	Debounce input filters enabled

34.7.15 LEDPRE

Address offset: 0x540

Time period the LED is switched ON prior to sampling

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A
Reset 0x00000010				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	LEDPRE		[0..511]	Period in us the LED is switched on prior to sampling

34.7.16 ACCDBL

Address offset: 0x544

Register accumulating the number of detected double transitions

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	R	ACCDBL		[0..15]	Register accumulating the number of detected double or illegal transitions. (SAMPLE = 2).

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																													A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
					When this register has reached its maximum value the accumulation of double / illegal transitions will stop. An overflow event (ACCOF) will be generated if any double or illegal transitions are detected after the maximum value was reached. This field is cleared by triggering the READCLRACC or RDCLRDBL task.

34.7.17 ACCDBLREAD

Address offset: 0x548

Snapshot of the ACCDBL, updated by the READCLRACC or RDCLRDBL task

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																													A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	R	ACCDBLREAD		[0..15]	Snapshot of the ACCDBL register. This field is updated when the READCLRACC or RDCLRDBL task is triggered.

34.8 Electrical Specification

34.8.1 QDEC Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
I_{QDEC}	Run current		5		µA
t_{SAMPLE}	Time between sampling signals from quadrature decoder	128		131072	µs
t_{LED}	Time from LED is turned on to signals are sampled	0		511	µs

35 Successive approximation analog-to-digital converter (SAADC)

The ADC is a differential successive approximation register (SAR) analog-to-digital converter.

Listed here are the main features of SAADC:

- 8/10/12-bit resolution
- Up to eight input channels
  - One channel per single-ended input and two channels per differential input
  - Scan mode can be configured with both single-ended channels and differential channels.
- Full scale input range (0 to VDD)
- Sampling triggered via a task from software or a PPI channel for full flexibility on sample frequency source from low power 32.768kHz RTC or more accurate 1/16MHz Timers
- One-shot conversion mode to sample a single channel
- Scan mode to sample a series of channels in sequence. Sample delay between channels is t_{ack} + t_{conv} which may vary between channels according to user configuration of tack.
- Support for direct sample transfer to RAM using EasyDMA
- Interrupts on single sample and full buffer events
- Samples stored as 16-bit 2’s compliment values for differential and single-ended sampling
- Continuous sampling without the need of an external timer
- Internal resistor string
- Limit checking on the fly

35.1 Overview

The ADC supports up to eight external analog input channels, depending on package variant. It can be operated in a one-shot mode with sampling under software control, or a continuous conversion mode with a programmable sampling rate.

The analog inputs can be configured as eight single-ended inputs, four differential inputs or a combination of these. Each channel can be configured to select `AIN0` to `AIN7` pins, or the `VDD` pin. Channels can be sampled individually in one-shot or continuous sampling modes, or, using scan mode, multiple channels can be sampled in sequence. Channels can also be oversampled to improve noise performance.

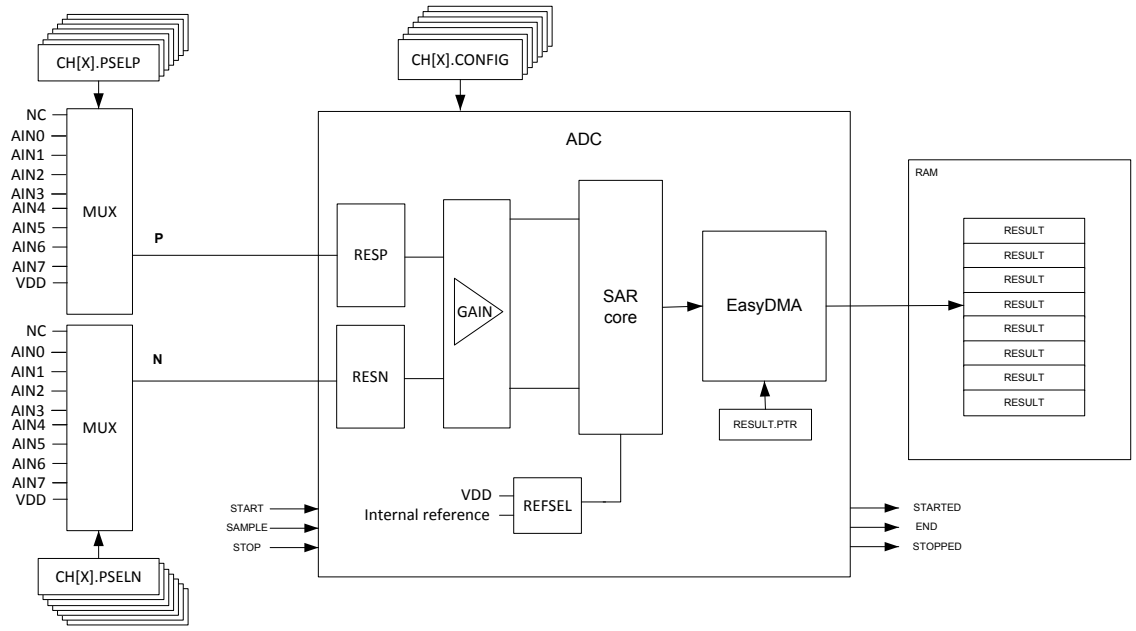

Figure 93: Simplified ADC block diagram

Internally, the ADC is always a differential analog-to-digital converter, but by default it is configured with single-ended input in the MODE field of the CH[n].CONFIG register. In single-ended mode, the negative input will be shorted to ground internally.

The assumption in single-ended mode is that the internal ground of the ADC is the same as the external ground that the measured voltage is referred to. The ADC is thus sensitive to ground bounce on the PCB in single-ended mode. If this is a concern we recommend using differential measurement.

35.2 Digital output

The output result of the ADC depends on the settings in the CH[n].CONFIG and RESOLUTION registers as follows:

$$RESULT = [V(P) - V(N)] * GAIN/REFERENCE * 2^{(RESOLUTION - m)}$$

where V(P) is the voltage at input P, V(N) is the voltage at input N, GAIN is the selected gain setting, REFERENCE is the selected reference voltage, and m=0 if CONFIG.MODE=SE, or m=1 if CONFIG.MODE=Diff.

The result generated by the ADC will deviate from the expected due DC errors like offset, gain, differential non-linearity (DNL), and integral non-linearity (INL). See *Electrical specification* for details on these parameters. The result can also vary due to AC errors like non-linearities in the GAIN block, settling errors due to high source impedance and sampling jitter. For battery measurement the DC errors are most noticeable.

The ADC has a wide selection of gains controlled in the GAIN field of the CH[n].CONFIG register. If CH[n].CONFIG.REFSEL=0, the input range of the ADC core is nominally +-0.6 V differential and the input must be scaled accordingly.

The ADC has a temperature dependent offset. If the ADC is to operate over a large temperature range, we recommend running CALIBRATEOFFSET at regular intervals, a CALIBRATEDONE event will be fired whenthe calibration is complete

35.3 Analog inputs and channels

Up to eight analog input channels, CH[n](n=0..7), can be configured.

See *Shared resources* on page 349 for shared input with comparators.

Any one of the available channels can be enabled for the ADC to operate in one-shot mode. If more than one CH[n] is configured, the ADC enters scan mode.

An analog input is selected as a positive converter input if CH[n].PSELP is set, setting CH[n].PSELP also enables the particular channel.

An analog input is selected as a negative converter input if CH[n].PSELN is set. The CH[n].PSELN register will have no effect unless differential mode is enabled, see MODE field in CH[n].CONFIG register.

If more than one of the CH[n].PSELP registers is set, the device enters scan mode. Input selections in scan mode are controlled by the CH[n].PSELP and CH[n].PSELN registers, where CH[n].PSELN is only used if the particular scan channel is specified as differential, see MODE field in CH[n].CONFIG register.

> **Important:** Channels selected for either COMP or LPCOMP cannot be used at the same time for ADC sampling, though channels not selected for use by these blocks can be used by the ADC.

Table 81: Legal connectivity CH[n] vs. analog input

Channel input	Source	Connectivity
CH[n].PSELP	AIN0...AIN7	Yes(any)
CH[n].PSELP	VDD	Yes
CH[n].PSELN	AIN0...AIN7	Yes(any)
CH[n].PSELN	VDD	Yes

35.4 Operation modes

The ADC input configuration supports one-shot mode, continuous mode and scan mode.

Scan mode and oversampling cannot be combined.

35.4.1 One-shot mode

One-shot operation is configured by enabling only one of the available channels defined by CH[n].PSELP, CH[n].PSELN, and CH[n].CONFIG registers.

Upon a SAMPLE task, the ADC starts to sample the input voltage. The CH[n].CONFIG.TACQ controls the acquisition time.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event has the same meaning as DONE when no oversampling takes place. Note that both events may occur before the actual value has been transferred into RAM by EasyDMA. For more information, see *EasyDMA* on page 348.

35.4.2 Continuous mode

Continuous sampling can be achieved by using the internal timer in the ADC, or triggering the SAMPLE task from one of the general purpose timers through the PPI.

Care shall be taken to ensure that the sample rate fulfils following criteria, depending on how many channels are active:

$$f_{SAMPLE} < 1/[CHANNELS \times (t_{ACQ} + t_{conv})]$$

The SAMPLERATE register can be used to use a local timer instead of individual SAMPLE tasks. When SAMPLERATE.MODE is set to Timers, a single SAMPLE task is necessary to start the SAADC; a STOP task stops sampling. The SAMPLERATE.CC field controls the sample rate.

To return to normal sampling, set SAMPLERATE.MODE back to Task.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event has the same meaning as DONE when no oversampling takes place. Note: both events may occur before the actual value has been transferred into RAM by EasyDMA.

35.4.3 Oversampling

An accumulator in the ADC can be used to average noise on the analog input. In general, oversampling improves the signal-to-noise ratio (SNR). Oversampling, however, does not improve the integral non-linearity (INL), or differential non-linearity (DNL).

Oversampling and scan should not be combined, since oversampling and scan will average over input channels.

The accumulator is controlled in the OVERSAMPLE register. The SAMPLE task must be set $2^{OVERSAMPLE}$ number of times before the result is written to RAM. This can be achieved by:

- Configuring a fixed sampling rate using a general purpose timer and PPI to trigger a SAMPLE task
- Triggering SAMPLE $2^{OVERSAMPLE}$ times from software
- Enabling BURST mode

CH[n].CONFIG.BURST can be enabled to avoid setting SAMPLE task $2^{OVERSAMPLE}$ times. With BURST = 1 the ADC will sample the input $2^{OVERSAMPLE}$ times as fast as it can (actual timing: $<(t_{ACQ}+t_{CONV})\times 2^{OVERSAMPLE}$). Thus, for the user it will just appear like the conversion took a bit longer time, but other than that, it is similar to one-shot mode. Scan mode can be combined with BURST=1, if burst is enabled on all channels.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event signals that enough conversions have taken place for an oversampled result to get transferred into RAM. Note that both events may occur before the actual value has been transferred into RAM by EasyDMA.

35.4.4 Scan mode

A channel is considered enabled if CH[n].PSELP is set. If more than one channel, CH[n], is enabled, the ADC enters scan mode.

In scan mode, one SAMPLE task will trigger one conversion per enabled channel. The time it takes to sample all channels is:

$$\text{Total time} < \text{Sum}(CH[x].t_{ACQ}+t_{CONV}),\ x=0..\text{enabled channels}$$

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event signals has the same meaning as DONE when no oversampling takes place. Note: both event may occur before the actual values have been transferred into RAM by EasyDMA.

35.5 Resistor ladder

The ADC has an internal resistor string for positive and negative input.

See *Figure 94: Resistor ladder for positive input (negative input is equivalent, using RESN instead of RESP)* on page 347. The resistors are controlled in the CH[n].CONFIG.RESP and CH[n].CONFIG.RESN registers.

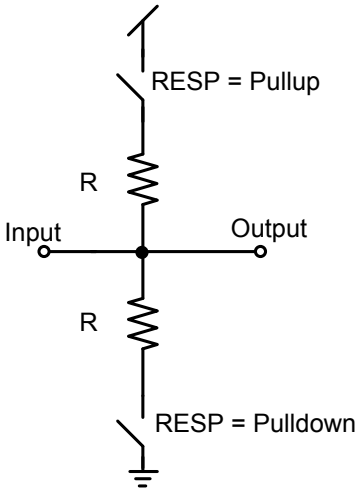

Figure 94: Resistor ladder for positive input (negative input is equivalent, using RESN instead of RESP)

35.6 Reference

The ADC can use two different references, controlled in the REFSEL field of the CH[n].CONFIG register.

These are:

- Internal reference
- VDD as reference

The internal reference results in an input range of +-0.6 V on the ADC core. VDD as reference results in an input range of +-VDD/4 on the ADC core. The gain block can be used to change the effective input range of the ADC.

```
Input range = (+- 0.6 V or +-VDD/4)/Gain
```

For example, choosing VDD as reference, single ended input (grounded negative input), and a gain of 1/4 the input range will be:

```
Input range = (VDD/4)/(1/4) = VDD
```

With internal reference, single ended input (grounded negative input), and a gain of 1/6 the input range will be:

```
Input range = (0.6 V)/(1/6) = 3.6 V
```

The AIN0-AIN7 inputs cannot exceed VDD, or be lower than VSS.

35.7 Acquisition time

To sample the input voltage, the ADC connects a capacitor to the input.

For illustration, see *Figure 95: Simplified ADC sample network* on page 348. The acquisition time indicates how long the capacitor is connected, see TACQ field in CH[n].CONFIG register. The required acquisition time depends on the source (R_{source}) resistance. For high source resistance the acquisition time should be increased, see *Table 82: Acquisition time* on page 348.

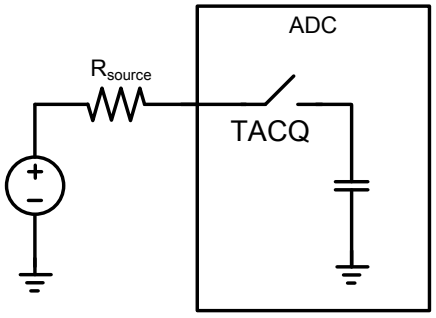

Figure 95: Simplified ADC sample network

Table 82: Acquisition time

TACQ [µs]	Maximum source resistance [kOhm]
3	10
5	40
10	100
15	200
20	400
40	800

35.8 Limits event monitoring

A channel can be event monitored by configuring limit register CH[n].LIMIT.

If the conversion result is higher than the defined high limit, or lower than the defined low limit, the appropriate event will fire.

35.9 EasyDMA

After configuring RESULT.PTR and RESULT.MAXCNT, the ADC resources are started by triggering the START task. The ADC is using EasyDMA to store results in a Result buffer in RAM.

The Result buffer is located at the address specified in the RESULT.PTR register. The RESULT.PTR register is double-buffered and it can be updated and prepared for the next START task immediately after the STARTED event is generated. The size of the Result buffer is specified in the RESULT.MAXCNT register and the ADC will generate an END event when it has filled up the Result buffer, see *Figure 96: ADC* on page 349. Results are stored in little-endian byte order in Data RAM. Every sample will be sign extended to 16 bit before stored in the Result buffer.

The ADC is stopped by triggering the STOP task. The STOP task will terminate an ongoing sampling. The ADC will generate a STOPPED event when it has stopped. If the ADC is already stopped when the STOP task is triggered, the STOPPED event will still be generated.

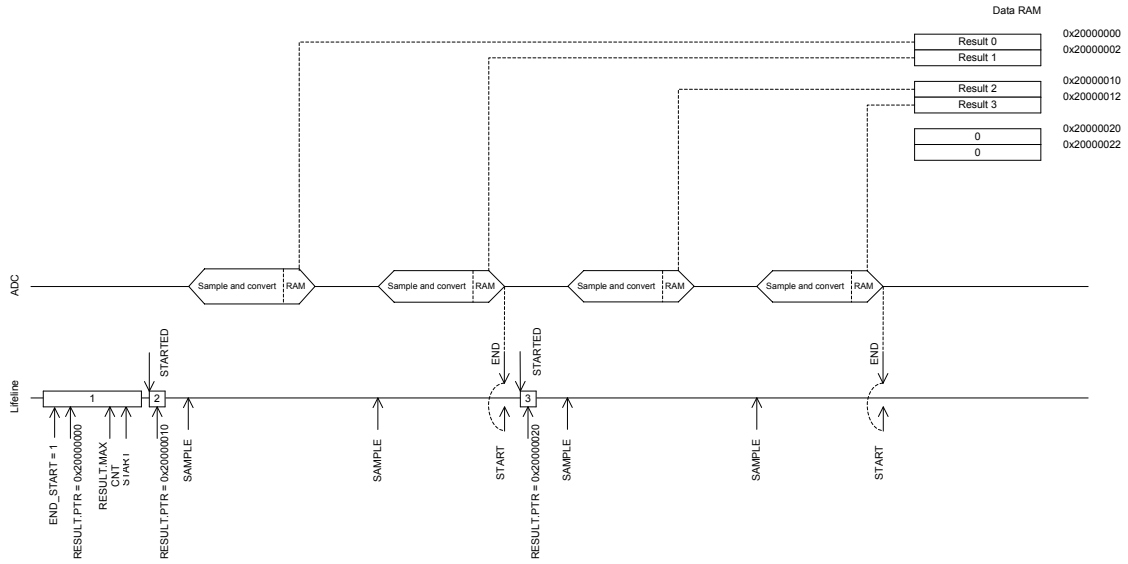

Figure 96: ADC

If the RESULT.PTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 34 for more information about the different memory regions.

The EasyDMA will have finished accessing the RAM when the END or STOPPED event has been generated.

The RESULT.AMOUNT register can be queried following an END event or a STOPPED event to see how many results have been transferred to the Result buffer in RAM since the START task was triggered.

In Scan mode the size of the Result buffer must be large enough to have room for minimum one result from each of the enabled channels. To secure this RESULT.MAXCNT must be specified to RESULT.MAXCNT >= "number of channels enabled". See *Scan mode* on page 346 for more information about Scan mode.

35.10 Shared resources

The ADC can coexist with COMP, LPCOMP and other peripherals using one of `AIN0-AIN7`, provided these are assigned to different pins.

It is not recommended to select the same analog input pin for both modules.

35.11 Registers

Table 83: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40007000	SAADC	SAADC	Analog to digital converter	

Table 84: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start the ADC and prepare the result buffer in RAM
TASKS_SAMPLE	0x004	Take one ADC sample, if scan is enabled all channels are sampled
TASKS_STOP	0x008	Stop the ADC and terminate any on-going conversion
TASKS_CALIBRATEOFFSE	0x00C	Starts offset auto-calibration
EVENTS_STARTED	0x100	The ADC has started
EVENTS_END	0x104	The ADC has filled up the Result buffer
EVENTS_DONE	0x108	A conversion task has been completed. Depending on the mode, multiple conversions might be needed for a result to be transferred to RAM.
EVENTS_RESULTDONE	0x10C	A result is ready to get transferred to RAM

Register	Offset	Description
EVENTS_CALIBRATEDON	0x110	Calibration is complete
EVENTS_STOPPED	0x114	The ADC has stopped
EVENTS_CH[0].LIMITH	0x118	Last results is equal or above CH[0].LIMIT.HIGH
EVENTS_CH[0].LIMITL	0x11C	Last results is equal or below CH[0].LIMIT.LOW
EVENTS_CH[1].LIMITH	0x120	Last results is equal or above CH[1].LIMIT.HIGH
EVENTS_CH[1].LIMITL	0x124	Last results is equal or below CH[1].LIMIT.LOW
EVENTS_CH[2].LIMITH	0x128	Last results is equal or above CH[2].LIMIT.HIGH
EVENTS_CH[2].LIMITL	0x12C	Last results is equal or below CH[2].LIMIT.LOW
EVENTS_CH[3].LIMITH	0x130	Last results is equal or above CH[3].LIMIT.HIGH
EVENTS_CH[3].LIMITL	0x134	Last results is equal or below CH[3].LIMIT.LOW
EVENTS_CH[4].LIMITH	0x138	Last results is equal or above CH[4].LIMIT.HIGH
EVENTS_CH[4].LIMITL	0x13C	Last results is equal or below CH[4].LIMIT.LOW
EVENTS_CH[5].LIMITH	0x140	Last results is equal or above CH[5].LIMIT.HIGH
EVENTS_CH[5].LIMITL	0x144	Last results is equal or below CH[5].LIMIT.LOW
EVENTS_CH[6].LIMITH	0x148	Last results is equal or above CH[6].LIMIT.HIGH
EVENTS_CH[6].LIMITL	0x14C	Last results is equal or below CH[6].LIMIT.LOW
EVENTS_CH[7].LIMITH	0x150	Last results is equal or above CH[7].LIMIT.HIGH
EVENTS_CH[7].LIMITL	0x154	Last results is equal or below CH[7].LIMIT.LOW
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
STATUS	0x400	Status
ENABLE	0x500	Enable or disable ADC
CH[0].PSELP	0x510	Input positive pin selection for CH[0]
CH[0].PSELN	0x514	Input negative pin selection for CH[0]
CH[0].CONFIG	0x518	Input configuration for CH[0]
CH[0].LIMIT	0x51C	High/low limits for event monitoring a channel
CH[1].PSELP	0x520	Input positive pin selection for CH[1]
CH[1].PSELN	0x524	Input negative pin selection for CH[1]
CH[1].CONFIG	0x528	Input configuration for CH[1]
CH[1].LIMIT	0x52C	High/low limits for event monitoring a channel
CH[2].PSELP	0x530	Input positive pin selection for CH[2]
CH[2].PSELN	0x534	Input negative pin selection for CH[2]
CH[2].CONFIG	0x538	Input configuration for CH[2]
CH[2].LIMIT	0x53C	High/low limits for event monitoring a channel
CH[3].PSELP	0x540	Input positive pin selection for CH[3]
CH[3].PSELN	0x544	Input negative pin selection for CH[3]
CH[3].CONFIG	0x548	Input configuration for CH[3]
CH[3].LIMIT	0x54C	High/low limits for event monitoring a channel
CH[4].PSELP	0x550	Input positive pin selection for CH[4]
CH[4].PSELN	0x554	Input negative pin selection for CH[4]
CH[4].CONFIG	0x558	Input configuration for CH[4]
CH[4].LIMIT	0x55C	High/low limits for event monitoring a channel
CH[5].PSELP	0x560	Input positive pin selection for CH[5]
CH[5].PSELN	0x564	Input negative pin selection for CH[5]
CH[5].CONFIG	0x568	Input configuration for CH[5]
CH[5].LIMIT	0x56C	High/low limits for event monitoring a channel
CH[6].PSELP	0x570	Input positive pin selection for CH[6]
CH[6].PSELN	0x574	Input negative pin selection for CH[6]
CH[6].CONFIG	0x578	Input configuration for CH[6]
CH[6].LIMIT	0x57C	High/low limits for event monitoring a channel
CH[7].PSELP	0x580	Input positive pin selection for CH[7]
CH[7].PSELN	0x584	Input negative pin selection for CH[7]
CH[7].CONFIG	0x588	Input configuration for CH[7]
CH[7].LIMIT	0x58C	High/low limits for event monitoring a channel
RESOLUTION	0x5F0	Resolution configuration
OVERSAMPLE	0x5F4	Oversampling configuration. OVERSAMPLE should not be combined with SCAN. The RESOLUTION is applied before averaging, thus for high OVERSAMPLE a higher RESOLUTION should be used.

Register	Offset	Description
SAMPLERATE	0x5F8	Controls normal or continuous sample rate
RESULT.PTR	0x62C	Data pointer
RESULT.MAXCNT	0x630	Maximum number of buffer words to transfer
RESULT.AMOUNT	0x634	Number of buffer words transferred since last START

35.11.1 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number																															
Id																															
														V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000														**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																										
A	RW	STARTED			Enable or disable interrupt on *EVENTS_STARTED* event																										
			Disabled	0	Disable																										
			Enabled	1	Enable																										
B	RW	END			Enable or disable interrupt on *EVENTS_END* event																										
			Disabled	0	Disable																										
			Enabled	1	Enable																										
C	RW	DONE			Enable or disable interrupt on *EVENTS_DONE* event																										
			Disabled	0	Disable																										
			Enabled	1	Enable																										
D	RW	RESULTDONE			Enable or disable interrupt on *EVENTS_RESULTDONE* event																										
			Disabled	0	Disable																										
			Enabled	1	Enable																										
E	RW	CALIBRATEDONE			Enable or disable interrupt on *EVENTS_CALIBRATEDONE* event																										
			Disabled	0	Disable																										
			Enabled	1	Enable																										
F	RW	STOPPED			Enable or disable interrupt on *EVENTS_STOPPED* event																										
			Disabled	0	Disable																										
			Enabled	1	Enable																										
G	RW	CH0LIMITH			Enable or disable interrupt on *EVENTS_CH[0].LIMITH* event																										
			Disabled	0	Disable																										
			Enabled	1	Enable																										
H	RW	CH0LIMITL			Enable or disable interrupt on *EVENTS_CH[0].LIMITL* event																										
			Disabled	0	Disable																										
			Enabled	1	Enable																										
I	RW	CH1LIMITH			Enable or disable interrupt on *EVENTS_CH[1].LIMITH* event																										
			Disabled	0	Disable																										
			Enabled	1	Enable																										
J	RW	CH1LIMITL			Enable or disable interrupt on *EVENTS_CH[1].LIMITL* event																										
			Disabled	0	Disable																										
			Enabled	1	Enable																										
K	RW	CH2LIMITH			Enable or disable interrupt on *EVENTS_CH[2].LIMITH* event																										
			Disabled	0	Disable																										
			Enabled	1	Enable																										
L	RW	CH2LIMITL			Enable or disable interrupt on *EVENTS_CH[2].LIMITL* event																										
			Disabled	0	Disable																										
			Enabled	1	Enable																										
M	RW	CH3LIMITH			Enable or disable interrupt on *EVENTS_CH[3].LIMITH* event																										
			Disabled	0	Disable																										
			Enabled	1	Enable																										
N	RW	CH3LIMITL			Enable or disable interrupt on *EVENTS_CH[3].LIMITL* event																										
			Disabled	0	Disable																										
			Enabled	1	Enable																										
O	RW	CH4LIMITH			Enable or disable interrupt on *EVENTS_CH[4].LIMITH* event																										
			Disabled	0	Disable																										

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id														V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Enabled	1																															
P	RW	CH4LIMITL																																	
			Disabled	0																															
			Enabled	1																															
Q	RW	CH5LIMITH																																	
			Disabled	0																															
			Enabled	1																															
R	RW	CH5LIMITL																																	
			Disabled	0																															
			Enabled	1																															
S	RW	CH6LIMITH																																	
			Disabled	0																															
			Enabled	1																															
T	RW	CH6LIMITL																																	
			Disabled	0																															
			Enabled	1																															
U	RW	CH7LIMITH																																	
			Disabled	0																															
			Enabled	1																															
V	RW	CH7LIMITL																																	
			Disabled	0																															
			Enabled	1																															

35.11.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id														V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	STARTED																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	END																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	DONE																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
D	RW	RESULTDONE																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
E	RW	CALIBRATEDONE																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
F	RW	STOPPED																																	
			Set	1																															
			Disabled	0																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id														V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Enabled	1																															
G	RW	CH0LIMITH																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
H	RW	CH0LIMITL																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
I	RW	CH1LIMITH																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
J	RW	CH1LIMITL																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
K	RW	CH2LIMITH																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
L	RW	CH2LIMITL																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
M	RW	CH3LIMITH																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
N	RW	CH3LIMITL																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
O	RW	CH4LIMITH																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
P	RW	CH4LIMITL																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
Q	RW	CH5LIMITH																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
R	RW	CH5LIMITL																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
S	RW	CH6LIMITH																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
T	RW	CH6LIMITL																																	
			Set	1																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id														V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Disabled	0																															
			Enabled	1																															
U	RW	CH7LIMITH																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
V	RW	CH7LIMITL																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															

35.11.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id														V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	STARTED																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	END																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	DONE																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
D	RW	RESULTDONE																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
E	RW	CALIBRATEDONE																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
F	RW	STOPPED																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
G	RW	CH0LIMITH																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
H	RW	CH0LIMITL																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
I	RW	CH1LIMITH																																	
			Clear	1																															
			Disabled	0																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id														V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Enabled	1																															
J	RW	CH1LIMITL																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
K	RW	CH2LIMITH																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
L	RW	CH2LIMITL																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
M	RW	CH3LIMITH																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
N	RW	CH3LIMITL																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
O	RW	CH4LIMITH																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
P	RW	CH4LIMITL																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
Q	RW	CH5LIMITH																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
R	RW	CH5LIMITL																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
S	RW	CH6LIMITH																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
T	RW	CH6LIMITL																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
U	RW	CH7LIMITH																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
V	RW	CH7LIMITL																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															

35.11.4 STATUS

Address offset: 0x400

Status

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															**Description**
A	R	STATUS																																	Status
			Ready	0																															ADC is ready. No on-going conversion.
			Busy	1																															ADC is busy. Conversion in progress.

35.11.5 ENABLE

Address offset: 0x500

Enable or disable ADC

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															**Description**
A	RW	ENABLE																																	Enable or disable ADC
			Disabled	0																															Disable ADC
			Enabled	1																															Enable ADC
																																			When enabled, the ADC will acquire access to the analog input pins specified in the CH[n].PSELP and CH[n].PSELN registers.

35.11.6 CH[0].PSELP

Address offset: 0x510

Input positive pin selection for CH[0]

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															**Description**
A	RW	PSELP																																	Analog positive input channel
			NC	0																															Not connected
			AnalogInput0	1																															AIN0
			AnalogInput1	2																															AIN1
			AnalogInput2	3																															AIN2
			AnalogInput3	4																															AIN3
			AnalogInput4	5																															AIN4
			AnalogInput5	6																															AIN5
			AnalogInput6	7																															AIN6
			AnalogInput7	8																															AIN7
			VDD	9																															VDD

35.11.7 CH[0].PSELN

Address offset: 0x514

Input negative pin selection for CH[0]

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															**Description**
A	RW	PSELN																																	Analog negative input, enables differential channel

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																														A	A	A	A	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**				**Value**																							**Description**					
			NC				0																							Not connected					
			AnalogInput0				1																							AIN0					
			AnalogInput1				2																							AIN1					
			AnalogInput2				3																							AIN2					
			AnalogInput3				4																							AIN3					
			AnalogInput4				5																							AIN4					
			AnalogInput5				6																							AIN5					
			AnalogInput6				7																							AIN6					
			AnalogInput7				8																							AIN7					
			VDD				9																							VDD					

35.11.8 CH[0].CONFIG

Address offset: 0x518

Input configuration for CH[0]

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id														F		E	E	E				D		C	C	C			B	B			A	A
Reset 0x00020000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**				**Value**																							**Description**					
A	RW	RESP																												Positive channel resistor control					
			Bypass				0																							Bypass resistor ladder					
			Pulldown				1																							Pull-down to GND					
			Pullup				2																							Pull-up to VDD					
			VDD1_2				3																							Set input at VDD/2					
B	RW	RESN																												Negative channel resistor control					
			Bypass				0																							Bypass resistor ladder					
			Pulldown				1																							Pull-down to GND					
			Pullup				2																							Pull-up to VDD					
			VDD1_2				3																							Set input at VDD/2					
C	RW	GAIN																												Gain control					
			Gain1_6				0																							1/6					
			Gain1_5				1																							1/5					
			Gain1_4				2																							1/4					
			Gain1_3				3																							1/3					
			Gain1_2				4																							1/2					
			Gain1				5																							1					
			Gain2				6																							2					
			Gain4				7																							4					
D	RW	REFSEL																												Reference control					
			Internal				0																							Internal reference (0.6 V)					
			VDD1_4				1																							VDD/4 as reference					
E	RW	TACQ																												Acquisition time, the time the ADC uses to sample the input voltage					
			3us				0																							3 us					
			5us				1																							5 us					
			10us				2																							10 us					
			15us				3																							15 us					
			20us				4																							20 us					
			40us				5																							40 us					
F	RW	MODE																												Enable differential mode					
			SE				0																							Single ended, PSELN will be ignored, negative input to ADC shorted to GND					
			Diff				1																							Differential					

35.11.9 CH[0].LIMIT

Address offset: 0x51C

High/low limits for event monitoring a channel

Bit number					31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id					B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x7FFF8000					**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																															
A	RW	LOW		[-32768 to +32767]	Low level limit																															
B	RW	HIGH		[-32768 to +32767]	High level limit																															

35.11.10 CH[1].PSELP

Address offset: 0x520

Input positive pin selection for CH[1]

Bit number					31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																A	A	A	A	A
Reset 0x00000000					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																															
A	RW	PSELP			Analog positive input channel																															
			NC	0	Not connected																															
			AnalogInput0	1	AIN0																															
			AnalogInput1	2	AIN1																															
			AnalogInput2	3	AIN2																															
			AnalogInput3	4	AIN3																															
			AnalogInput4	5	AIN4																															
			AnalogInput5	6	AIN5																															
			AnalogInput6	7	AIN6																															
			AnalogInput7	8	AIN7																															
			VDD	9	VDD																															

35.11.11 CH[1].PSELN

Address offset: 0x524

Input negative pin selection for CH[1]

Bit number					31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																A	A	A	A	A
Reset 0x00000000					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																															
A	RW	PSELN			Analog negative input, enables differential channel																															
			NC	0	Not connected																															
			AnalogInput0	1	AIN0																															
			AnalogInput1	2	AIN1																															
			AnalogInput2	3	AIN2																															
			AnalogInput3	4	AIN3																															
			AnalogInput4	5	AIN4																															
			AnalogInput5	6	AIN5																															
			AnalogInput6	7	AIN6																															
			AnalogInput7	8	AIN7																															
			VDD	9	VDD																															

35.11.12 CH[1].CONFIG

Address offset: 0x528

Input configuration for CH[1]

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id														F		E	E	E				D		C	C	C			B	B			A	A
Reset 0x00020000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																														**Description**
A	RW	RESP																																Positive channel resistor control
			Bypass	0																														Bypass resistor ladder
			Pulldown	1																														Pull-down to GND
			Pullup	2																														Pull-up to VDD
			VDD1_2	3																														Set input at VDD/2
B	RW	RESN																																Negative channel resistor control
			Bypass	0																														Bypass resistor ladder
			Pulldown	1																														Pull-down to GND
			Pullup	2																														Pull-up to VDD
			VDD1_2	3																														Set input at VDD/2
C	RW	GAIN																																Gain control
			Gain1_6	0																														1/6
			Gain1_5	1																														1/5
			Gain1_4	2																														1/4
			Gain1_3	3																														1/3
			Gain1_2	4																														1/2
			Gain1	5																														1
			Gain2	6																														2
			Gain4	7																														4
D	RW	REFSEL																																Reference control
			Internal	0																														Internal reference (0.6 V)
			VDD1_4	1																														VDD/4 as reference
E	RW	TACQ																																Acquisition time, the time the ADC uses to sample the input voltage
			3us	0																														3 us
			5us	1																														5 us
			10us	2																														10 us
			15us	3																														15 us
			20us	4																														20 us
			40us	5																														40 us
F	RW	MODE																																Enable differential mode
			SE	0																														Single ended, PSELN will be ignored, negative input to ADC shorted to GND
			Diff	1																														Differential

35.11.13 CH[1].LIMIT

Address offset: 0x52C

High/low limits for event monitoring a channel

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x7FFF8000			**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																														**Description**
A	RW	LOW		[-32768 to +32767]																														Low level limit
B	RW	HIGH		[-32768 to +32767]																														High level limit

35.11.14 CH[2].PSELP

Address offset: 0x530

Input positive pin selection for CH[2]

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																														A	A	A	A	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																							
A	RW	PSELP																																
			NC								0																							
			AnalogInput0								1																							
			AnalogInput1								2																							
			AnalogInput2								3																							
			AnalogInput3								4																							
			AnalogInput4								5																							
			AnalogInput5								6																							
			AnalogInput6								7																							
			AnalogInput7								8																							
			VDD								9																							

35.11.15 CH[2].PSELN

Address offset: 0x534

Input negative pin selection for CH[2]

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																														A	A	A	A	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																							
A	RW	PSELN																																
			NC								0																							
			AnalogInput0								1																							
			AnalogInput1								2																							
			AnalogInput2								3																							
			AnalogInput3								4																							
			AnalogInput4								5																							
			AnalogInput5								6																							
			AnalogInput6								7																							
			AnalogInput7								8																							
			VDD								9																							

35.11.16 CH[2].CONFIG

Address offset: 0x538

Input configuration for CH[2]

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id														F		E	E	E				D		C	C	C			B	B			A	A
Reset 0x00020000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																							
A	RW	RESP																																
			Bypass								0																							
			Pulldown								1																							
			Pullup								2																							
			VDD1_2								3																							
B	RW	RESN																																
			Bypass								0																							
			Pulldown								1																							
			Pullup								2																							
			VDD1_2								3																							
C	RW	GAIN																																
			Gain1_6								0																							
			Gain1_5								1																							

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															F		E	E	E				D		C	C	C			B	B			A	A
Reset 0x00020000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Gain1_4	2																															
			Gain1_3	3																															
			Gain1_2	4																															
			Gain1	5																															
			Gain2	6																															
			Gain4	7																															
D	RW	REFSEL																																	
			Internal	0																															
			VDD1_4	1																															
E	RW	TACQ																																	
			3us	0																															
			5us	1																															
			10us	2																															
			15us	3																															
			20us	4																															
			40us	5																															
F	RW	MODE																																	
			SE	0																															
			Diff	1																															

35.11.17 CH[2].LIMIT

Address offset: 0x53C

High/low limits for event monitoring a channel

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x7FFF8000				**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	LOW		[-32768 to +32767]																															
B	RW	HIGH		[-32768 to +32767]																															

35.11.18 CH[3].PSELP

Address offset: 0x540

Input positive pin selection for CH[3]

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PSELP																																	
			NC	0																															
			AnalogInput0	1																															
			AnalogInput1	2																															
			AnalogInput2	3																															
			AnalogInput3	4																															
			AnalogInput4	5																															
			AnalogInput5	6																															
			AnalogInput6	7																															
			AnalogInput7	8																															
			VDD	9																															

35.11.19 CH[3].PSELN

Address offset: 0x544

Input negative pin selection for CH[3]

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PSELN																																	
			NC	0																															
			AnalogInput0	1																															
			AnalogInput1	2																															
			AnalogInput2	3																															
			AnalogInput3	4																															
			AnalogInput4	5																															
			AnalogInput5	6																															
			AnalogInput6	7																															
			AnalogInput7	8																															
			VDD	9																															

35.11.20 CH[3].CONFIG

Address offset: 0x548

Input configuration for CH[3]

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															F		E	E	E				D		C	C	C			B	B			A	A
Reset 0x00020000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	RESP																																	
			Bypass	0																															
			Pulldown	1																															
			Pullup	2																															
			VDD1_2	3																															
B	RW	RESN																																	
			Bypass	0																															
			Pulldown	1																															
			Pullup	2																															
			VDD1_2	3																															
C	RW	GAIN																																	
			Gain1_6	0																															
			Gain1_5	1																															
			Gain1_4	2																															
			Gain1_3	3																															
			Gain1_2	4																															
			Gain1	5																															
			Gain2	6																															
			Gain4	7																															
D	RW	REFSEL																																	
			Internal	0																															
			VDD1_4	1																															
E	RW	TACQ																																	
			3us	0																															
			5us	1																															
			10us	2																															
			15us	3																															
			20us	4																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															F		E	E	E				D		C	C	C			B	B			A	A
Reset 0x00020000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			40us	5																															
F	RW	MODE																																	
			SE	0																															
			Diff	1																															

35.11.21 CH[3].LIMIT

Address offset: 0x54C

High/low limits for event monitoring a channel

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x7FFF8000				**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	LOW		[-32768 to +32767]																															
B	RW	HIGH		[-32768 to +32767]																															

35.11.22 CH[4].PSELP

Address offset: 0x550

Input positive pin selection for CH[4]

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PSELP																																	
			NC	0																															
			AnalogInput0	1																															
			AnalogInput1	2																															
			AnalogInput2	3																															
			AnalogInput3	4																															
			AnalogInput4	5																															
			AnalogInput5	6																															
			AnalogInput6	7																															
			AnalogInput7	8																															
			VDD	9																															

35.11.23 CH[4].PSELN

Address offset: 0x554

Input negative pin selection for CH[4]

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PSELN																																	
			NC	0																															
			AnalogInput0	1																															
			AnalogInput1	2																															
			AnalogInput2	3																															
			AnalogInput3	4																															
			AnalogInput4	5																															

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																														A	A	A	A	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**				**Value**																											
			AnalogInput5				6																							AIN5				
			AnalogInput6				7																							AIN6				
			AnalogInput7				8																							AIN7				
			VDD				9																							VDD				

35.11.24 CH[4].CONFIG

Address offset: 0x558

Input configuration for CH[4]

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id														F		E	E	E				D		C	C	C			B	B			A	A
Reset 0x00020000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**				**Value**																											
A	RW	RESP																																
			Bypass				0																							Bypass resistor ladder				
			Pulldown				1																							Pull-down to GND				
			Pullup				2																							Pull-up to VDD				
			VDD1_2				3																							Set input at VDD/2				
B	RW	RESN																																
			Bypass				0																							Bypass resistor ladder				
			Pulldown				1																							Pull-down to GND				
			Pullup				2																							Pull-up to VDD				
			VDD1_2				3																							Set input at VDD/2				
C	RW	GAIN																																
			Gain1_6				0																							1/6				
			Gain1_5				1																							1/5				
			Gain1_4				2																							1/4				
			Gain1_3				3																							1/3				
			Gain1_2				4																							1/2				
			Gain1				5																							1				
			Gain2				6																							2				
			Gain4				7																							4				
D	RW	REFSEL																																
			Internal				0																							Internal reference (0.6 V)				
			VDD1_4				1																							VDD/4 as reference				
E	RW	TACQ																																
																														Acquisition time, the time the ADC uses to sample the input voltage				
			3us				0																							3 us				
			5us				1																							5 us				
			10us				2																							10 us				
			15us				3																							15 us				
			20us				4																							20 us				
			40us				5																							40 us				
F	RW	MODE																																
			SE				0																							Single ended, PSELN will be ignored, negative input to ADC shorted to GND				
			Diff				1																							Differential				

35.11.25 CH[4].LIMIT

Address offset: 0x55C

High/low limits for event monitoring a channel

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x7FFF8000				**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	LOW		[-32768 to +32767]																															
B	RW	HIGH		[-32768 to +32767]																															

35.11.26 CH[5].PSELP

Address offset: 0x560

Input positive pin selection for CH[5]

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PSELP																																	
			NC	0																															
			AnalogInput0	1																															
			AnalogInput1	2																															
			AnalogInput2	3																															
			AnalogInput3	4																															
			AnalogInput4	5																															
			AnalogInput5	6																															
			AnalogInput6	7																															
			AnalogInput7	8																															
			VDD	9																															

35.11.27 CH[5].PSELN

Address offset: 0x564

Input negative pin selection for CH[5]

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PSELN																																	
			NC	0																															
			AnalogInput0	1																															
			AnalogInput1	2																															
			AnalogInput2	3																															
			AnalogInput3	4																															
			AnalogInput4	5																															
			AnalogInput5	6																															
			AnalogInput6	7																															
			AnalogInput7	8																															
			VDD	9																															

35.11.28 CH[5].CONFIG

Address offset: 0x568

Input configuration for CH[5]

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															F		E	E	E				D		C	C	C			B	B			A	A
Reset 0x00020000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	RESP																																	

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															F		E	E	E				D		C	C	C			B	B			A	A
Reset 0x00020000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Bypass	0																															
			Pulldown	1																															
			Pullup	2																															
			VDD1_2	3																															
B	RW	RESN																																	
			Bypass	0																															
			Pulldown	1																															
			Pullup	2																															
			VDD1_2	3																															
C	RW	GAIN																																	
			Gain1_6	0																															
			Gain1_5	1																															
			Gain1_4	2																															
			Gain1_3	3																															
			Gain1_2	4																															
			Gain1	5																															
			Gain2	6																															
			Gain4	7																															
D	RW	REFSEL																																	
			Internal	0																															
			VDD1_4	1																															
E	RW	TACQ																																	
			3us	0																															
			5us	1																															
			10us	2																															
			15us	3																															
			20us	4																															
			40us	5																															
F	RW	MODE																																	
			SE	0																															
			Diff	1																															

35.11.29 CH[5].LIMIT

Address offset: 0x56C

High/low limits for event monitoring a channel

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x7FFF8000				**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	LOW		[-32768 to +32767]																															
B	RW	HIGH		[-32768 to +32767]																															

35.11.30 CH[6].PSELP

Address offset: 0x570

Input positive pin selection for CH[6]

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																														A	A	A	A	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																							
A	RW	PSELP																																
			NC								0																							
			AnalogInput0								1																							
			AnalogInput1								2																							
			AnalogInput2								3																							
			AnalogInput3								4																							
			AnalogInput4								5																							
			AnalogInput5								6																							
			AnalogInput6								7																							
			AnalogInput7								8																							
			VDD								9																							

35.11.31 CH[6].PSELN

Address offset: 0x574

Input negative pin selection for CH[6]

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																														A	A	A	A	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																							
A	RW	PSELN																																
			NC								0																							
			AnalogInput0								1																							
			AnalogInput1								2																							
			AnalogInput2								3																							
			AnalogInput3								4																							
			AnalogInput4								5																							
			AnalogInput5								6																							
			AnalogInput6								7																							
			AnalogInput7								8																							
			VDD								9																							

35.11.32 CH[6].CONFIG

Address offset: 0x578

Input configuration for CH[6]

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id														F		E	E	E				D		C	C	C			B	B			A	A
Reset 0x00020000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																							
A	RW	RESP																																
			Bypass								0																							
			Pulldown								1																							
			Pullup								2																							
			VDD1_2								3																							
B	RW	RESN																																
			Bypass								0																							
			Pulldown								1																							
			Pullup								2																							
			VDD1_2								3																							
C	RW	GAIN																																
			Gain1_6								0																							
			Gain1_5								1																							

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															F		E	E	E				D		C	C	C			B	B			A	A
Reset 0x00020000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Gain1_4	2																															
			Gain1_3	3																															
			Gain1_2	4																															
			Gain1	5																															
			Gain2	6																															
			Gain4	7																															
D	RW	REFSEL																																	
			Internal	0																															
			VDD1_4	1																															
E	RW	TACQ																																	
			3us	0																															
			5us	1																															
			10us	2																															
			15us	3																															
			20us	4																															
			40us	5																															
F	RW	MODE																																	
			SE	0																															
			Diff	1																															

35.11.33 CH[6].LIMIT

Address offset: 0x57C

High/low limits for event monitoring a channel

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x7FFF8000				**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	LOW		[-32768 to +32767]																															
B	RW	HIGH		[-32768 to +32767]																															

35.11.34 CH[7].PSELP

Address offset: 0x580

Input positive pin selection for CH[7]

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PSELP																																	
			NC	0																															
			AnalogInput0	1																															
			AnalogInput1	2																															
			AnalogInput2	3																															
			AnalogInput3	4																															
			AnalogInput4	5																															
			AnalogInput5	6																															
			AnalogInput6	7																															
			AnalogInput7	8																															
			VDD	9																															

35.11.35 CH[7].PSELN

Address offset: 0x584

Input negative pin selection for CH[7]

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PSELN																																	
			NC	0																															
			AnalogInput0	1																															
			AnalogInput1	2																															
			AnalogInput2	3																															
			AnalogInput3	4																															
			AnalogInput4	5																															
			AnalogInput5	6																															
			AnalogInput6	7																															
			AnalogInput7	8																															
			VDD	9																															

35.11.36 CH[7].CONFIG

Address offset: 0x588

Input configuration for CH[7]

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															F		E	E	E				D		C	C	C			B	B			A	A
Reset 0x00020000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	RESP																																	
			Bypass	0																															
			Pulldown	1																															
			Pullup	2																															
			VDD1_2	3																															
B	RW	RESN																																	
			Bypass	0																															
			Pulldown	1																															
			Pullup	2																															
			VDD1_2	3																															
C	RW	GAIN																																	
			Gain1_6	0																															
			Gain1_5	1																															
			Gain1_4	2																															
			Gain1_3	3																															
			Gain1_2	4																															
			Gain1	5																															
			Gain2	6																															
			Gain4	7																															
D	RW	REFSEL																																	
			Internal	0																															
			VDD1_4	1																															
E	RW	TACQ																																	
			3us	0																															
			5us	1																															
			10us	2																															
			15us	3																															
			20us	4																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															F		E	E	E				D		C	C	C			B	B			A	A
Reset 0x00020000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			40us	5																															
F	RW	MODE																																	
			SE	0																															
			Diff	1																															

35.11.37 CH[7].LIMIT

Address offset: 0x58C

High/low limits for event monitoring a channel

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x7FFF8000				**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	LOW		[-32768 to +32767]																															
B	RW	HIGH		[-32768 to +32767]																															

35.11.38 RESOLUTION

Address offset: 0x5F0

Resolution configuration

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																	A	A	A
Reset 0x00000001				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	VAL																																	
			8bit	0																															
			10bit	1																															
			12bit	2																															
			14bit	3																															

35.11.39 OVERSAMPLE

Address offset: 0x5F4

Oversampling configuration. OVERSAMPLE should not be combined with SCAN. The RESOLUTION is applied before averaging, thus for high OVERSAMPLE a higher RESOLUTION should be used.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	OVERSAMPLE																																	
			Bypass	0																															
			Over2x	1																															
			Over4x	2																															
			Over8x	3																															
			Over16x	4																															
			Over32x	5																															
			Over64x	6																															
			Over128x	7																															
			Over256x	8																															

35.11.40 SAMPLERATE

Address offset: 0x5F8

Controls normal or continuous sample rate

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																							B		A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	CC		[80..2047]																															
B	RW	MODE																																	
			Task	0																															
			Timers	1																															

35.11.41 RESULT.PTR

Address offset: 0x62C

Data pointer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PTR																																	

35.11.42 RESULT.MAXCNT

Address offset: 0x630

Maximum number of buffer words to transfer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	MAXCNT																																	

35.11.43 RESULT.AMOUNT

Address offset: 0x634

Number of buffer words transferred since last START

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	AMOUNT																																	

35.12 Electrical Specification

35.12.1 SAADC Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
DNL	Differential non-linearity, 10-bit resolution	-0.95	<1		LSB
INL	Integral non-linearity, 10-bit resolution		1		LSB
V_{OS}	Differential offset error (calibrated), 10-bit resolution [a]	-15		15	LSB
C_{EG}	Gain error temperature coefficient	-0.05		0.05	%/°C

[a] Digital output code at zero volt differential input.

Symbol	Description	Min.	Typ.	Max.	Units
f_{SAMPLE}	Maximum sampling rate			200	kHz
$t_{ACQ,10k}$	Acquisition time (configurable), source Resistance <= 10kOhm		3		µs
$t_{ACQ,40k}$	Acquisition time (configurable), source Resistance <= 40kOhm		5		µs
$t_{ACQ,100k}$	Acquisition time (configurable), source Resistance <= 100kOhm		10		µs
$t_{ACQ,200k}$	Acquisition time (configurable), source Resistance <= 200kOhm		15		µs
$t_{ACQ,400k}$	Acquisition time (configurable), source Resistance <= 400kOhm		20		µs
$t_{ACQ,800k}$	Acquisition time (configurable), source Resistance <= 800kOhm		40		µs
t_{CONV}	Conversion time		<2		µs
$I_{ADC,CONV}$	ADC current during ACQuisition and CONVersion[29]		700		µA
$I_{ADC,IDLE}$	Idle current, when not sampling, excluding clock sources and regulator base currents[30]		<5		µA
$E_{G1/6}$	Error[b] for Gain = 1/6	-3		3	%
$E_{G1/4}$	Error[b] for Gain = 1/4	-3		3	%
$E_{G1/2}$	Error[b] for Gain = 1/2	-3		4	%
E_{G1}	Error[b] for Gain = 1	-3		4	%
C_{SAMPLE}	Sample and hold capacitance at maximum gain[31]		2.5		pF
R_{INPUT}	Input resistance		>1		MΩ
E_{NOB}	Effective number of bits, differential mode, 12-bit resolution, 1/1 gain, 3 µs acquisition time, crystal HFCLK, 200 ksps		9		Bit
S_{NDR}	Peak signal to noise and distortion ratio, differential mode, 12-bit resolution, 1/1 gain, 3 µs acquisition time, crystal HFCLK, 200 ksps		56		dB
S_{FDR}	Spurious free dynamic range, differential mode, 12-bit resolution, 1/1 gain, 3 µs acquisition time, crystal HFCLK, 200 ksps		70		dBc
R_{LADDER}	Ladder resistance		160		kΩ

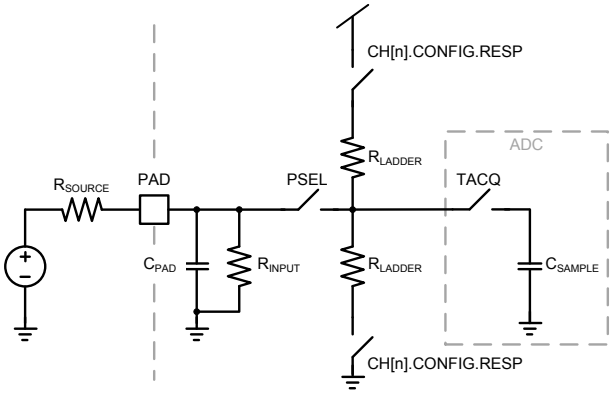

Figure 97: Model of SAADC input (one channel)

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Note: SAADC average current calculation for a given application is based on the sample period, conversion and acquisition time (t_{conv} and t_{ACQ}) and conversion and idle current ($I_{ADC,CONV}$ and $I_{ADC,IDLE}$). For example, sampling at 4kHz gives a sample period of 250µs. The average current consumption would then be:

$$I_{AVERAGE} = \left(\frac{\left(t_{CONV} + t_{ACQ}\right)}{250}\right)\left(I_{ADC,CONV}\right) + \left(\frac{250 - \left(t_{CONV} + t_{ACQ}\right)}{250}\right)\left(I_{ADC,IDLE}\right)$$

29 During ACQuisition and CONVersion, the best power supply quality will be requested in 1V3. If DC/DC is active, it will operate in normal mode during that time.

30 When t_{ACQ} is 10us or longer, and if DC/DC is active, it will be allowed to work in refresh mode if no other resource is requiring a high quality power supply from 1V3. If t_{ACQ} is smaller than 10us and DC/DC is active, refresh mode will not be allowed, and it will remain in normal mode from the START task to the STOPPED event. So depending on t_{ACQ} and other resources' needs, the appropriate base current needs to be taken into account.

b Does not include temperature drift

31 Maximum gain corresponds to highest capacitance.

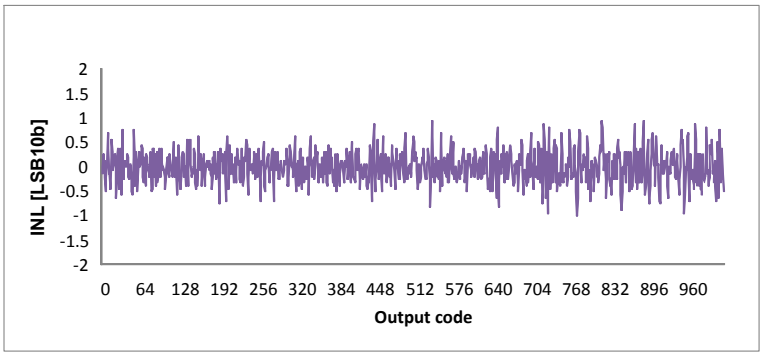


Figure 98: ADC INL vs Output Code

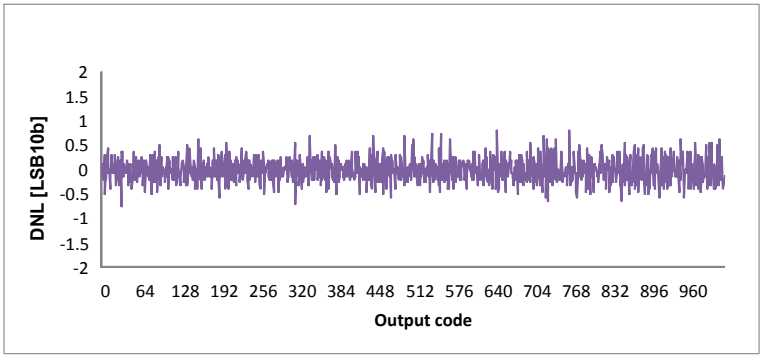


Figure 99: ADC DNL vs Output Code

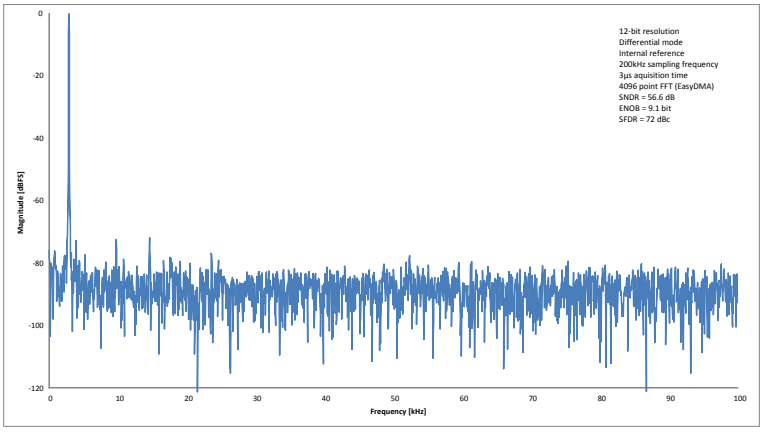


Figure 100: FFT of a 2.8 kHz sine at 200 ksps ()

35.13 Performance factors

Clock jitter, affecting sample timing accuracy, and circuit noise can affect ADC performance.

Jitter can be between START tasks or from START task to acquisition. START timer accuracy and startup times of regulators and references will contribute to variability. Sources of circuit noise may include CPU activity and the DC/DC converter. Best ADC performance is achieved using START timing based on the TIMER module, HFXO clock source, and Constant Latency mode.

36 Comparator (COMP)

The Comparator (COMP) compares the input voltage (VIN+) that is derived from an analog input pin selected via the PSEL register against a second input voltage (VIN-) that can be derived from multiple sources depending on operation mode.

Listed here are the main features for COMP:

- Input range 0 V to VDD
- Single-ended mode
  - Fully flexible hysteresis using a 64-level reference ladder
- Differential mode
  - Configurable 50 mV hysteresis
- Reference inputs:
  - VDD
  - External reference from AIN0 to AIN1 (between 0 V and VDD)
  - Internal references 1.2 V, 1.8 V and 2.4 V
- Three operation modes: low power, normal and high-speed
- Single-pin capacitive sensor support
- Event generation on output changes
  - UP event on VIN- > VIN+
  - DOWN event on VIN- < VIN+
  - CROSS event on VIN+ and VIN- crossing
  - READY event on core and internal reference (if used) ready

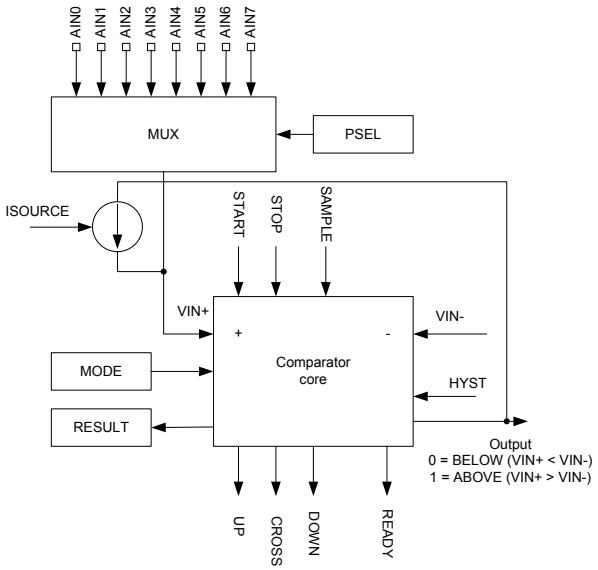


Figure 101: Comparator overview

> **Important:** COMP cannot be used (STARTed) at the same time as LPCOMP. Only one comparator can be used at a time.

The COMP is started by triggering the START task, and stopped by triggering the STOP task. After a start-up time of $t_{COMP,START}$ [32] the COMP will generate a READY event to indicate that the comparator is ready

[32] See $t_{PROPDLY,LP}$, $t_{PROPDLY,N}$, $t_{PROPDLY,HS}$, $I_{COMP,LP}$, $I_{COMP,N}$ and $I_{COMP,HS}$ in *Electrical parameters* for more information about COMP speed and power characteristics related to these different modes.

to use and the output of the COMP is correct. When the COMP module is started, events will be generated every time VIN+ crosses VIN-.

VIN- can be derived directly from AIN0 or AIN1 in differential mode, or VREF in single-ended mode. VUP and VDOWN thresholds can be set to implement a hysteresis on VIN- using the Reference Ladder. VREF can be derived from VDD, AIN0, AIN1 or internal 1.2V, 1.8V and 2.4V references.

An upward crossing will generate an UP event and a downward crossing will generate a DOWN event. The CROSS event will be generated every time there is a crossing, independent of direction.

An optional hysteresis on VIN+ and VIN- can be enabled when the module is used in differential mode through the HYST register. In single ended mode the two reference ladders (VUP and VDOWN, see *Figure 104: Comparator in single-ended mode* on page 377) will be used instead of the hysteresis mechanism configured in HYST.

This hysteresis is in the order of magnitude of 50 mV, and shall prevent noise on the signal to create unwanted events. See *Figure 105: Hysteresis example where VIN+ starts below VUP* on page 377 for illustration of the effect of an active hysteresis on a noisy input signal.

The COMP can be configured to operate in two main operation modes, differential mode and single ended mode, see MODE register for more information.

The COMP can, for both main operation modes, operate in different speed and power consumption modes, see MODE register. High-speed mode will consume more power compared to low-power mode, and low-power mode will result in slower response time compared to high-speed mode.

The immediate value of the COMP can be sampled to the RESULT register by triggering the SAMPLE task.

A selectable current can be applied (ISOURCE register) on the currently selected AINx line. Enabling the block creates a feedback path around the comparator, forming a relaxation oscillator. The circuit will sink current from VIN+ when the comparator output is high, and source current into VIN+ when the comparator output is low. The frequency of the oscillator is dependent on the capacitance at the analog input pin, the reference voltages and the value of the current source. In this mode, only a capacitive sensor needs to be attached between the analog input pin and ground. With a selected current of 10 uA, VUP-VDOWN equal to 1 V, and an external capacity of typically 10 pF, the resulting oscillation frequency is around 500 kHz.

The frequency of the oscillator can be calculated as

```
f_OSC = I_SOURCE / (2C·(VUP-VDOWN) )
```

36.1 Differential mode

In differential mode, the reference input VIN- is derived directly from one of the AINx pins.

In this mode, the impedance on VIN-'s signal path is equal to the impedance on VIN+'s signal path. See $Z_{COMPVINP}$ and $Z_{COMPVINND}$ in the product specification for more information. In differential mode, the PSEL, MODE and EXTREFSEL registers must be configured before the COMP is enabled via the ENABLE register. When HYST is turned on while in this mode, the Output of the comparator (and associated events) will change from ABOVE to BELOW whenever VIN+ becomes smaller than (VIN- - ($V_{DIFFHYST}$ / 2)). Similarly, it will change from BELOW to ABOVE whenever VIN+ becomes larger than (VIN- + ($V_{DIFFHYST}$ / 2)), as illustrated in *Figure 103: Hysteresis enabled in differential mode* on page 376.

Restriction: Depending on the device, not all the analog inputs may be available for each MUX.

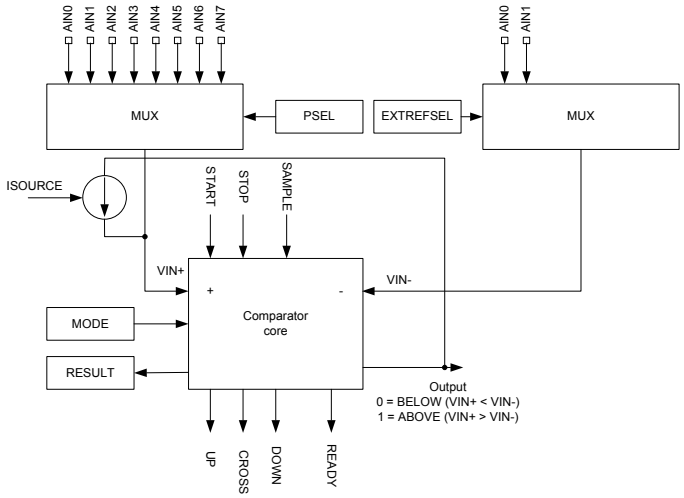
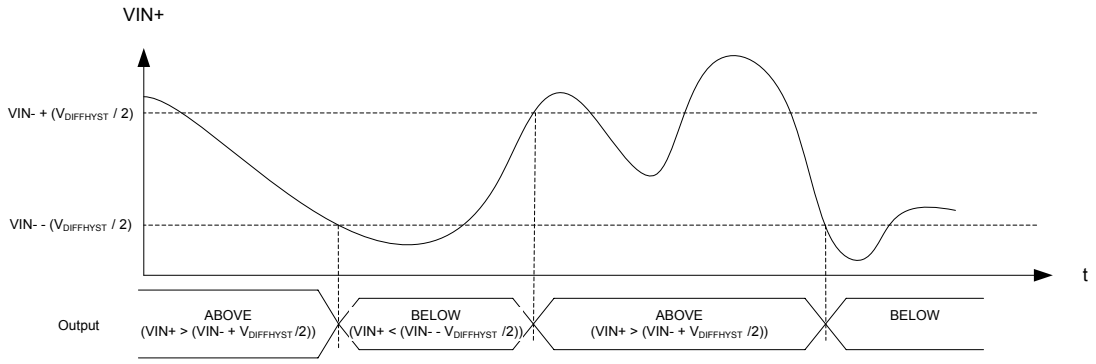


Figure 102: Comparator in differential mode

Figure 103: Hysteresis enabled in differential mode



36.2 Single-ended mode

In single-ended mode, VIN- is derived from the Reference Ladder.

In this mode, the impedance on VIN-'s signal path is different from $Z_{COMPVINP}$, see $Z_{COMVINNS}$ in the product specification for more information. The Reference Ladder uses the reference voltage VREF to derive two new voltage references, VUP and VDOWN. VUP and VDOWN are configured via THUP and THDOWN in the TH register. VREF can be sourced from any of the available references sources as illustrated in *Figure 104: Comparator in single-ended mode* on page 377. This is configured via EXTREFSEL and REFSEL.

When the comparator core detects that VIN+ > VIN-, i.e. ABOVE as per the RESULT register, VIN- will switch to VDOWN. When VIN- falls below VIN- again, VIN- will be switched back to VUP. By specifying VUP larger than VDOWN, a hysteresis as illustrated in *Figure 105: Hysteresis example where VIN+ starts below VUP* on page 377 and *Figure 106: Hysteresis example where VIN+ starts above VUP* on page 378 can be generated. In single-ended mode, the PSEL, MODE, EXTREFSEL, REFSEL and TH registers must be configured before the COMP is enabled via the ENABLE register.

Restriction: Depending on the device, not all the analog inputs may be available for each MUX.

Writing to the HYST register has no effect in single-ended mode, and the content of this register is ignored.

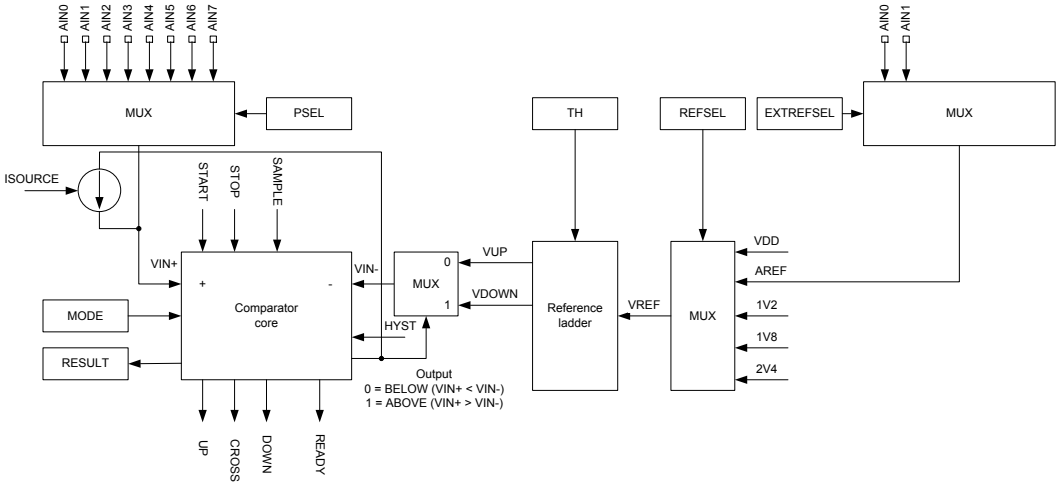


Figure 104: Comparator in single-ended mode

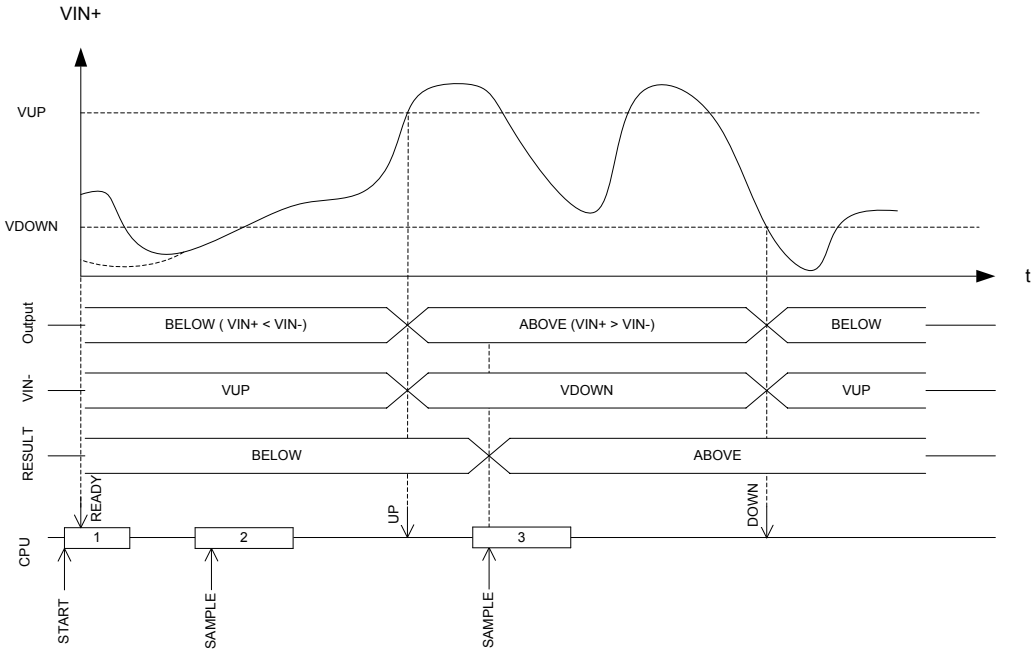


Figure 105: Hysteresis example where VIN+ starts below VUP

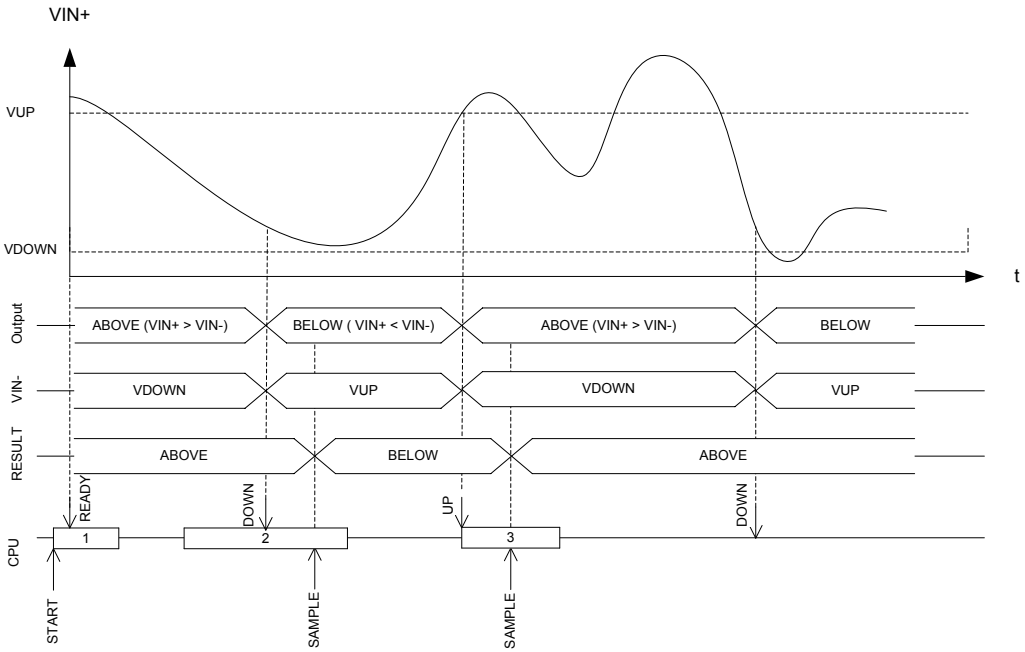


Figure 106: Hysteresis example where VIN+ starts above VUP

36.3 Pin configuration

The user can use the PSEL register to select one of the analog input pins, `AIN0` through `AIN7`, as input VIN +.

See *Figure 104: Comparator in single-ended mode* on page 377. Similarly the user can use the EXTREFSEL register to select one of the AINx analog input pins as reference input, in case AREF is selected in REFSEL. The selected analog pins will be acquired by the COMP when it is enabled via the ENABLE register.

Depending on the device, not all the analog inputs may be available for each MUX. See PSEL and EXTREFSEL register definition for more information about which analog pins are available on a particular device.

36.4 Shared resources

The COMP shares analog resources with the SAADC and LPCOMP peripherals.

While it is possible to use SAADC at the same time as COMP or LPCOMP, COMP and LPCOMP are mutually exclusive: enabling one will automatically disable the other. In addition, when using SAADC and COMP or LPCOMP simultaneously, it is not possible to select the same analog input pin for both modules.

> **Important:** The COMP peripheral shall not be disabled (by writing to the ENABLE register) before the peripheral has stopped; failing to do so may result in unpredictable behaviour.

36.5 Registers

Table 85: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40013000	COMP	COMP	General Purpose Comparator	

Table 86: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start comparator
TASKS_STOP	0x004	Stop comparator
TASKS_SAMPLE	0x008	Sample comparator value
EVENTS_READY	0x100	COMP is ready and output is valid
EVENTS_DOWN	0x104	Downward crossing
EVENTS_UP	0x108	Upward crossing
EVENTS_CROSS	0x10C	Downward or upward crossing
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
RESULT	0x400	Compare result
ENABLE	0x500	COMP enable
PSEL	0x504	Pin select
REFSEL	0x508	Reference source select
EXTREFSEL	0x50C	External reference select
TH	0x530	Threshold configuration for hysteresis unit
MODE	0x534	Mode configuration
HYST	0x538	Comparator hysteresis enable
ISOURCE	0x53C	Current source select on analog input

36.5.1 SHORTS

Address offset: 0x200

Shortcut register

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												E	D	C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	READY_SAMPLE			Shortcut between *EVENTS_READY* event and *TASKS_SAMPLE* task
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
B	RW	READY_STOP			Shortcut between *EVENTS_READY* event and *TASKS_STOP* task
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
C	RW	DOWN_STOP			Shortcut between *EVENTS_DOWN* event and *TASKS_STOP* task
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
D	RW	UP_STOP			Shortcut between *EVENTS_UP* event and *TASKS_STOP* task
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
E	RW	CROSS_STOP			Shortcut between *EVENTS_CROSS* event and *TASKS_STOP* task
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut

36.5.2 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															D	C	B	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	READY			Enable or disable interrupt on *EVENTS_READY* event
			Disabled	0	Disable
			Enabled	1	Enable
B	RW	DOWN			Enable or disable interrupt on *EVENTS_DOWN* event
			Disabled	0	Disable
			Enabled	1	Enable
C	RW	UP			Enable or disable interrupt on *EVENTS_UP* event
			Disabled	0	Disable
			Enabled	1	Enable
D	RW	CROSS			Enable or disable interrupt on *EVENTS_CROSS* event
			Disabled	0	Disable
			Enabled	1	Enable

36.5.3 INTENSET

Address offset: 0x304

Enable interrupt

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															D	C	B	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	READY			Write '1' to Enable interrupt on *EVENTS_READY* event
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
B	RW	DOWN			Write '1' to Enable interrupt on *EVENTS_DOWN* event
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
C	RW	UP			Write '1' to Enable interrupt on *EVENTS_UP* event
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	CROSS			Write '1' to Enable interrupt on *EVENTS_CROSS* event
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

36.5.4 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															D	C	B	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	READY			Write '1' to Disable interrupt on *EVENTS_READY* event
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
B	RW	DOWN			Write '1' to Disable interrupt on *EVENTS_DOWN* event
			Clear	1	Disable
			Disabled	0	Read: Disabled

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Enabled	1																															
C	RW	UP																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
D	RW	CROSS																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															

36.5.5 RESULT

Address offset: 0x400

Compare result

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	RESULT																																	
			Below	0																															
			Above	1																															

36.5.6 ENABLE

Address offset: 0x500

COMP enable

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	ENABLE																																	
			Disabled	0																															
			Enabled	2																															

36.5.7 PSEL

Address offset: 0x504

Pin select

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PSEL																																	
			AnalogInput0	0																															
			AnalogInput1	1																															
			AnalogInput2	2																															
			AnalogInput3	3																															
			AnalogInput4	4																															
			AnalogInput5	5																															
			AnalogInput6	6																															
			AnalogInput7	7																															

36.5.8 REFSEL

Address offset: 0x508

Reference source select

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	REFSEL																																	
			Int1V2	0																															
			Int1V8	1																															
			Int2V4	2																															
			VDD	4																															
			ARef	5																															

Id	RW	Field	Value Id	Value	Description
A	RW	REFSEL			Reference select
			Int1V2	0	VREF = internal 1.2 V reference (VDD >= 1.7 V)
			Int1V8	1	VREF = internal 1.8 V reference (VDD >= VREF + 0.2 V)
			Int2V4	2	VREF = internal 2.4 V reference (VDD >= VREF + 0.2 V)
			VDD	4	VREF = VDD
			ARef	5	VREF = AREF (VDD >= VREF >= AREFMIN)

36.5.9 EXTREFSEL

Address offset: 0x50C

External reference select

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	EXTREFSEL																																	
			AnalogReference0	0																															
			AnalogReference1	1																															

Id	RW	Field	Value Id	Value	Description
A	RW	EXTREFSEL			External analog reference select
			AnalogReference0	0	Use AIN0 as external analog reference
			AnalogReference1	1	Use AIN1 as external analog reference

36.5.10 TH

Address offset: 0x530

Threshold configuration for hysteresis unit

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																						B	B	B	B	B	B		A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	THUP		[63:0]																															
B	RW	THDOWN		[63:0]																															

Id	RW	Field	Value Id	Value	Description
A	RW	THUP		[63:0]	VUP = (THUP+1)/64*VREF
B	RW	THDOWN		[63:0]	VDOWN = (THDOWN+1)/64*VREF

36.5.11 MODE

Address offset: 0x534

Mode configuration

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																											B							A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	SP																																	
			Low	0																															
			Normal	1																															
			High	2																															
B	RW	MAIN																																	
			SE	0																															
			Diff	1																															

Id	RW	Field	Value Id	Value	Description
A	RW	SP			Speed and power mode
			Low	0	Low power mode
			Normal	1	Normal mode
			High	2	High speed mode
B	RW	MAIN			Main operation mode
			SE	0	Single ended mode
			Diff	1	Differential mode

36.5.12 HYST

Address offset: 0x538

Comparator hysteresis enable

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	HYST																																	
			NoHyst	0																															
			Hyst50mV	1																															

36.5.13 ISOURCE

Address offset: 0x53C

Current source select on analog input

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	ISOURCE																																	
			Off	0																															
			Ien2mA5	1																															
			Ien5mA	2																															
			Ien10mA	3																															

36.6 Electrical Specification

36.6.1 COMP Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
$I_{COMP,LP}$	Core run current in low power mode		2		µA
$I_{COMP,N}$	Core run current in normal mode		5		µA
$I_{COMP,HS}$	Core run current in high-speed mode		11		µA
$t_{PROPDLY,LP}$	Propagation delay, low power mode[a]			1.8	µS
$t_{PROPDLY,N}$	Propagation delay, normal mode[a]		0.4		µS
$t_{PROPDLY,HS}$	Propagation delay, high-speed mode[a]			0.2	µS
I_{SOURCE}	Configurable input current provided by the output driven current source.				µA
$I_{SOURCE,A}$			2.5		µA
$I_{SOURCE,B}$			5		µA
$I_{SOURCE,C}$			10		µA
$V_{DIFFHYST}$	Optional hysteresis applied to differential input		40		mV
$V_{VDD-VREF}$	Required difference between VDD and a selected VREF, VDD > VREF	0.3			V
I_{INT_REF}	Current used by the internal bandgap reference when selected as source for VREF		13		µA
$t_{INT\_REF,START}$	Startup time for the internal bandgap reference		50	80	µS
E_{INT_REF}	Internal bandgap reference error	-3		3	%
R_{LADDER}	Reference ladder resistance, ILADDER = VREF / RLADDER	1	550		kΩ
$V_{INPUTOFFSET}$	Input offset	-10		10	mV
$D_{NLLADDER}$	Differential non-linearity of reference ladder				LSB
$t_{COMP,START}$	Startup time for the comparator core			3	µS

[a] Propagation delay is with 10mV overdrive.

Total comparator run current must be calculated from the I_{COMP}, I_{INT_REF}, I_{SOURCE} and I_{LADDER} values for a given reference voltage.

37 Low power comparator (LPCOMP)

LPCOMP compares an input voltage against a reference voltage.

Listed here are the main features of LPCOMP:

- 0 - VDD input range
- Ultra low power
- eight external inputs (AIN0 to AIN7)
- Reference voltage options:
  - two external analog reference inputs, or
  - 15 level internal reference ladder (VDD/16)
- Optional hysteresis enable on input
- Wake up source from OFF mode

In System ON, the LPCOMP can generate separate events on rising and falling edges of a signal, or sample the current state of the pin as being above or below the selected reference. The block can be configured to use any of the analog inputs on the device. Additionally, the low power comparator can be used as an analog wakeup source from System OFF or System ON. The comparator threshold can be programmed to a range of fractions of the supply voltage.

Restriction: LPCOMP cannot be used (STARTed) at the same time as COMP. Only one comparator can be used at a time.

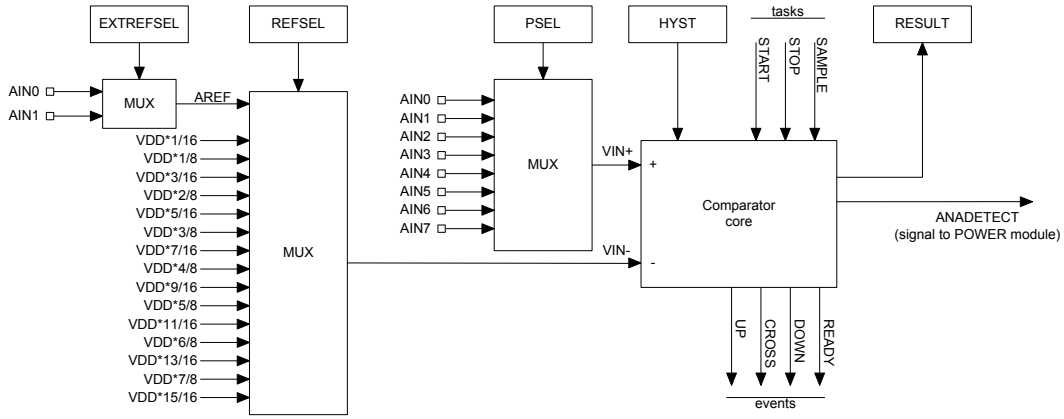


Figure 107: Low power comparator

The wakeup comparator (LPCOMP) compares an input voltage (VIN+), which comes from an analog input pin selected via the PSEL register against a reference voltage (VIN-) selected via the REFSEL and EXTREFSEL registers.

The PSEL, REFSEL, and EXTREFSEL registers must be configured before the LPCOMP is enabled through the ENABLE register.

The HYST register allows enabling an optional hysteresis in the comparator core. This hysteresis is in the order of magnitude of 50 mV, and shall prevent noise on the signal to create unwanted events. See *Figure 108: Effect of hysteresis on a noisy input signal* on page 386 for illustration of the effect of an active hysteresis on a noisy input signal. It is disabled by default, and shall be configured before enabling LPCOMP as well.

Specific chip variants may not offer all the reference and/or analog inputs defined here.

The LPCOMP is started by triggering the START task. After a start-up time of $t_{LPCOMP,STARTUP}$ the LPCOMP will generate a READY event to indicate that the comparator is ready to use and the output of the LPCOMP is correct. The LPCOMP will generate events every time VIN+ crosses VIN-. More specifically, every time VIN+ rises above VIN- (upward crossing) an UP event is generated along with a CROSS event. Every time VIN+ falls below VIN- (downward crossing), a DOWN event is generated along with a CROSS event. When

hysteresis is enabled, the upward crossing level becomes (VIN- + VHYST/2), and the downward crossing level becomes (VIN- - VHYST/2).

The LPCOMP is stopped by triggering the STOP task.

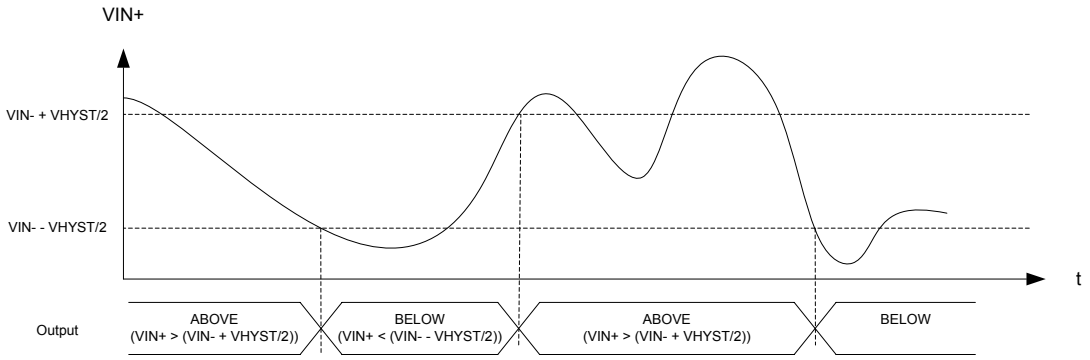


Figure 108: Effect of hysteresis on a noisy input signal

LPCOMP will be operational in both System ON and System OFF mode when it is enabled through the ENABLE register, see *Power management (POWER)* on page 79 for more information about power modes. All LPCOMP registers including the ENABLE register are classified as retained registers when the LPCOMP is enabled. However, when the device wakes up from System OFF, all LPCOMP registers will be reset.

The LPCOMP can wake up the system from System OFF by asserting the ANADETECT signal. The ANADETECT signal can be derived from any of the event sources that generate the UP, DOWN and CROSS events. In case of wakeup from System OFF, no events will be generated, only the ANADETECT signal. See the ANADETECT register (*ANADETECT* on page 390) for more information on how to configure the ANADETECT signal.

The immediate value of the LPCOMP can be sampled to the RESULT register by triggering the SAMPLE task.

See the RESETREAS register in the POWER module (*RESETREAS* on page 86) for more information on how to detect a wakeup from LPCOMP.

37.1 Pin configuration

You can use the PSEL register to select one of the analog input pins, `AIN0` through `AIN7`, as the analog input pin for the LPCOMP

See *Figure 17: GPIO Port and the GPIO pin details* on page 110 for more information on the pins. Similarly, you can use the EXTREFSEL register to select one of the analog reference input pins, AIN0 and AIN1, as input for AREF in case AREF is selected in REFSEL. The selected analog pins will be acquired by the LPCOMP when it is enabled through the ENABLE register. See the product specification for more information about which analog pins are available on a particular device.

37.2 Shared resources

The LPCOMP shares resources with other peripherals.

The LPCOMP shares analog resources with SAADC and COMP. While it is possible to use SAADC at the same time as COMP or LPCOMP, COMP and LPCOMP are mutually exclusive: enabling one will automatically disable the other. In addition, when using SAADC and COMP or LPCOMP simultaneously, it is not possible to select the same analog input pin for both modules.

> **Note:** The LPCOMP peripheral shall not be disabled (by writing to the ENABLE register) before the peripheral has been stopped; failing to do so may result in unpredictable behaviour.

37.3 Registers

Table 87: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40013000	LPCOMP	LPCOMP	Low power comparator	

Table 88: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start comparator
TASKS_STOP	0x004	Stop comparator
TASKS_SAMPLE	0x008	Sample comparator value
EVENTS_READY	0x100	LPCOMP is ready and output is valid
EVENTS_DOWN	0x104	Downward crossing
EVENTS_UP	0x108	Upward crossing
EVENTS_CROSS	0x10C	Downward or upward crossing
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
RESULT	0x400	Compare result
ENABLE	0x500	Enable LPCOMP
PSEL	0x504	Input pin select
REFSEL	0x508	Reference select
EXTREFSEL	0x50C	External reference select
ANADETECT	0x520	Analog detect configuration
HYST	0x538	Comparator hysteresis enable

37.3.1 SHORTS

Address offset: 0x200

Shortcut register

Bit number																															
Id																													E	D	C	B	A
Reset 0x00000000																													**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																										
A	RW	READY_SAMPLE			Shortcut between *EVENTS_READY* event and *TASKS_SAMPLE* task																										
			Disabled	0	Disable shortcut																										
			Enabled	1	Enable shortcut																										
B	RW	READY_STOP			Shortcut between *EVENTS_READY* event and *TASKS_STOP* task																										
			Disabled	0	Disable shortcut																										
			Enabled	1	Enable shortcut																										
C	RW	DOWN_STOP			Shortcut between *EVENTS_DOWN* event and *TASKS_STOP* task																										
			Disabled	0	Disable shortcut																										
			Enabled	1	Enable shortcut																										
D	RW	UP_STOP			Shortcut between *EVENTS_UP* event and *TASKS_STOP* task																										
			Disabled	0	Disable shortcut																										
			Enabled	1	Enable shortcut																										
E	RW	CROSS_STOP			Shortcut between *EVENTS_CROSS* event and *TASKS_STOP* task																										
			Disabled	0	Disable shortcut																										
			Enabled	1	Enable shortcut																										

37.3.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	READY																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	DOWN																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	UP																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
D	RW	CROSS																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															

37.3.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	READY																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	DOWN																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	UP																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
D	RW	CROSS																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															

37.3.4 RESULT

Address offset: 0x400

Compare result

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	RESULT																																	
			Bellow	0																															
			Above	1																															

37.3.5 ENABLE

Address offset: 0x500

Enable LPCOMP

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	ENABLE																																	
			Disabled	0																															
			Enabled	1																															

37.3.6 PSEL

Address offset: 0x504

Input pin select

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PSEL																																	
			AnalogInput0	0																															
			AnalogInput1	1																															
			AnalogInput2	2																															
			AnalogInput3	3																															
			AnalogInput4	4																															
			AnalogInput5	5																															
			AnalogInput6	6																															
			AnalogInput7	7																															

37.3.7 REFSEL

Address offset: 0x508

Reference select

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	REFSEL																																	
			Ref1_8Vdd	0																															
			Ref2_8Vdd	1																															
			Ref3_8Vdd	2																															
			Ref4_8Vdd	3																															
			Ref5_8Vdd	4																															
			Ref6_8Vdd	5																															
			Ref7_8Vdd	6																															
			ARef	7																															
			Ref1_16Vdd	8																															
			Ref3_16Vdd	9																															
			Ref5_16Vdd	10																															
			Ref7_16Vdd	11																															
			Ref9_16Vdd	12																															
			Ref11_16Vdd	13																															
			Ref13_16Vdd	14																															
			Ref15_16Vdd	15																															

37.3.8 EXTREFSEL

Address offset: 0x50C

External reference select

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	EXTREFSEL																																	
			AnalogReference0	0																															
			AnalogReference1	1																															

37.3.9 ANADETECT

Address offset: 0x520

Analog detect configuration

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	ANADETECT																																	
			Cross	0																															
			Up	1																															
			Down	2																															

37.3.10 HYST

Address offset: 0x538

Comparator hysteresis enable

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	HYST																																	
			NoHyst	0																															
			Hyst50mV	1																															

37.4 Electrical Specification

37.4.1 LPCOMP Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
I_{LPC}	Run current for low power comparator		0.5		µA
$t_{LPCANADET}$	Time from VIN crossing (>=50mV above threshold) to ANADETECT signal generated.		3		µs
$E_{REFLADDER}$	Error in reference ladder threshold voltage	-15		40	mV
V_{HYST}	Optional hysteresis		35		mV

38 Watchdog timer (WDT)

A countdown watchdog timer using the low-frequency clock source (LFCLK) offers configurable and robust protection against application lock-up.

The watchdog timer is started by triggering the START task.

The watchdog can be paused during long CPU sleep periods for low power applications and when the debugger has halted the CPU. The watchdog is implemented as a down-counter that generates a TIMEOUT event when it wraps over after counting down to 0. When the watchdog timer is started through the START task, the watchdog counter is loaded with the value specified in the CRV register. This counter is also reloaded with the value specified in the CRV register when a reload request is granted.

The watchdog's timeout period is given by:

```
timeout [s] = ( CRV + 1 ) / 32768
```

When started, the watchdog will automatically force the 32.768 kHz RC oscillator on as long as no other 32.768 kHz clock source is running and generating the 32.768 kHz system clock, see *CLOCK* chapter.

38.1 Reload criteria

The watchdog has eight separate reload request registers, which shall be used to request the watchdog to reload its counter with the value specified in the CRV register. To reload the watchdog counter, the special value 0x6E524635 needs to be written to all enabled reload registers.

One or more RR registers can be individually enabled through the RREN register.

38.2 Temporarily pausing the watchdog

By default, the watchdog will be active counting down the down-counter while the CPU is sleeping and when it is halted by the debugger. It is however possible to configure the watchdog to automatically pause while the CPU is sleeping as well as when it is halted by the debugger.

38.3 Watchdog reset

A TIMEOUT event will automatically lead to a watchdog reset equivalent to a system reset.

See *POWER chapter* for more information about reset sources. If the watchdog is configured to generate an interrupt on the TIMEOUT event, the watchdog reset will be postponed with two 32.768 kHz clock cycles after the TIMEOUT event has been generated. Once the TIMEOUT event has been generated, the impending watchdog reset will always be effectuated.

The watchdog must be configured before it is started. After it is started, the watchdog's configuration registers, which comprise registers CRV, RREN, and CONFIG, will be blocked for further configuration.

The watchdog is reset when the device is put into System OFF mode. The watchdog is also reset when the whole system is reset, except for when the system is reset through a soft reset, see *POWER chapter* for more information about reset types.

When the device starts running again, after a reset, or waking up from OFF mode, the watchdog configuration registers will be available for configuration again.

38.4 Registers

Table 89: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40010000	WDT	WDT	Watchdog Timer	

Table 90: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start the watchdog
EVENTS_TIMEOUT	0x100	Watchdog timeout
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
RUNSTATUS	0x400	Run status
REQSTATUS	0x404	Request status
CRV	0x504	Counter reload value
RREN	0x508	Enable register for reload request registers
CONFIG	0x50C	Configuration register
RR[0]	0x600	Reload request 0
RR[1]	0x604	Reload request 1
RR[2]	0x608	Reload request 2
RR[3]	0x60C	Reload request 3
RR[4]	0x610	Reload request 4
RR[5]	0x614	Reload request 5
RR[6]	0x618	Reload request 6
RR[7]	0x61C	Reload request 7

38.4.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																														
A	RW	TIMEOUT			Write '1' to Enable interrupt on *EVENTS_TIMEOUT* event																														
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														

38.4.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																														
A	RW	TIMEOUT			Write '1' to Disable interrupt on *EVENTS_TIMEOUT* event																														
			Clear	1	Disable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														

38.4.3 RUNSTATUS

Address offset: 0x400

Run status

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	RUNSTATUS																																	
			NotRunning	0																															
			Running	1																															

38.4.4 REQSTATUS

Address offset: 0x404

Request status

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												H	G	F	E	D	C	B	A
Reset 0x00000001				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	RR0																																	
			DisabledOrRequested	0																															
			EnabledAndUnrequested	1																															
B	R	RR1																																	
			DisabledOrRequested	0																															
			EnabledAndUnrequested	1																															
C	R	RR2																																	
			DisabledOrRequested	0																															
			EnabledAndUnrequested	1																															
D	R	RR3																																	
			DisabledOrRequested	0																															
			EnabledAndUnrequested	1																															
E	R	RR4																																	
			DisabledOrRequested	0																															
			EnabledAndUnrequested	1																															
F	R	RR5																																	
			DisabledOrRequested	0																															
			EnabledAndUnrequested	1																															
G	R	RR6																																	
			DisabledOrRequested	0																															
			EnabledAndUnrequested	1																															
H	R	RR7																																	
			DisabledOrRequested	0																															
			EnabledAndUnrequested	1																															

38.4.5 CRV

Address offset: 0x504

Counter reload value

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	CRV		[0x0000000F..0xFFFFFFFF																															
				clock																															

38.4.6 RREN

Address offset: 0x508

Enable register for reload request registers

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												H	G	F	E	D	C	B	A
Reset 0x00000001				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	RR0																																	
			Disabled	0																															
			Enabled	1																															
B	RW	RR1																																	
			Disabled	0																															
			Enabled	1																															
C	RW	RR2																																	
			Disabled	0																															
			Enabled	1																															
D	RW	RR3																																	
			Disabled	0																															
			Enabled	1																															
E	RW	RR4																																	
			Disabled	0																															
			Enabled	1																															
F	RW	RR5																																	
			Disabled	0																															
			Enabled	1																															
G	RW	RR6																																	
			Disabled	0																															
			Enabled	1																															
H	RW	RR7																																	
			Disabled	0																															
			Enabled	1																															

38.4.7 CONFIG

Address offset: 0x50C

Configuration register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																C			A
Reset 0x00000001				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	SLEEP																																	
			Pause	0																															
			Run	1																															
C	RW	HALT																																	
			Pause	0																															
			Run	1																															

38.4.8 RR[0]

Address offset: 0x600

Reload request 0

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	W	RR																																	

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**			**Value**																			**Description**									
			Reload			0x6E524635																			Value to request a reload of the watchdog timer									

38.4.9 RR[1]

Address offset: 0x604

Reload request 1

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**			**Value**																			**Description**									
A	W	RR																							Reload request register									
			Reload			0x6E524635																			Value to request a reload of the watchdog timer									

38.4.10 RR[2]

Address offset: 0x608

Reload request 2

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**			**Value**																			**Description**									
A	W	RR																							Reload request register									
			Reload			0x6E524635																			Value to request a reload of the watchdog timer									

38.4.11 RR[3]

Address offset: 0x60C

Reload request 3

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**			**Value**																			**Description**									
A	W	RR																							Reload request register									
			Reload			0x6E524635																			Value to request a reload of the watchdog timer									

38.4.12 RR[4]

Address offset: 0x610

Reload request 4

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**			**Value**																			**Description**									
A	W	RR																							Reload request register									
			Reload			0x6E524635																			Value to request a reload of the watchdog timer									

38.4.13 RR[5]

Address offset: 0x614

Reload request 5

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	W	RR																																	
			Reload	0x6E524635																															

38.4.14 RR[6]

Address offset: 0x618

Reload request 6

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	W	RR																																	
			Reload	0x6E524635																															

38.4.15 RR[7]

Address offset: 0x61C

Reload request 7

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	W	RR																																	
			Reload	0x6E524635																															

38.5 Electrical Specification

38.5.1 Watchdog Timer Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
I_{WDT}	Run current for watchdog timer		0.1		µA
t_{WDT}	Time out interval	31 µs		36 h	

39 Software Interrupts (SWI)

A set of interrupts have been reserved for use as software interrupts.

39.1 Registers

Table 91: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40014000	SWI	SWI0	Software interrupt 0	
0x40015000	SWI	SWI1	Software interrupt 1	
0x40016000	SWI	SWI2	Software interrupt 2	
0x40017000	SWI	SWI3	Software interrupt 3	
0x40018000	SWI	SWI4	Software interrupt 4	
0x40019000	SWI	SWI5	Software interrupt 5	

40 Near field communication tag (NFCT)

The NFCT peripheral (referred to as the 'NFC peripheral' from now on) supports communication signal interface type A and 106 kbps bit rate from NFC Forum.

With appropriate software, the NFC peripheral can be used to emulate the listening device NFC-A as specified by the NFC Forum.

Listed here are the main features for the NFC peripheral:

- NFC-A listen mode operation
  - 13.56 MHz input frequency
  - Bit rate 106 kbps
- Wake-on-field low power Field Detection (SENSE) mode
- Frame assemble and disassemble for the NFC-A frames specified by NFC Forum
- Programmable Frame Timing Controller
- Integrated automatic collision resolution, CRC and parity functions

40.1 Overview

The NFC peripheral is an implementation of an NFC Forum compliant listening device NFC-A.

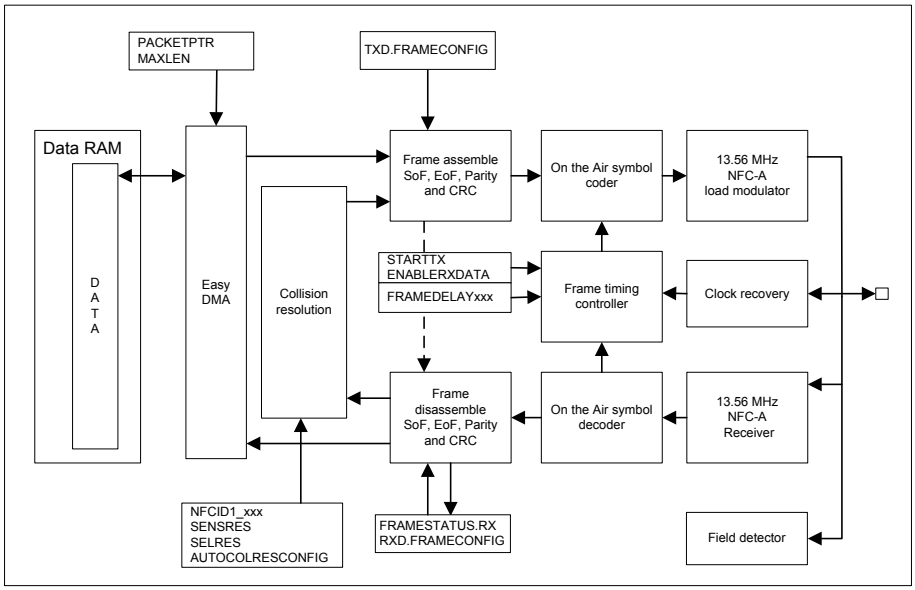


Figure 109: NFC block diagram

The NFC peripheral contains a 13.56 MHz AM receiver and a 13.56 MHz load modulator compatible with the NFC-A technology defined in the NFC Forum with 106 kbps data-rate.

The received frames will be automatically disassembled and the data part of the frame transferred to RAM. When transmitting, the frame data will be transferred directly from RAM and transmitted with configurable frame type and delay timing. The system will be notified by an event whenever a complete frame is received or sent.

It also supports the collision detection and resolution ("anticollision") as defined by NFC Forum.

Wake-on-field is supported in SENSE mode while the device is either in System OFF or System ON mode. When the antenna enters an NFC field, an event will be triggered notifying the system to activate the NFC functionality for incoming frames. In system ON, if the energy detected at the antenna increases beyond a threshold value, the module will generate a FIELDDETECTED event. The module will generate a FIELDLOST event when the quality or strength of the field no longer support NFC communication. Please refer to *NFCT Electrical Specification* on page 416 for the Low Power Field Detect threshold values.

In system OFF, the NFC Low Power Field Detect function can wake the system up through a reset. The NFC bit in the RESETREAS register will be set as cause of the wake-up, see *Reset* on page 83 in the POWER chapter. No FIELDDETECTED event is generated in that situation.

If the system is put into system OFF mode while a field is already present, the NFC Low Power Field Detect function will wake the system up right away and generate a reset.

Note that a reset has as a consequence to disable NFC, so the reset handler will have to enable NFC again and set it up properly.

Outgoing data will be collected from RAM with the EasyDMA function and assembled according to the TXD.FRAMECONFIG register. Incoming data will be disassembled according to the RXD.FRAMECONFIG register and the data section in the frame will be written to RAM via the EasyDMA function.

The NFC peripheral includes Frame Timing Controller that can be used to accurately control the inter-frame delay between the incoming frame and a corresponding outgoing frame. It also includes optional CRC functionality.

The NFC peripheral has a set of different states. The module can change state by triggering a task, or when specific operations are finalized. Events and tasks allow software to keep track of and change the current state.

See *Figure 109: NFC block diagram* on page 398, *Figure 110: NFC state diagram, automatic collision resolution enabled* on page 399 and *Figure 111: NFC state diagram, automatic collision resolution disabled* on page 400 for more information.

Notes:

- FIELDLOST event will not be reflected in the state machine (for instance by going back to the DISABLE state), it is up to software to decide on the actions to take when a field lost occurs.
- FIELDLOST event is not generated in SENSE mode.
- FIELDDETECTED event is generated only on the transition from FIELDLOST event to energy detected by the NFC peripheral. So, sending SENSE task while field is still present does not generate FIELDDETECTED event.
- If the FIELDDETECTED event is cleared before sending the ACTIVATE task, then the FIELDDETECTED event shows up again. The shortcut FIELDDETECTED_ACTIVATE can be used to avoid this condition.

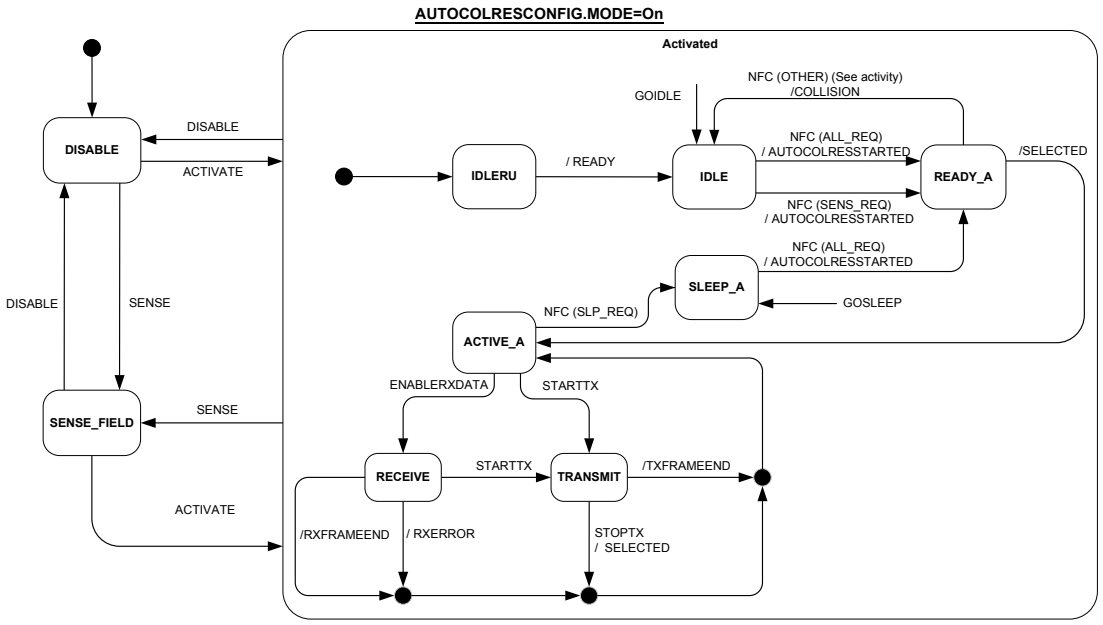


Figure 110: NFC state diagram, automatic collision resolution enabled

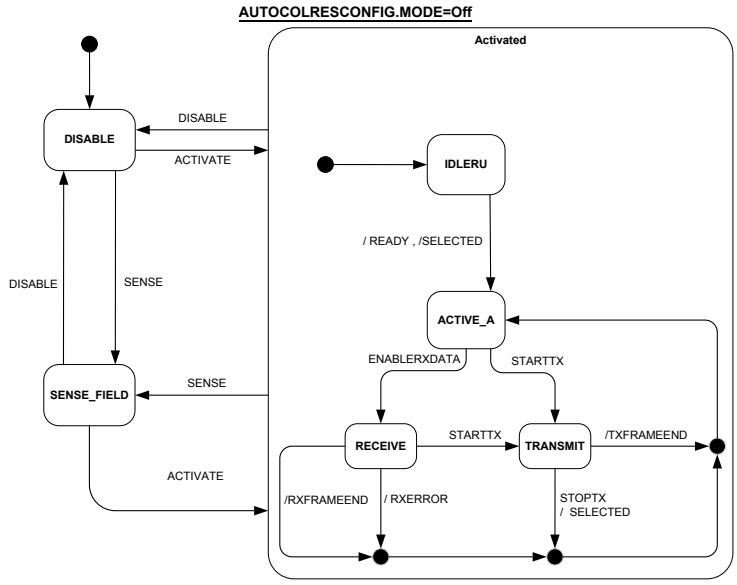


Figure 111: NFC state diagram, automatic collision resolution disabled

40.2 Collision resolution

The NFC peripheral implements an automatic collision resolution function as defined by the NFC Forum.

The SENSRES and SELRES registers need to be programmed upfront in order for the collision resolution to behave correctly. Depending on the NFCIDSIZE field in SENSRES, the following registers also need to be programmed upfront:

- NFCID1_LAST if NFCID1SIZE=NFCID1Single (ID = 4 bytes);
- NFCID1_2ND_LAST and NFCID1_LAST if NFCID1SIZE=NFCID1Double (ID = 7 bytes);
- NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST if NFCID1SIZE=NFCID1Triple (ID = 10 bytes);

Table 92: NFCID1 byte allocation (top sent first on air) on page 400 explains the position of the ID bytes in NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST, depending on the ID size, and as compared to the definition used in the *NFC Forum, NFC Digital Protocol Technical Specification*.

Table 92: NFCID1 byte allocation (top sent first on air)

	ID = 4 bytes	ID = 7 bytes	ID = 10 bytes
NFCID1_Q			$nfcid1_0$
NFCID1_R			$nfcid1_1$
NFCID1_S			$nfcid1_2$
NFCID1_T		$nfcid1_0$	$nfcid1_3$
NFCID1_U		$nfcid1_1$	$nfcid1_4$
NFCID1_V		$nfcid1_2$	$nfcid1_5$
NFCID1_W	$nfcid1_0$	$nfcid1_3$	$nfcid1_6$
NFCID1_X	$nfcid1_1$	$nfcid1_4$	$nfcid1_7$
NFCID1_Y	$nfcid1_2$	$nfcid1_5$	$nfcid1_8$
NFCID1_Z	$nfcid1_3$	$nfcid1_6$	$nfcid1_9$

Automatic collision resolution is enabled by default, and can be disabled through the MODE field in the AUTOCOLRESCONFIG register. When it is set to OFF, all commands will be sent over DMA as defined in disassembler.

The hardware implementation can handle the states from IDLE to ACTIVE_A automatically as defined in the *NFC Forum, NFC Activity Technical Specification*, and the other states are to be handled by software. The software keeps track of the state through events. The collision resolution will trigger an AUTOCOLRESSTARTED event when it has started. Reaching the ACTIVE_A state is indicated by the SELECTED event.

If collision resolution fails, a COLLISION event is triggered. Note that errors occurring during automatic collision resolution may also cause ERROR and/or RXERROR events to be generated. It is recommended that the software ignores those during automatic collision resolution.

Sending STOPTX task while the automatic collision resolution is in progress may cause unpredictable behaviour.

A pre-defined set of registers, NFC.TAGHEADER0..3, containing a valid NFCID1 value, is available in *FICR*, and can be used by software to populate the NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST registers. Refer to the release notes of the NFC stack for more details on the format.

40.3 Pin configuration

NFC uses two pins to connect the antenna.

These pins are shared with GPIOs, and the PROTECT field in the NFCPINS register in *UICR* defines the usage of these pins and their protection level against excessive voltages. The content of the NFCPINS register is reloaded at every reset.

When NFCPINS.PROTECT=NFC, a protection circuit will be enabled on the dedicated pins, preventing the chip from being damaged in the presence of a strong NFC field. The GPIO function will be disabled on those pins as well.

When NFCPINS.PROTECT=Disabled, the device will not be protected against strong NFC field damages caught by a connected NFC antenna, and the NFCT peripheral will not operate as expected, as it will never leave the DISABLE state.

The pins dedicated to the NFC antenna function will have some limitation when the pins are configured for normal GPIO operation. The pin capacitance will be higher on those (refer to C_{PAD_NFC} in the *GPIO Electrical Specification* on page 149 below), and some increased leakage current between the two pins is to be expected if they are used in GPIO mode, and are driven to different logical values. To save power the two pins should always be set to the same logical value whenever entering one of the device power saving modes. Please refer to I_{NFC_LEAK} in *GPIO Electrical Specification* on page 149 for details.

40.4 EasyDMA

The NFC peripheral implements EasyDMA for reading and writing of data packets from and to the Data RAM without CPU involvement.

The NFC EasyDMA utilizes one pointer called PACKETPTR for receiving and transmitting packets.

If the EasyDMA is processing a READ or WRITE event between the peripheral and the RAM, any new request for data transfer will be ignored. If a write and read operation is issued at the same time, the WRITE event would be prioritized. E.g. the peripheral has received a SoF symbol from a remote device and the CPU is requesting the module to enter the TRANSMIT state at the same time.

The MAXLEN register determines the maximum number of bytes that can be read from or written to the RAM. This feature can be used to secure that the NFC peripheral does not overwrite, or read beyond, the RAM assigned to a packet. Note that if the RXD.AMOUNT or TXD.AMOUNT register indicates longer data packets than set in MAXLEN, the frames sent to or received from the physical layer will be incomplete. In RX, the OVERRUN bit in the FRAMESTATUS.RX register will be set and an RXERROR event will be triggered in that situation.

Note that RXD.AMOUNT and TXD.AMOUNT define a frame length in bytes and bits excluding SoF, EoF and parity, but including CRC for RXD.AMOUNT only, make sure to take potential additional bits into account when setting MAXLEN.

If TXD.AMOUNT is smaller than MAXLEN, then at the end of a transmit frame, the NFCT is ready to receive, and any data received would be written into the same buffer in Data RAM, starting at the address next to the last sent byte, regardless whether PACKETPTR had been changed or not since the last TXFRAMESTART event. Only sending task ENABLERXDATA ensures that a new value in PACKETPTR pointing to the RX buffer in Data RAM is taken into account.

If PACKETPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See Chapter *Memory* on page 34 for more information about the different memory regions.

The NFC peripherals normally do alternative receive and transmit frames. So, to prepare for the next frame, the PACKETPTR, MAXLEN, TXD.FRAMECONFIG and TXD.AMOUNT can be updated while the receive is in progress, and, similarly, the PACKETPTR, MAXLEN and RXD.FRAMECONFIG can be updated while the transmit is in progress. They can be updated and prepared for the next NFC frame immediately after the STARTED event of the current frame has been received. Updating the TXD.FRAMECONFIG and TXD.AMOUNT during the current transmit frame or updating RXD.FRAMECONFIG during current receive frame may cause unpredictable behaviour.

In accordance with the NFC specification, the least a significant bit from the least significant byte is sent on air first. The bytes are stored in increasing order, starting at the lowest address in the EasyDMA buffer in RAM.

40.5 Frame timing controller

The NFC peripheral includes a frame timing controller that continuously keeps track of the number of the 13.56 MHz RF-carrier clock periods since the last positive pulse edge of the 13.56 MHz RF-signal envelope.

The NFC peripheral can be programmed to send a responding frame within a time window or at an exact count of RF-carrier periods. In case of FRAMEDELAYMODE = Window a STARTTX task triggered before the Frame Timing Controller counter is equal to FRAMEDELAYMIN will force the transmission to halt until the counter is equal to FRAMEDELAYMIN. If the counter is within FRAMEDELAYMIN and FRAMEDELAYMAX when the STARTTX task is triggered, the peripheral will start the transmission straight away. In case of FRAMEDELAYMODE = ExactVal, a STARTTX task, triggered before the frame delay counter is equal to FRAMEDELAYMAX, will halt the actual transmission start until the counter is equal to FRAMEDELAYMAX.

In case of FRAMEDELAYMODE = WindowGrid, the behaviour is similar to the FRAMEDELAYMODE = Window, but the actual transmission between FRAMEDELAYMIN and FRAMEDELAYMAX starts on a bit grid as defined for NFC-A Listen frames (slot duration of 128 RF-carrier periods).

The FRAMEDELAYMIN and FRAMEDELAYMAX values shall only be updated before the STARTTX task is triggered. Failing to do so may cause unpredictable behaviour. A ERROR event (with FRAMEDELAYTIMEOUT cause in ERRORSTATUS) will be asserted if the Frame Timing Controller counter reaches FRAMEDELAYMAX without any STARTTX task triggered. This may happen even when the response is not required as per *NFC Forum, NFC Digital Protocol Technical Specification*.
In the case when automatic collision resolution is enabled, any commands handled by the automatic collision resolution that don't involve a response being generated may also result in an ERROR event (with FRAMEDELAYTIMEOUT cause in ERRORSTATUS).

The frame timing controller operation is illustrated in *Figure 112: Frame Timing Controller (FRAMEDELAYMODE=Window)* on page 402.

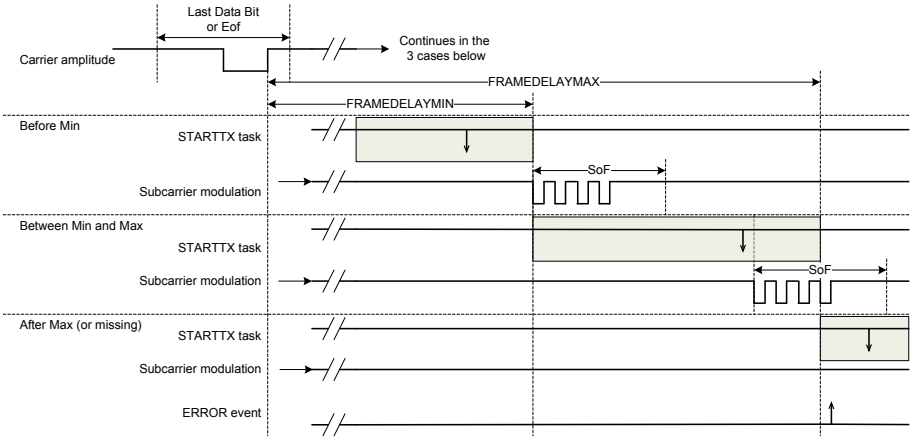


Figure 112: Frame Timing Controller (FRAMEDELAYMODE=Window)

40.6 Frame assembler

When asserting the STARTTX task the Frame assembler module will start reading TXD.AMOUNT.TXDATABYTES bytes (plus one additional byte if TXD.AMOUNT.TXDATABITS > 0) from the RAM position set by the PACKETPTR.

The NFC peripheral transmits the data as read from RAM, adding framing and the CRC calculated on the fly. The NFC peripheral will take (8*TXD.AMOUNT.TXDATABYTES + TXD.AMOUNT.TXDATABITS) bits and assemble a frame according to settings in TXD.FRAMECONFIG. Both short frames, standard frames and bit oriented SDD frames as specified in the NFC Forum Digital Protocol technical specification can be assembled by correct setting of the TXD.FRAMECONFIG register.

The bytes will be transmitted on air in the same order as they are read from RAM with a rising bit order within each byte (least significant bit first). That is, b0 will be transmitted on air before b1, and so on. The bits read from RAM will be coded into symbols as defined in the *NFC Forum, NFC Digital Protocol Technical Specification*.

> **Important:** Some NFC Forum documents, such as *NFC Forum, NFC Digital Protocol Technical Specification*. define bit numbering in a byte from b1 (LSb) to b8 (MSb), while most other technical documents from the NFC Forum, and also the Nordic Semiconductor documentation, traditionally numbers them from b0 to b7. The present document uses the b0 to b7 numbering scheme. Be aware of this when comparing with the *NFC Forum, NFC Digital Protocol Technical Specification* to others.

The frame assembler can be configured in TXD.FRAMECONFIG to add Start of Frame (SoF) symbol, calculate and add parity bits, and calculate and add CRC to the data read from RAM when assembling the frame. The total frame will then be longer than what is defined by TXD.AMOUNT.TXDATABYTES and TXDATABITS. DISCARDMODE will select if the first bits in the first byte read from RAM or the last bits in the last byte read from RAM will be discarded if TXD.AMOUNT.TXDATABITS are not equal to zero. Note that if TXD.FRAMECONFIG.PARITY = Parity and TXD.FRAMECONFIG.DISCARDMODE=DiscardStart, a parity bit will be included after the non-complete first byte. No parity will be added after a non-complete last byte.

The Frame Assemble operation is illustrated in *Figure 113: Frame assemble* on page 403 for different settings in TXD.FRAMECONFIG. All shaded bits fields are added by the frame assembler. Some of these bits are optional and appearances are configured in TXD.FRAMECONFIG. Please note that the frames illustrated do not necessarily comply with the NFC specification. The figure is only to illustrate the behavior of the NFC peripheral.

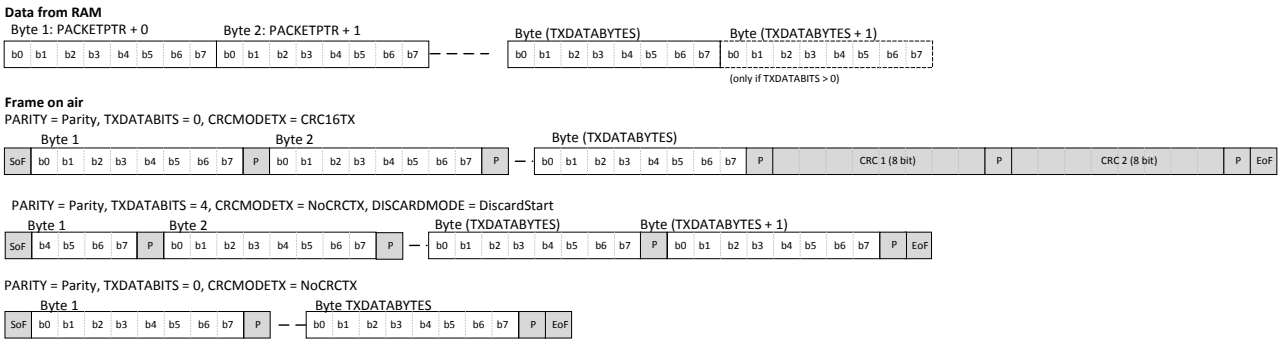


Figure 113: Frame assemble

The accurate timing for transmitting the frame on air is set using the frame timing controller settings.

40.7 Frame disassembler

By default, the NFC peripheral is active in RECEIVE mode after the SELECTED event, unless it goes into TRANSMIT mode by issuing STARTTX.

At the end of TX, the peripheral returns to RX mode and is ready to receive frames. In this state, when the poller transmits a frame, the NFC peripheral detects the Start of Frame (SoF).

If ENABLERXDATA was issued earlier, data will be written to RAM starting from PACKETPTR, and the NFC peripheral will assert the RXFRAMESTART event. The frame disassembler will verify and remove on the fly any parity bits and SoF and End of Frame (EoF) symbols based on RXD.FRAMECONFIG register configuration. It will, however, verify and transfer the CRC bytes into RAM, if the CRC is was enabled via RXD.FRAMECONFIG.

When an EoF symbol is detected the NFC peripheral will assert the RXFRAMEEND event and write the RXD.AMOUNT register to indicate numbers of received bytes and bits in the data packet. The module does not interpret the content of the data received from the remote NFC device, except for SoF, EoF, parity and CRC checking, as described above. The Frame disassemble operation is illustrated in *Figure 114: Frame disassemble illustration* on page 404.

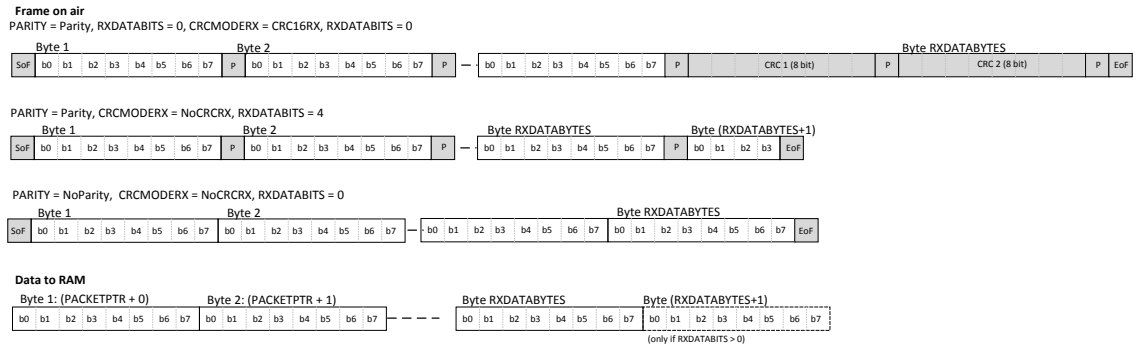


Figure 114: Frame disassemble illustration

40.8 Antenna interface

In ACTIVATED state, an amplitude regulator will adjust the voltage swing on the antenna pins to a value that is within the V_{swing} limit.

Refer to *NFCT Electrical Specification* on page 416.

40.9 NFCT antenna recommendations

The NFCT antenna coil must be connected differential between `NFC1` and `NFC2` pins of the device.

Two external capacitors should be used to tune the resonance of the antenna circuit to 13.56 MHz.

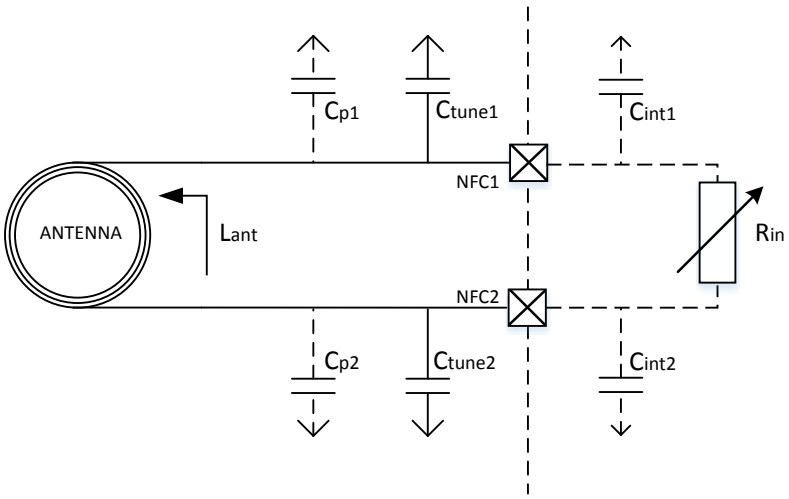


Figure 115: NFCT antenna recommendations

The required tuning capacitor value is given by the below equations:

$$C'_{tune} = \frac{1}{(2\pi \cdot 13.56\ MHz)^2 \cdot L_{ant}} \quad where\ C'_{tune} = \frac{1}{2} \cdot (C_p + C_{\text{int}} + C_{tune})$$

$$and\ C_{tune1} = C_{tune2} = C_{tune} \qquad C_{p1} = C_{p2} = C_p \qquad C_{\text{int1}} = C_{\text{int2}} = C_{\text{int}}$$

$$C_{tune} = \frac{2}{(2\pi \cdot 13.56\ MHz)^2 \cdot L_{ant}} - C_p - C_{\text{int}}$$

An antenna inductance of L_{ant} = 2 µH will give tuning capacitors in the range of 130 pF on each pin. For good performance, match the total capacitance on `NFC1` and `NFC2`.

40.10 Battery protection

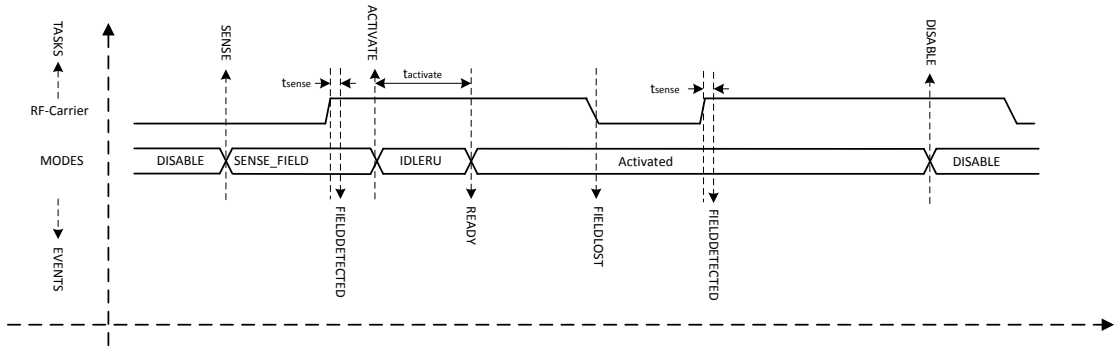
If the antenna is exposed to a strong NFC field, current may flow in the opposite direction on the supply due to parasitic diodes and ESD structures.

If the battery used does not tolerate return current, a series diode must be placed between the battery and the device in order to protect the battery.

40.11 NFCT timing parameters diagram

Illustrated here are the NFCT timing parameters.

Figure 116: NFCT timing parameters



40.12 References

NFC Forum, NFC Analog Specification version 1.0, www.nfc-forum.org

NFC Forum, NFC Digital Protocol Technical Specification version 1.1, www.nfc-forum.org

NFC Forum, NFC Activity Technical Specification version 1.1, www.nfc-forum.org

40.13 Registers

Table 93: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40005000	NFCT	NFCT	Near Field Communication Tag	

Table 94: Register Overview

Register	Offset	Description
TASKS_ACTIVATE	0x000	Activate NFC peripheral for incoming and outgoing frames, change state to activated
TASKS_DISABLE	0x004	Disable NFC peripheral
TASKS_SENSE	0x008	Enable NFC sense field mode, change state to sense mode
TASKS_STARTTX	0x00C	Start transmission of a outgoing frame, change state to transmit
TASKS_ENABLERXDATA	0x01C	Initializes the EasyDMA for receive.
TASKS_GOIDLE	0x024	Force state machine to IDLE state
TASKS_GOSLEEP	0x028	Force state machine to SLEEP_A state
EVENTS_READY	0x100	The NFC peripheral is ready to receive and send frames
EVENTS_FIELDDETECTED	0x104	Remote NFC field detected
EVENTS_FIELDLOST	0x108	Remote NFC field lost
EVENTS_TXFRAMESTART	0x10C	Marks the start of the first symbol of a transmitted frame
EVENTS_TXFRAMEEND	0x110	Marks the end of the last transmitted on-air symbol of a frame
EVENTS_RXFRAMESTART	0x114	Marks the end of the first symbol of a received frame
EVENTS_RXFRAMEEND	0x118	Received data have been checked (CRC, parity) and transferred to RAM, and EasyDMA has ended accessing the RX buffer
EVENTS_ERROR	0x11C	NFC error reported. The ERRORSTATUS register contains details on the source of the error.
EVENTS_RXERROR	0x128	NFC RX frame error reported. The FRAMESTATUS.RX register contains details on the source of the error.
EVENTS_ENDRX	0x12C	RX buffer (as defined by PACKETPTR and MAXLEN) in Data RAM full.
EVENTS_ENDTX	0x130	Transmission of data in RAM has ended, and EasyDMA has ended accessing the TX buffer
EVENTS_AUTOCOLRESST	0x138	Auto collision resolution process has started
EVENTS_COLLISION	0x148	NFC Auto collision resolution error reported.
EVENTS_SELECTED	0x14C	NFC Auto collision resolution successfully completed
EVENTS_STARTED	0x150	EasyDMA is ready to receive or send frames.
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt

Register	Offset	Description
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSTATUS	0x404	NFC Error Status register
FRAMESTATUS.RX	0x40C	Result of last incoming frames
CURRENTLOADCTRL	0x430	Current value driven to the NFC Load Control
FIELDPRESENT	0x43C	Indicates the presence or not of a valid field
FRAMEDELAYMIN	0x504	Minimum frame delay
FRAMEDELAYMAX	0x508	Maximum frame delay
FRAMEDELAYMODE	0x50C	Configuration register for the Frame Delay Timer
PACKETPTR	0x510	Packet pointer for TXD and RXD data storage in Data RAM
MAXLEN	0x514	Size of allocated for TXD and RXD data storage buffer in Data RAM
TXD.FRAMECONFIG	0x518	Configuration of outgoing frames
TXD.AMOUNT	0x51C	Size of outgoing frame
RXD.FRAMECONFIG	0x520	Configuration of incoming frames
RXD.AMOUNT	0x524	Size of last incoming frame
NFCID1_LAST	0x590	Last NFCID1 part (4, 7 or 10 bytes ID)
NFCID1_2ND_LAST	0x594	Second last NFCID1 part (7 or 10 bytes ID)
NFCID1_3RD_LAST	0x598	Third last NFCID1 part (10 bytes ID)
AUTOCOLRESCONFIG	0x59C	Controls the Auto collision resolution function. This setting must be done before the NFCT peripheral is enabled.
SENSRES	0x5A0	NFC-A SENS_RES auto-response settings
SELRES	0x5A4	NFC-A SEL_RES auto-response settings

40.13.1 SHORTS

Address offset: 0x200

Shortcut register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	FIELDDETECTED_ACTIVATE																																	
			Disabled	0																															
			Enabled	1																															
B	RW	FIELDLOST_SENSE																																	
			Disabled	0																															
			Enabled	1																															

40.13.2 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															T	S	R				N		M	L	K			H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	READY																																	
			Disabled	0																															
			Enabled	1																															
B	RW	FIELDDETECTED																																	
			Disabled	0																															
			Enabled	1																															
C	RW	FIELDLOST																																	
			Disabled	0																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															T	S	R				N		M	L	K			H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Enabled	1																															
D	RW	TXFRAMESTART																																	
			Disabled	0																															
			Enabled	1																															
E	RW	TXFRAMEEND																																	
			Disabled	0																															
			Enabled	1																															
F	RW	RXFRAMESTART																																	
			Disabled	0																															
			Enabled	1																															
G	RW	RXFRAMEEND																																	
			Disabled	0																															
			Enabled	1																															
H	RW	ERROR																																	
			Disabled	0																															
			Enabled	1																															
K	RW	RXERROR																																	
			Disabled	0																															
			Enabled	1																															
L	RW	ENDRX																																	
			Disabled	0																															
			Enabled	1																															
M	RW	ENDTX																																	
			Disabled	0																															
			Enabled	1																															
N	RW	AUTOCOLRESSTARTED																																	
			Disabled	0																															
			Enabled	1																															
R	RW	COLLISION																																	
			Disabled	0																															
			Enabled	1																															
S	RW	SELECTED																																	
			Disabled	0																															
			Enabled	1																															
T	RW	STARTED																																	
			Disabled	0																															
			Enabled	1																															

40.13.3 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															T	S	R				N		M	L	K			H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	READY																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	FIELDDETECTED																																	
			Set	1																															
			Disabled	0																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															T	S	R				N		M	L	K			H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Enabled	1																															
C	RW	FIELDLOST																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
D	RW	TXFRAMESTART																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
E	RW	TXFRAMEEND																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
F	RW	RXFRAMESTART																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
G	RW	RXFRAMEEND																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
H	RW	ERROR																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
K	RW	RXERROR																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
L	RW	ENDRX																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
M	RW	ENDTX																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
N	RW	AUTOCOLRESSTARTED																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
R	RW	COLLISION																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
S	RW	SELECTED																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
T	RW	STARTED																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															

40.13.4 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number					31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																T	S	R				N		M	L	K			H	G	F	E	D	C	B	A
Reset 0x00000000					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																															
A	RW	READY			Write '1' to Disable interrupt on *EVENTS_READY* event																																	
			Clear	1	Disable																																	
			Disabled	0	Read: Disabled																																	
			Enabled	1	Read: Enabled																																	
B	RW	FIELDDETECTED			Write '1' to Disable interrupt on *EVENTS_FIELDDETECTED* event																																	
			Clear	1	Disable																																	
			Disabled	0	Read: Disabled																																	
			Enabled	1	Read: Enabled																																	
C	RW	FIELDLOST			Write '1' to Disable interrupt on *EVENTS_FIELDLOST* event																																	
			Clear	1	Disable																																	
			Disabled	0	Read: Disabled																																	
			Enabled	1	Read: Enabled																																	
D	RW	TXFRAMESTART			Write '1' to Disable interrupt on *EVENTS_TXFRAMESTART* event																																	
			Clear	1	Disable																																	
			Disabled	0	Read: Disabled																																	
			Enabled	1	Read: Enabled																																	
E	RW	TXFRAMEEND			Write '1' to Disable interrupt on *EVENTS_TXFRAMEEND* event																																	
			Clear	1	Disable																																	
			Disabled	0	Read: Disabled																																	
			Enabled	1	Read: Enabled																																	
F	RW	RXFRAMESTART			Write '1' to Disable interrupt on *EVENTS_RXFRAMESTART* event																																	
			Clear	1	Disable																																	
			Disabled	0	Read: Disabled																																	
			Enabled	1	Read: Enabled																																	
G	RW	RXFRAMEEND			Write '1' to Disable interrupt on *EVENTS_RXFRAMEEND* event																																	
			Clear	1	Disable																																	
			Disabled	0	Read: Disabled																																	
			Enabled	1	Read: Enabled																																	
H	RW	ERROR			Write '1' to Disable interrupt on *EVENTS_ERROR* event																																	
			Clear	1	Disable																																	
			Disabled	0	Read: Disabled																																	
			Enabled	1	Read: Enabled																																	
K	RW	RXERROR			Write '1' to Disable interrupt on *EVENTS_RXERROR* event																																	
			Clear	1	Disable																																	
			Disabled	0	Read: Disabled																																	
			Enabled	1	Read: Enabled																																	
L	RW	ENDRX			Write '1' to Disable interrupt on *EVENTS_ENDRX* event																																	
			Clear	1	Disable																																	
			Disabled	0	Read: Disabled																																	
			Enabled	1	Read: Enabled																																	
M	RW	ENDTX			Write '1' to Disable interrupt on *EVENTS_ENDTX* event																																	
			Clear	1	Disable																																	
			Disabled	0	Read: Disabled																																	
			Enabled	1	Read: Enabled																																	
N	RW	AUTOCOLRESSTARTED			Write '1' to Disable interrupt on *EVENTS_AUTOCOLRESSTARTED* event																																	
			Clear	1	Disable																																	
			Disabled	0	Read: Disabled																																	
			Enabled	1	Read: Enabled																																	
R	RW	COLLISION			Write '1' to Disable interrupt on *EVENTS_COLLISION* event																																	

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id												T	S	R				N		M	L	K			H	G	F	E	D	C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
S	RW	SELECTED			Write '1' to Disable interrupt on *EVENTS_SELECTED* event
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
T	RW	STARTED			Write '1' to Disable interrupt on *EVENTS_STARTED* event
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

40.13.5 ERRORSTATUS

Address offset: 0x404

NFC Error Status register

Write a bit to '1' to clear it. Writing '0' has no effect.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																										G			D	C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	FRAMEDELAYTIMEOUT			No STARTTX task triggered before expiration of the time set in FRAMEDELAYMAX
B	RW	INVALIDNFCSYMBOL			The received pulse does not match a valid NFC-A symbol
C	RW	NFCFIELDTOOSTRONG			Field level is too high at max load resistance
D	RW	NFCFIELDTOOWEAK			Field level is too low at min load resistance
G	RW	EOFERROR			No valid End of Frame detected

40.13.6 FRAMESTATUS.RX

Address offset: 0x40C

Result of last incoming frames

Write a bit to '1' to clear it. Writing '0' has no effect.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																													C	B		A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	CRCERROR			No valid End of Frame detected
			CRCCorrect	0	Valid CRC detected
			CRCError	1	CRC received does not match local check
B	RW	PARITYSTATUS			Parity status of received frame
			ParityOK	0	Frame received with parity OK
			ParityError	1	Frame received with parity error
C	RW	OVERRUN			Overrun detected
			NoOverrun	0	No overrun detected
			Overrun	1	Overrun error

40.13.7 CURRENTLOADCTRL

Address offset: 0x430

Current value driven to the NFC Load Control

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																														A	A	A	A	A	A
Reset 0x00000008				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	CURRENTLOADCTRL																																	
				Current value driven to the NFC Load Control																																	

40.13.8 FIELDPRESENT

Address offset: 0x43C

Indicates the presence or not of a valid field

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	FIELDPRESENT																																	
				Indicates the presence or not of a valid field. Linked to the FIELDDETECTED and FIELDLOST events.																																	
			NoField	0																																	
				No valid field detected																																	
			FieldPresent	1																																	
				Valid field detected																																	
B	R	LOCKDETECT																																	
				Indicates if the low level has locked to the field																																	
			NotLocked	0																																	
				Not locked to field																																	
			Locked	1																																	
				Locked to field																																	

40.13.9 FRAMEDELAYMIN

Address offset: 0x504

Minimum frame delay

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000480				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	FRAMEDELAYMIN																																	
				Minimum frame delay in number of 13.56 MHz clocks																																	

40.13.10 FRAMEDELAYMAX

Address offset: 0x508

Maximum frame delay

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00001000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	FRAMEDELAYMAX																																	
				Maximum frame delay in number of 13.56 MHz clocks																																	

40.13.11 FRAMEDELAYMODE

Address offset: 0x50C

Configuration register for the Frame Delay Timer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		A	A
Reset 0x00000001				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	FRAMEDELAYMODE																																	
				Configuration register for the Frame Delay Timer																																	
			FreeRun	0																																	
				Transmission is independent of frame timer and will start when the STARTTX task is triggered. No timeout.																																	
			Window	1																																	
				Frame is transmitted between FRAMEDELAYMIN and FRAMEDELAYMAX																																	
			ExactVal	2																																	
				Frame is transmitted exactly at FRAMEDELAYMAX																																	

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		A	A
Reset 0x00000001				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			WindowGrid	3																															
				Frame is transmitted on a bit grid between FRAMEDELAYMIN and FRAMEDELAYMAX																															

40.13.12 PACKETPTR

Address offset: 0x510

Packet pointer for TXD and RXD data storage in Data RAM

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PTR																																	
				Packet pointer for TXD and RXD data storage in Data RAM. This address is a byte aligned RAM address.																															

40.13.13 MAXLEN

Address offset: 0x514

Size of allocated for TXD and RXD data storage buffer in Data RAM

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																											A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	MAXLEN		[0..257]																															
				Size of allocated for TXD and RXD data storage buffer in Data RAM																															

40.13.14 TXD.FRAMECONFIG

Address offset: 0x518

Configuration of outgoing frames

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															D		C	B	A
Reset 0x00000017				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PARITY																																	
				Adding parity or not in the frame																															
			NoParity	0																															
				Parity is not added in TX frames																															
			Parity	1																															
				Parity is added TX frames																															
B	RW	DISCARDMODE																																	
				Discarding unused bits in start or at end of a Frame																															
			DiscardEnd	0																															
				Unused bits is discarded at end of frame																															
			DiscardStart	1																															
				Unused bits is discarded at start of frame																															
C	RW	SOF																																	
				Adding SoF or not in TX frames																															
			NoSoF	0																															
				Start of Frame symbol not added																															
			SoF	1																															
				Start of Frame symbol added																															
D	RW	CRCMODETX																																	
				CRC mode for outgoing frames																															
			NoCRCTX	0																															
				CRC is not added to the frame																															
			CRC16TX	1																															
				16 bit CRC added to the frame based on all the data read from RAM that is used in the frame																															

40.13.15 TXD.AMOUNT

Address offset: 0x51C

Size of outgoing frame

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				B B B B B B B B A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	TXDATABITS		[0..7]	Number of bits in the last or first byte read from RAM that shall be included in the frame (excluding parity bit). The DISCARDMODE field in FRAMECONFIG.TX selects if unused bits is discarded at the start or at the end of a frame. A value of 0 bytes and 0 bits is invalid.
B	RW	TXDATABYTES		[0..257]	Number of complete bytes that shall be included in the frame, excluding CRC, parity and framing

40.13.16 RXD.FRAMECONFIG

Address offset: 0x520

Configuration of incoming frames

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				C B A
Reset 0x00000015				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 1**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	PARITY			Parity expected or not in RX frame
			NoParity	0	Parity is not expected in RX frames
			Parity	1	Parity is expected in RX frames
B	RW	SOF			SoF expected or not in RX frames
			NoSoF	0	Start of Frame symbol is not expected in RX frames
			SoF	1	Start of Frame symbol is expected in RX frames
C	RW	CRCMODERX			CRC mode for incoming frames
			NoCRCRX	0	CRC is not expected in RX frames
			CRC16RX	1	Last 16 bits in RX frame is CRC, CRC is checked and CRCSTATUS updated

40.13.17 RXD.AMOUNT

Address offset: 0x524

Size of last incoming frame

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				B B B B B B B B A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	R	RXDATABITS			Number of bits in the last byte in the frame, if less than 8 (including CRC, but excluding parity and SoF/EoF framing)
B	R	RXDATABYTES			Number of complete bytes received in the frame (including CRC, but excluding parity and SoF/EoF framing)

40.13.18 NFCID1_LAST

Address offset: 0x590

Last NFCID1 part (4, 7 or 10 bytes ID)

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				D D D D D D D D C C C C C C C C B B B B B B B B A A A A A A A A
Reset 0x00006363				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 1 1 0 1 1 0 0 0 1 1**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	NFCID1_Z			NFCID1 byte Z (very last byte sent)
B	RW	NFCID1_Y			NFCID1 byte Y
C	RW	NFCID1_X			NFCID1 byte X
D	RW	NFCID1_W			NFCID1 byte W

40.13.19 NFCID1_2ND_LAST

Address offset: 0x594

Second last NFCID1 part (7 or 10 bytes ID)

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id												C	C	C	C	C	C	C	C	B	B	B	B	B	B	B	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**								**Description**																							
A	RW	NFCID1_V										NFCID1 byte V																							
B	RW	NFCID1_U										NFCID1 byte U																							
C	RW	NFCID1_T										NFCID1 byte T																							

40.13.20 NFCID1_3RD_LAST

Address offset: 0x598

Third last NFCID1 part (10 bytes ID)

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id												C	C	C	C	C	C	C	C	B	B	B	B	B	B	B	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**								**Description**																							
A	RW	NFCID1_S										NFCID1 byte S																							
B	RW	NFCID1_R										NFCID1 byte R																							
C	RW	NFCID1_Q										NFCID1 byte Q																							

40.13.21 AUTOCOLRESCONFIG

Address offset: 0x59C

Controls the Auto collision resolution function. This setting must be done before the NFCT peripheral is enabled.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**								**Description**																							
A	RW	MODE										Enables/disables Auto collision resolution																							
			Enabled	0								Auto collision resolution enabled																							
			Disabled	1								Auto collision resolution disabled																							
B	RW	FILTER										Enables/disables Auto collision resolution short frame (any frames less than 7 bits) noise filter																							
			Off	0								Auto collision resolution short frame noise filter disabled																							
			On	1								Auto collision resolution ignores any frames less than 7 bits																							

40.13.22 SENSRES

Address offset: 0x5A0

NFC-A SENS_RES auto-response settings

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																				E	E	E	E	D	D	D	D	C	C	B	A	A	A	A
Reset 0x00000001				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**								**Description**																							
A	RW	BITFRAMESDD										Bit frame SDD as defined by the b5:b1 of byte 1 in SENS_RES response in the NFC Forum, NFC Digital Protocol Technical Specification																							
			SDD00000	0								SDD pattern 00000																							
			SDD00001	1								SDD pattern 00001																							
			SDD00010	2								SDD pattern 00010																							
			SDD00100	4								SDD pattern 00100																							

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																				E	E	E	E	D	D	D	D	C	C	B	A	A	A	A	A
Reset 0x00000001				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			SDD01000	8																															
			SDD10000	16																															
B	RW	RFU5																																	
C	RW	NFCIDSIZE																																	
			NFCID1Single	0																															
			NFCID1Double	1																															
			NFCID1Triple	2																															
D	RW	PLATFCONFIG																																	
E	RW	RFU74																																	

40.13.23 SELRES

Address offset: 0x5A4

NFC-A SEL_RES auto-response settings

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												E	D	D	C	C	B	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	RFU10																																	
B	RW	CASCADE																																	
			Complete	0																															
			NotComplete	1																															
C	RW	RFU43																																	
D	RW	PROTOCOL																																	
E	RW	RFU7																																	

40.14 Electrical Specification

40.14.1 NFCT Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
f_c	Frequency of operation		13.56		MHz
C_{MI}	Carrier modulation index		95		%
DR	Data Rate		106		kbps
f_s	Modulation sub-carrier frequency		f_c/16		MHz
V_{swing}	Peak differential Input voltage swing on NFC1 and NFC2	0.5*VDD		VDD	Vp
V_{sense}	Peak differential Field detect threshold level on NFC1-NFC2		0.9		Vp
$I_{fielddetect,sense}$	Current in SENSE STATE		100		nA
$I_{fielddetect,activated}$	Current in ACTIVATED STATE		400		uA
R_{in_min}	Minimum input resistance when regulating voltage swing			40	Ω
$R_{in\_min,Vhigh}$	Minimum input resistance when regulating voltage swing, VDD >2.4V			10	Ω
R_{in_max}	Maximum input resistance when regulating voltage swing	1			kΩ
$R_{in\_loadmod}$	Input resistance when load modulating	2		15	Ω
$R_{in\_loadmod,Vhigh}$	Input resistance when load modulating, VDD >2.4V	2		6	Ω
I_{max}	Maximum input current on NFC pins			80	mA

40.14.2 NFCT Timing Parameters

Symbol	Description	Min.	Typ.	Max.	Units
$t_{activate}$	Time from task_ACTIVATE in SENSE or DISABLE state to ACTIVATE_A or IDLE state[33]			500	us
t_{sense}	Time from remote field is present in SENSE mode to FIELDDETECTED event is asserted		2	20	us

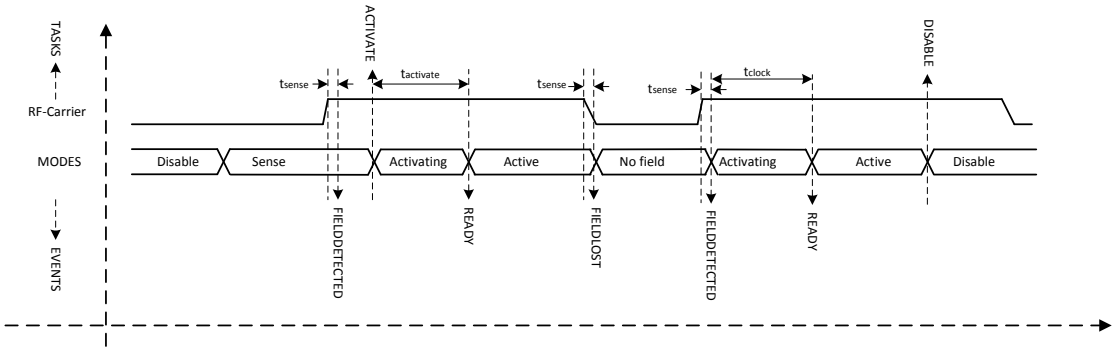


Figure 117: NFCT Power-up timing diagram

[33] Does not account for voltage supply and oscillator startup times

41 Pulse density modulation interface (PDM)

The PDM module enables input of pulse density modulated signals from external audio frontends, for example, digital microphones. The PDM module generates the PDM clock and support single channel or dual channel (Left and Right) data input. Data is transferred directly to RAM buffers using EasyDMA

Listed here are the main features for PDM:

- Up to two PDM microphones configured as a Left/Right pair using the same data input
- 16 kHz output sample rate, 16-bit samples
- EasyDMA support for sample buffering
- HW decimation filters

The PDM (Pulse density modulation) module illustrated in *Figure 118: PDM module* on page 418 is interfacing up to two digital microphones with PDM interface. It implements EasyDMA which relieves real-time requirements associated with controlling the PDM slave from a low priority CPU execution context. It also includes all the necessary digital filter elements to produce PCM samples. The PDM module allows continuous audio streaming.

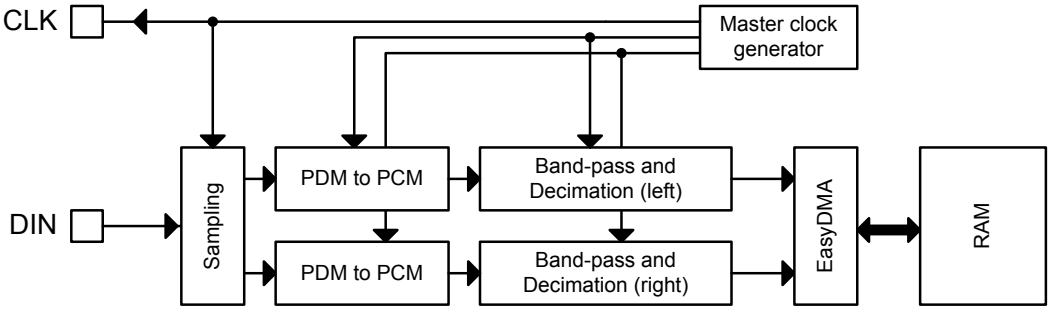


Figure 118: PDM module

41.1 Pin configuration

The CLK and DIN signals associated to the PDM module are mapped to physical pins according to the configuration specified in the PSEL.CLK and PSEL.DIN registers respectively. If the CONNECT field in any PSEL register is set to Disconnected, the associated PDM module signal will not be connected to that required physical pins, and will not operate properly.

The PSEL.CLK and PSEL.DIN registers and their configurations are only used as long as the PDM module is enabled, and retained only as long as the device is in System ON mode, see *Power management (POWER)* on page 79 for more information about power modes.

To ensure correct behaviour in the PDM module, the pins used by the PDM module must be configured in the GPIO peripheral as described in *Table 95: GPIO configuration* on page 418 before enabling the PDM module. This is to ensure that the pins used by the PDM module are driven correctly if the PDM module itself is temporarily disabled or the device temporarily enters system OFF. This configuration must be retained in the GPIO for the selected IOs as long as the PDM module is supposed to be connected to an external PDM circuit.

Only one peripheral can be assigned to drive a particular GPIO pin at a time, failing to do so may result in unpredictable behaviour.

Table 95: GPIO configuration

PDM signal	PDM pin	Direction	Function	Comment
CLK	As specified in PSEL.CLK	Output	Sample clock	
DIN	As specified in PSEL.DIN	Input	Data stream	

41.2 EasyDMA

Samples will be written directly to RAM, and EasyDMA must be configured accordingly.

The address pointer for the EasyDMA channel is set in SAMPLE.PTR register. If the destination address set in SAMPLE.PTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 34 for more information about the different memory regions.

DMA supports Stereo (Left+Right 16-bit samples) and Mono (Left only) data transfer, depending on setting in the CHANNELS field in the MODE register. The samples are stored little endian.

Table 96: DMA sample storage

MODE.CHANNELS	Bits per sample	Result stored per RAM word	Physical RAM allocated (32 bit words)	Result boundary indexes in RAM	Note
Stereo	32 (2x16)	L+R	SAMPLE.MAXCNT	R0=[31:16]; L0=[15:0]	Default
Mono	16	2xL	ceil(SAMPLE.MAXCNT/2)	L1=[31:16]; L0=[15:0]	

The destination buffer in RAM consists of one block, the size of which is set in SAMPLE.MAXCNT register. Format is number of samples. Physical RAM allocated for one block hence depends on the amount of samples per word. In Stereo mode, the total size of allocated RAM can be calculated as follows:

```
(RAM allocation, in bytes) = SAMPLE.MAXCNT * 4;
```

In Mono mode, the total size of allocated RAM can be calculated as follows:

```
(RAM allocation, in bytes) = SAMPLE.MAXCNT * 2
```

The PDM acquisition can be started by the START task, after the SAMPLE.PTR and SAMPLE.MAXCNT registers have been written. When starting the module, it will take some time for the filters to start outputting valid data. Transients from the PDM microphone itself may also occur. The first few samples (typically around 50) might hence contain invalid values or transients. It is hence advised to discard the first few samples after a PDM start.

As soon as the STARTED event is received, the firmware can write the next SAMPLE.PTR value (this register is double-buffered), to ensure continuous operation.

When the buffer in RAM is filled with samples, an END event is triggered. The firmware can start processing the data in the buffer. Meanwhile, the PDM module starts acquiring data into the new buffer pointed to by SAMPLE.PTR, and sends a new STARTED event, so that the firmware can update SAMPLE.PTR to the next buffer address.

41.3 Module operation

By default, bits from the left PDM microphone are sampled on PDM_CLK falling edge, bits for the right are sampled on the rising edge of PDM_CLK, resulting in two bitstreams. Each bitstream is fed into a digital filter which converts the Pulse Density Modulation stream into 16-bit PCM samples, and filters and down-samples them to reach the appropriate sample rate.

The EDGE field in the MODE register allows swapping Left and Right, so that Left will be sampled on rising edge, and Right on Falling.

The PDM module uses EasyDMA to store the samples coming out from the filters into one buffer in RAM.

Depending on the mode chosen in the CHANNELS field in the MODE register, memory either contains alternating left and right 16 bit samples (Stereo), or only left 16 bit samples (Mono).

To ensure continuous PDM sampling, it is up to the application to update the EasyDMA destination address pointer as the previous buffer is filled.

The continuous transfer can be started or stopped by sending the START and STOP tasks. STOP becomes effective after the current frame has finished transferring, which will generate the STOPPED event. The STOPPED event indicates that all activity in the module are finished, and that the data is available in RAM (EasyDMA has finished transferring as well). Attempting to restart before receiving the STOPPED event may result in unpredictable behaviour.

41.4 Hardware example

Connect the microphone clock to CLK, and data to DIN.

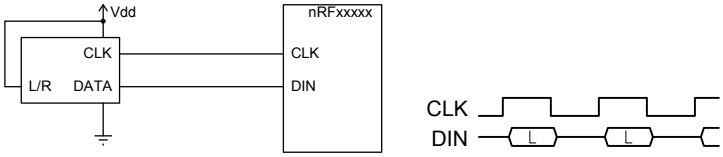


Figure 119: Example of a single PDM microphone, wired as left

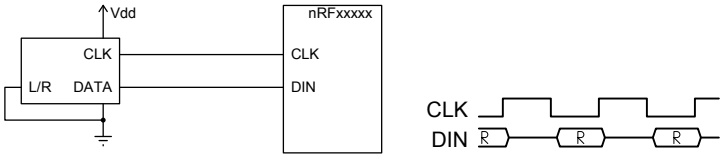


Figure 120: Example of a single PDM microphone, wired as right

Note that in a single-microphone (mono) configuration, depending on the microphone's implementation, either the left or the right channel (sampled at falling or rising CLK edge respectively) will contain reliable data. If two microphones are used, one of them has to be set as left, the other as right (L/R pin tied high or to GND on the respective microphone). It is strongly recommended to use two microphones of exactly the same brand and type so that their timings in left and right operation match.

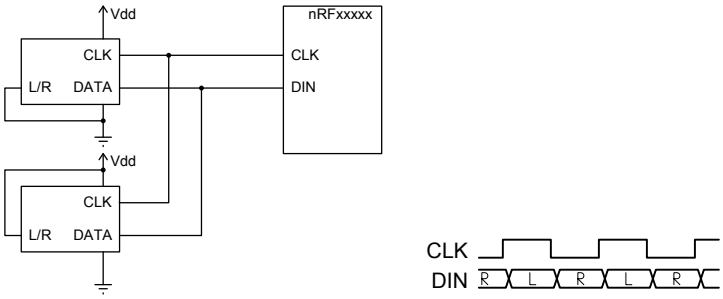


Figure 121: Example of two PDM microphones

41.5 Decimation filter

In order to convert the incoming data stream into PCM audio samples, a decimation filter is included in the PDM interface module.

The input of the filter is the two-channel PDM serial stream (with left channel on clock high, right channel on clock low), its output is 2 × 16-bit PCM samples at a sample rate 64 times lower than the PDM clock rate.

The filter stage of each channel is followed by a digital volume control, to attenuate or amplify the output samples in a range of -20 dB to +20 dB. The gain is controlled by the GAINL and GAINR registers.

41.6 Master clock generator

The FREQ field in the master clock's PDMCLKCTRL register allows adjusting the PDM clock's frequency.

41.7 Registers

Table 97: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4001D000	PDM	PDM	Pulse Density Modulation (Digital Microphone) Interface	

Table 98: Register Overview

Register	Offset	Description
TASKS_START	0x000	Starts continuous PDM transfer
TASKS_STOP	0x004	Stops PDM transfer
EVENTS_STARTED	0x100	PDM transfer has started
EVENTS_STOPPED	0x104	PDM transfer has finished
EVENTS_END	0x108	The PDM has written the last sample specified by SAMPLE.MAXCNT (or the last sample after a STOP task has been received) to Data RAM
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	PDM module enable register
PDMCLKCTRL	0x504	PDM clock generator control
MODE	0x508	Defines the routing of the connected PDM microphones' signals
GAINL	0x518	Left output gain adjustment
GAINR	0x51C	Right output gain adjustment
PSEL.CLK	0x540	Pin number configuration for PDM CLK signal
PSEL.DIN	0x544	Pin number configuration for PDM DIN signal
SAMPLE.PTR	0x560	RAM address pointer to write samples to with EasyDMA
SAMPLE.MAXCNT	0x564	Number of samples to allocate memory for in EasyDMA mode

41.7.1 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number																																
Id																														C	B	A
Reset 0x00000000									**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	STARTED			Enable or disable interrupt on *EVENTS_STARTED* event
			Disabled	0	Disable
			Enabled	1	Enable
B	RW	STOPPED			Enable or disable interrupt on *EVENTS_STOPPED* event
			Disabled	0	Disable
			Enabled	1	Enable
C	RW	END			Enable or disable interrupt on *EVENTS_END* event
			Disabled	0	Disable
			Enabled	1	Enable

41.7.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	STARTED																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	STOPPED																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	END																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															

41.7.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	STARTED																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	STOPPED																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	END																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															

41.7.4 ENABLE

Address offset: 0x500

PDM module enable register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	ENABLE																																	
			Disabled	0																															
			Enabled	1																															

41.7.5 PDMCLKCTRL

Address offset: 0x504

PDM clock generator control

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x08400000			**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																														
A	RW	FREQ																																
			Default	0x08400000																														

41.7.6 MODE

Address offset: 0x508

Defines the routing of the connected PDM microphones' signals

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																	B	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																														
A	RW	OPERATION																																
			Stereo	0																														
			Mono	1																														
B	RW	EDGE																																
			LeftFalling	0																														
			LeftRising	1																														

41.7.7 GAINL

Address offset: 0x518

Left output gain adjustment

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												A	A	A	A	A	A	A
Reset 0x00000028			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																														
A	RW	GAINL																																
			MinGain	0x00																														
			DefaultGain	0x28																														
			MaxGain	0x50																														

41.7.8 GAINR

Address offset: 0x51C

Right output gain adjustment

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A
Reset 0x00000028			**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0**
Id	**Value Id**	**Value**	**Description**
A			Right output gain adjustment, in 0.5 dB steps, around the requirement that 0dB gain adjustment corresponds to 2500 RMS output samples (16-bit) with 1 kHz 90dBA signal into a -26dBFS sensitivity PDM microphone. (same encoding as GAINL)
	MinGain	0x00	-20dB gain adjustment (minimum)
	DefaultGain	0x28	0dB gain adjustment ('2500 RMS' requirement)
	MaxGain	0x50	+20dB gain adjustment (maximum)

41.7.9 PSEL.CLK

Address offset: 0x540

Pin number configuration for PDM CLK signal

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			C A A A A A
Reset 0xFFFFFFFF			**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Id	**Value Id**	**Value**	**Description**
A		[0..31]	Pin number
C			Connection
	Disconnected	1	Disconnect
	Connected	0	Connect

41.7.10 PSEL.DIN

Address offset: 0x544

Pin number configuration for PDM DIN signal

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			C A A A A A
Reset 0xFFFFFFFF			**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Id	**Value Id**	**Value**	**Description**
A		[0..31]	Pin number
C			Connection
	Disconnected	1	Disconnect
	Connected	0	Connect

41.7.11 SAMPLE.PTR

Address offset: 0x560

RAM address pointer to write samples to with EasyDMA

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000			**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**Value Id**	**Value**	**Description**
A			Address to write PDM samples to over DMA

41.7.12 SAMPLE.MAXCNT

Address offset: 0x564

Number of samples to allocate memory for in EasyDMA mode

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	BUFFSIZE		[0..32767]	Length of DMA RAM allocation in number of samples. Number of RAM word allocated depends on MODE.CHANNELS.

41.8 Electrical Specification

41.8.1 PDM Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
$I_{PDM,mono}$	PDM module active current, mono operation		200		uA
$I_{PDM,stereo}$	PDM module active current, stereo operation		250		uA
$f_{PDM,CLK}$	PDM clock speed		1.032		MHz
$t_{PDM,JITTER}$	Jitter in PDM clock output			20	ns
$T_{dPDM,CLK}$	PDM clock duty cycle	40	50	60	%
$t_{PDM,DATA}$	Decimation filter delay			5	ms
$t_{PDM,cv}$	Allowed clock edge to data valid			125	ns
$t_{PDM,ci}$	Allowed (other) clock edge to data invalid	0			ns
$t_{PDM,s}$	Data setup time at $f_{PDM,CLK}$=1.024 MHz	363			ns
$t_{PDM,h}$	Data hold time at $f_{PDM,CLK}$=1.024 MHz	0			ns

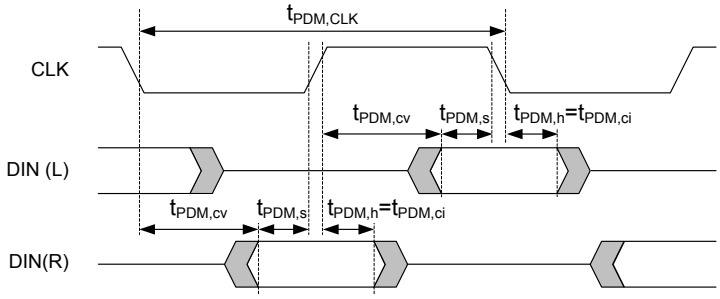


Figure 122: PDM timing diagram

42 Inter-IC sound (I2S) interface

The I2S (Inter-IC Sound) module, supports the original two-channel I2S format and common derived formats including (Digital Signal Processing) DSP. It implements EasyDMA for sample transfer directly to and from RAM without CPU intervention.

The I2S peripheral has the following main features:

- Master and Slave mode
- Simultaneous bi-directional (TX and RX) audio streaming
- Original I2S and DSP format
- 8, 16 and 24-bit sample width
- Low-jitter Master Clock generator
- Various sample rates

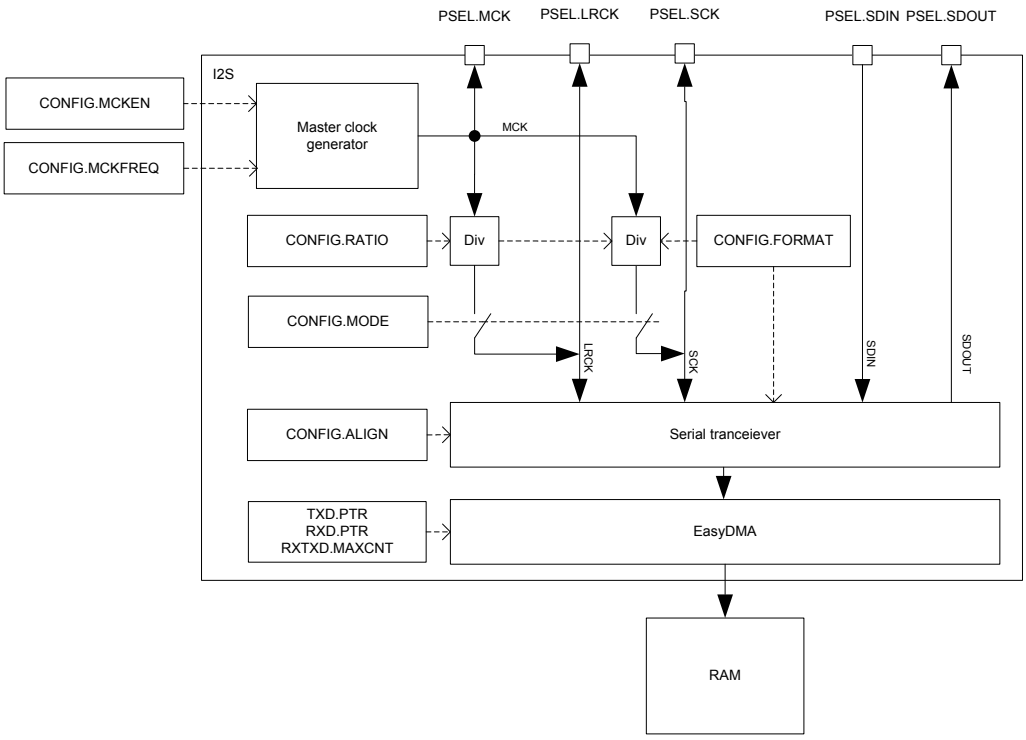


Figure 123: I2S master

42.1 Mode

The I2S protocol specification defines two modes of operation, Master and Slave.

The I2S mode decides which of the two sides (Master or Slave) shall provide the clock signals LRCK and SCK, and these signals are always supplied by the Master to the Slave.

42.2 Transmitting and receiving

The I2S module supports both transmission (TX) and reception (RX) of serial data. In both cases the serial data is shifted synchronously to the clock signals SCK and LRCK.

TX data is written to the SDOUT pin on the falling edge of SCK and RX data is read from the SDIN pin on the rising edge of SCK. The MSB is always transmitted first.

TX and RX are available in both Master and Slave modes and can be enabled/disabled independently in the CONFIG.TXEN and CONFIG.RXEN registers.

Transmission and/or reception is started by triggering the START task. When started and transmission is enabled (in the CONFIG.TXEN register), the TXPTRUPD event will be generated for every RXTXD.MAXCNT number of transmitted data words (containing one or more samples). Similarly, when started and reception is enabled (in the CONFIG.RXEN register), the RXPTRUPD event will be generated for every RXTXD.MAXCNT received data words.

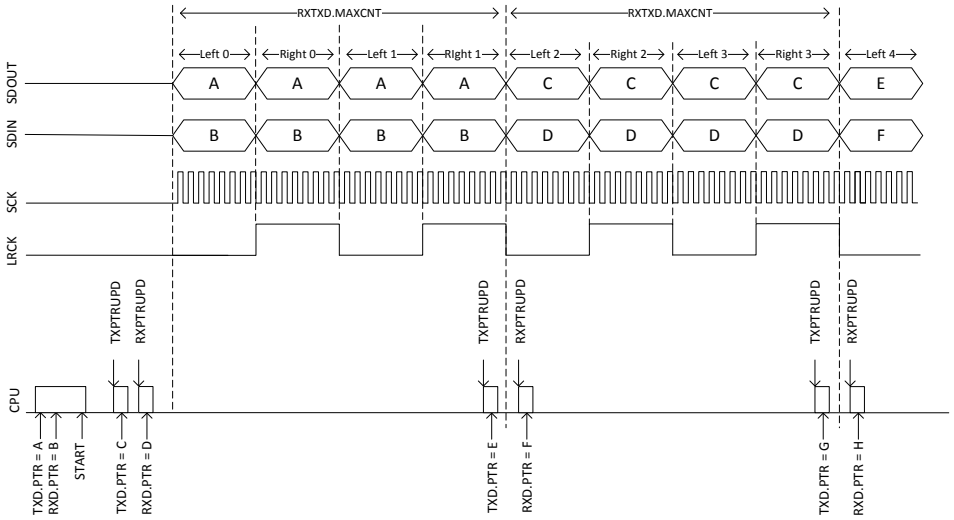


Figure 124: Transmitting and receiving. CONFIG.FORMAT = DSP, CONFIG.SWIDTH = 8BIT, CONFIG.CHANNELS = STEREO, RXTXD.MAXCNT = 1.

42.3 Left right clock (LRCK)

The Left Right Clock (LRCK), often referred to as "word clock", "sample clock" or "word select" in I2S context, is the clock defining the frames in the serial bit streams sent and received on SDOUT and SDIN, respectively.

Each frame contains one left and right sample pair, with the left sample being transferred during the low half period of LRCK followed by the right sample being transferred during the high period of LRCK.

Consequently, the LRCK frequency is equivalent to the audio sample rate.

When operating in Master mode the LRCK is generated from the MCK, and the frequency of LRCK is then given as:

```
LRCK = MCK / CONFIG.RATIO
```

LRCK always toggles around the falling edge of the serial clock SCK.

42.4 Serial clock (SCK)

The serial clock (SCK), often referred to as the serial bit clock, pulses once for each data bit being transferred on the serial data lines SDIN and SDOUT.

When operating in Master mode the SCK is generated from the MCK, and the frequency of SCK is then given as:

```
SCK = 2 * LRCK * CONFIG.SWIDTH
```

The falling edge of the SCK falls on the toggling edge of LRCK.

When operating in Slave mode SCK is provided by the external I2S master.

42.5 Master clock (MCK)

The Master Clock (MCK) is the clock from which LRCK and SCK are derived when operating in Master mode.

The MCK is generated by an internal MCK generator. This generator always needs to be enabled when in Master mode, but the generator can also be enabled when in Slave mode. Enabling the generator when in slave mode can be useful in the case where the external Master is not able to generate its own master clock.

The MCK generator is enabled/disabled in the CONFIG.MCKEN register, and the generator is started or stopped by the START or STOP tasks.

In Master mode the LRCK and the SCK frequencies are closely related, as both are derived from MCK and set indirectly through the CONFIG.RATIO and CONFIG.SWIDTH registers.

When configuring these register the user is responsible for fulfilling the following requirements:

1. SCK frequency can never exceed the MCK frequency, which can be formulated as:

```
CONFIG.RATIO >= 2 * CONFIG.SWIDTH
```

2. The MCK/LRCK ratio shall be a multiple of 2 * CONFIG.SWIDTH, which can be formulated as:

```
Integer = (CONFIG.RATIO / (2 * CONFIG.SWIDTH))
```

The MCK signal can be routed to an output pin (specified in PSEL.MCK) to supply external I2S devices that require the MCK to be supplied from the outside.

When operating in Slave mode the I2S module does not use the MCK and the MCK generator does not need to be enabled.

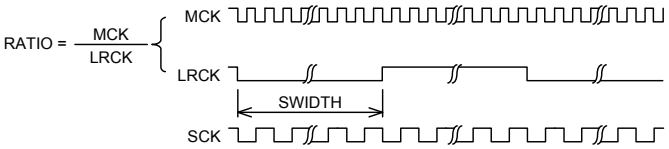


Figure 125: Relation between RATIO, MCK and LRCK.

Table 99: Configuration examples

Desired LRCK [Hz]	CONFIG.SWIDTH	CONFIG.RATIO	CONFIG.MCKFREQ	MCK [Hz]	LRCK [Hz]	LRCK error [%]
16000	16BIT	32X	32MDIV63	507936.5	15873.0	-0.8
16000	16BIT	64X	32MDIV31	1032258.1	16129.0	0.8
16000	16BIT	256X	32MDIV8	4000000.0	15625.0	-2.3
32000	16BIT	32X	32MDIV31	1032258.1	32258.1	0.8
32000	16BIT	64X	32MDIV16	2000000.0	31250.0	-2.3
32000	16BIT	256X	32MDIV4	8000000.0	31250.0	-2.3
44100	16BIT	32X	32MDIV23	1391304.3	43478.3	-1.4
44100	16BIT	64X	32MDIV11	2909090.9	45454.5	3.1
44100	16BIT	256X	32MDIV3	10666666.7	41666.7	-5.5

42.6 Width, alignment and format

The CONFIG.SWIDTH register primarily defines the sample width of the data written to memory. In master mode, it then also sets the amount of bits per frame. In Slave mode it controls padding / trimming if required.

Left, right, transmitted, and received samples always have the same width. The CONFIG.FORMAT register specifies the position of the data frames with respect to the LRCK edges in both Master and Slave modes.

When using I²S format, the first bit in a half-frame (containing one left or right sample) gets sampled on the second rising edge of the SCK after a LRCK edge. When using DSP mode, the first bit in a half-frame gets sampled on the first rising edge of SCK following a LRCK edge.

For data being received on SDIN the sample value can be either right- or left-aligned inside a half-frame, as specified in the CONFIG.ALIGN register. CONFIG.ALIGN affects only the decoding of the incoming samples (SDIN), while the outgoing samples (SDOUT) are always left-aligned (or justified).

When using left-alignment, each half-frame starts with the MSB of the sample value (both for data being sent on SDOUT and received on SDIN).

When using right-alignment, each half-frame of data being received on SDIN ends with the LSB of the sample value, while each half-frame of data being sent on SDOUT starts with the MSB of the sample value (same as for left-alignment).

In Master mode the size of a half-frame (in number of SCK periods) equals the sample width (in number of bits), and in this case the alignment setting does not care as each half-frame in any case will start with the MSB and end with the LSB of the sample value.

In slave mode, however, the sample width does not need to equal the frame size. This means you might have extra or fewer SCK pulses per half-frame than what the sample width specified in CONFIG.SWIDTH requires.

In the case where we use **left-alignment** and the number of SCK pulses per half-frame is **higher** than the sample width, the following will apply:

- For data received on SDIN, all bits after the LSB of the sample value will be discarded.
- For data sent on SDOUT, all bits after the LSB of the sample value will be 0.

In the case where we use **left-alignment** and the number of SCK pulses per frame is **lower** than the sample width, the following will apply:

- Data sent and received on SDOUT and SDIN will be truncated with the LSBs being removed first.

In the case where we use **right-alignment** and the number of SCK pulses per frame is **higher** than the sample width, the following will apply:

- For data received on SDIN, all bits before the MSB of the sample value will be discarded.
- For data sent on SDOUT, all bits after the LSB of the sample value will be 0 (same behavior as for left-alignment).

In the case where we use **right-alignment** and the number of SCK pulses per frame is **lower** than the sample width, the following will apply:

- Data received on SDIN will be sign extended to "sample width" number of bits before being written to memory.
- Data sent on SDOUT will be truncated with the LSBs being removed first (same behavior as for left-alignment).

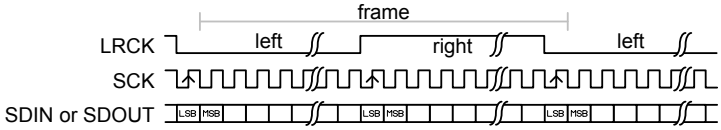


Figure 126: I²S format. CONFIG.SWIDTH equalling half-frame size.

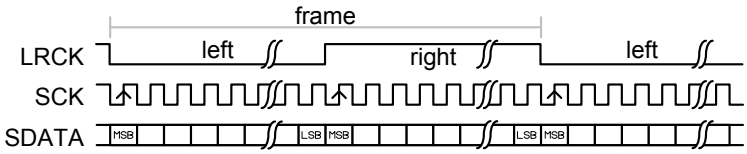


Figure 127: DSP format. CONFIG.SWIDTH equalling half-frame size.

42.7 Pin configuration

The signals MCK, SCK, LRCK, SDIN and SDOUT associated with the I2S module are mapped to physical pins according to the pin numbers specified in the PSEL.x registers. These pins are acquired whenever the I2S module is enabled through the ENABLE register.

When a pin is acquired by the I2S module the direction of the pin (input or output) will be configured automatically, and any pin direction setting done in the GPIO module will be overridden. The direction for the various I2S pins are shown in *Table 100: I2S pin direction* on page 430.

To secure correct signal levels on the pins when the system is in OFF mode, and when the I2S module is disabled, these pins must be configured in the GPIO peripheral directly.

Table 100: I2S pin direction

I2S pin	Direction (Master mode)	Direction (Slave mode)
PSEL.MCK	Output	Output
PSEL.LRCK	Output	Input
PSEL.SCK	Output	Input
PSEL.SDIN	Input	Input
PSEL.SDOUT	Output	Output

42.8 EasyDMA

The I2S module implements EasyDMA for accessing internal Data RAM without CPU intervention.

The source and destination pointers for the TX and RX data are configured in the TXD.PTR and RXD.PTR registers, respectively. The memory pointed to by these pointers will only be read or written when TX or RX are enabled in the CONFIG.TXEN and CONFIG.RXEN registers, respectively.

The addresses written to the pointer registers TXD.PTR and RXD.PTR are double buffered in hardware and these double buffers are updated for every RXTXD.MAXCNT words (containing one or more samples) read/written from/to memory. The events TXPTRUPD and RXPTRUPD are generated whenever the TXD.PTR and RXD.PTR are transferred to these double buffers.

If TXD.PTR is not pointing to the Data RAM region when transmission is enabled, or RXD.PTR is not pointing to the Data RAM region when reception is enabled, an EasyDMA transfer may result in a HardFault and/or memory corruption. See *Memory* on page 34 for more information about the different memory regions.

Due to the nature of I2S, where the number of transmitted samples always equals the number of received samples (at least when both TX and RX are enabled), one common register RXTXD.MAXCNT is used for specifying the sizes of these two memory buffers. The size of the buffers is specified in a number of 32-bit words. Such a 32-bit memory word can either contain four 8-bit samples, two 16-bit samples or one right-aligned 24-bit sample sign extended to 32 bit.

In stereo mode (decided by CONFIG.CHANNELS), the samples are stored as "left and right sample pairs" in memory. Figure *Figure 128: Memory mapping for 8-bit stereo. CONFIG.SWIDTH = 8BIT, CONFIG.CHANNELS = STEREO.* on page 431, *Figure 130: Memory mapping for 16 bit stereo. CONFIG.SWIDTH = 16BIT, CONFIG.CHANNELS = STEREO.* on page 431 and *Figure 132: Memory mapping for 24-bit stereo. CONFIG.SWIDTH = 24BIT, CONFIG.CHANNELS = STEREO.* on page 432 show how the samples are mapped to memory in this mode.

In mono mode (left or right channel only) samples for only one single channel are stored in memory. Figure *Figure 129: Memory mapping for 8-bit mono. CONFIG.SWIDTH = 8BIT, CONFIG.CHANNELS = LEFT.* on page 431, *Figure 131: Memory mapping for 16-bit mono, left channel only. CONFIG.SWIDTH = 16BIT, CONFIG.CHANNELS = LEFT.* on page 431 and *Figure 133: Memory mapping for 24-bit mono, left channel only. CONFIG.SWIDTH = 24BIT, CONFIG.CHANNELS = LEFT.* on page 432 show how samples are mapped to memory in this mode.

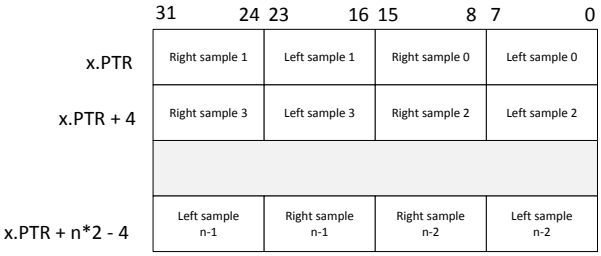


Figure 128: Memory mapping for 8-bit stereo. CONFIG.SWIDTH = 8BIT, CONFIG.CHANNELS = STEREO.

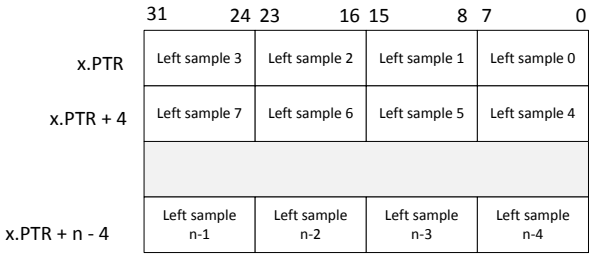


Figure 129: Memory mapping for 8-bit mono. CONFIG.SWIDTH = 8BIT, CONFIG.CHANNELS = LEFT.

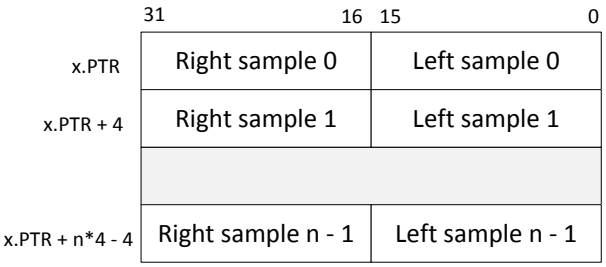


Figure 130: Memory mapping for 16 bit stereo. CONFIG.SWIDTH = 16BIT, CONFIG.CHANNELS = STEREO.

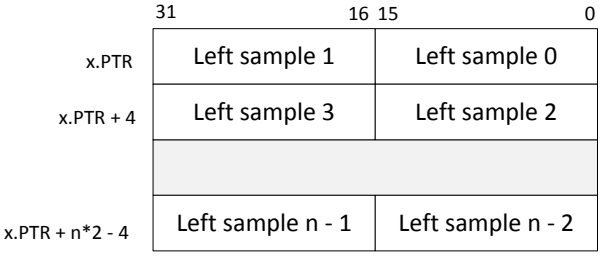


Figure 131: Memory mapping for 16-bit mono, left channel only. CONFIG.SWIDTH = 16BIT, CONFIG.CHANNELS = LEFT.

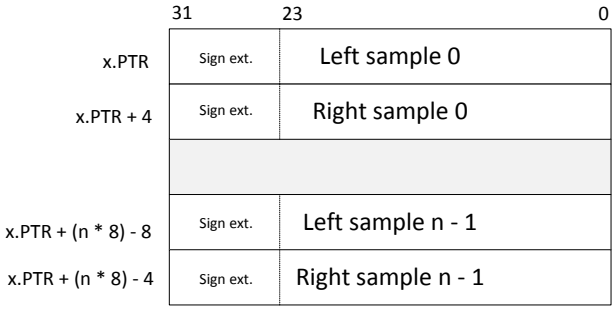


Figure 132: Memory mapping for 24-bit stereo. CONFIG.SWIDTH = 24BIT, CONFIG.CHANNELS = STEREO.

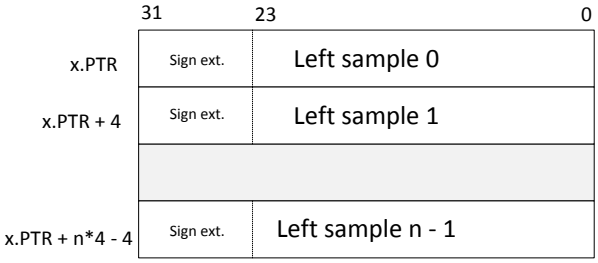


Figure 133: Memory mapping for 24-bit mono, left channel only. CONFIG.SWIDTH = 24BIT, CONFIG.CHANNELS = LEFT.

42.9 Module operation

Described here is a typical operating procedure for the I²S module.

1. Configure the I²S module using the CONFIG registers

```
NRF_I2S->CONFIG.RXEN = 1; // Enable reception
NRF_I2S->CONFIG.TXEN = 1; // Enable transmission
NRF_I2S->CONFIG.MCKEN = 1; // Enable MCK generator
NRF_I2S->CONFIG.MCKFREQ = 0x20000000; // MCKFREQ = 4 MHz
NRF_I2S->CONFIG.RATIO = 6; // Ratio = 256
// MCKFREQ = 4 MHz and Ratio = 256 gives sample rate = 15.625 ks/s
NRF_I2S->CONFIG.SWIDTH = 1; // Sample width = 16 bit
NRF_I2S->CONFIG.ALIGN = 0; // Alignment = Left
NRF_I2S->CONFIG.FORMAT = 0; // Format = I2S
NRF_I2S->CONFIG.CHANNELS = 0; // Use stereo
```

2. Map IO pins using the PINSEL registers

```
NRF_I2S->PSEL.MCK = 0;  // MCK routed to pin 0
NRF_I2S->PSEL.SCK = 1; // SCK routed to pin 1
NRF_I2S->PSEL.LRCK = 2; // LRCK routed to pin 2
NRF_I2S->PSEL.SDOUT = 3; // SDOUT routed to pin 3
NRF_I2S->PSEL.SDIN = 4; // SDIN routed on pin 4
```

3. Configure TX and RX data pointers using the TXD, RXD and RXTXD registers

```
NRF_I2S->TXD.PTR = my_tx_buf;
NRF_I2S->RXD.PTR = my_rx_buf;
NRF_I2S->TXD.MAXCNT = MY_BUF_SIZE;
```

4. Enable the I²S module using the ENABLE register

```
NRF_I2S->ENABLE = 1;
```

5. Start audio streaming using the START task

```
NRF_I2S->TASKS_START = 1;
```

6. Handle received and transmitted data when receiving the TXPTRUPD and RXPTRUPD events

```
if(NRF_I2S->EVENTS_TXPTRUPD  != 0)
{
    NRF_I2S->TXD.PTR = my_next_tx_buf;
    NRF_I2S->EVENTS_TXPTRUPD = 0;
}

if(NRF_I2S->EVENTS_RXPTRUPD != 0)
{
    NRF_I2S->RXD.PTR = my_next_rx_buf;
    NRF_I2S->EVENTS_RXPTRUPD = 0;
}
```

42.10 Registers

Table 101: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40025000	I2S	I2S	Inter-IC Sound interface	

Table 102: Register Overview

Register	Offset	Description
TASKS_START	0x000	Starts continuous I²S transfer. Also starts MCK generator when this is enabled.
TASKS_STOP	0x004	Stops I²S transfer. Also stops MCK generator. Triggering this task will cause the {event:STOPPED} event to be generated.
EVENTS_RXPTRUPD	0x104	The RXD.PTR register has been copied to internal double-buffers. When the I2S module is started and RX is enabled, this event will be generated for every RXTXD.MAXCNT words that are received on the SDIN pin.
EVENTS_STOPPED	0x108	I²S transfer stopped.
EVENTS_TXPTRUPD	0x114	The TDX.PTR register has been copied to internal double-buffers. When the I2S module is started and TX is enabled, this event will be generated for every RXTXD.MAXCNT words that are sent on the SDOUT pin.
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	Enable I²S module.
CONFIG.MODE	0x504	I²S mode.
CONFIG.RXEN	0x508	Reception (RX) enable.
CONFIG.TXEN	0x50C	Transmission (TX) enable.
CONFIG.MCKEN	0x510	Master clock generator enable.
CONFIG.MCKFREQ	0x514	Master clock generator frequency.
CONFIG.RATIO	0x518	MCK / LRCK ratio.

Register	Offset	Description
CONFIG.SWIDTH	0x51C	Sample width.
CONFIG.ALIGN	0x520	Alignment of sample within a frame.
CONFIG.FORMAT	0x524	Frame format.
CONFIG.CHANNELS	0x528	Enable channels.
RXD.PTR	0x538	Receive buffer RAM start address.
TXD.PTR	0x540	Transmit buffer RAM start address.
RXTXD.MAXCNT	0x550	Size of RXD and TXD buffers.
PSEL.MCK	0x560	Pin select for MCK signal.
PSEL.SCK	0x564	Pin select for SCK signal.
PSEL.LRCK	0x568	Pin select for LRCK signal.
PSEL.SDIN	0x56C	Pin select for SDIN signal.
PSEL.SDOUT	0x570	Pin select for SDOUT signal.

42.10.1 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																											F				C	B	
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
B	RW	RXPTRUPD			Enable or disable interrupt on EVENTS_RXPTRUPD event
			Disabled	0	Disable
			Enabled	1	Enable
C	RW	STOPPED			Enable or disable interrupt on EVENTS_STOPPED event
			Disabled	0	Disable
			Enabled	1	Enable
F	RW	TXPTRUPD			Enable or disable interrupt on EVENTS_TXPTRUPD event
			Disabled	0	Disable
			Enabled	1	Enable

42.10.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																											F				C	B	
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
B	RW	RXPTRUPD			Write '1' to Enable interrupt on EVENTS_RXPTRUPD event
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
C	RW	STOPPED			Write '1' to Enable interrupt on EVENTS_STOPPED event
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW	TXPTRUPD			Write '1' to Enable interrupt on EVENTS_TXPTRUPD event
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

42.10.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			F C B
Reset 0x00000000			**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

Id	RW	Field	Value Id	Value	Description
B	RW	RXPTRUPD			Write '1' to Disable interrupt on *EVENTS_RXPTRUPD* event
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
C	RW	STOPPED			Write '1' to Disable interrupt on *EVENTS_STOPPED* event
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW	TXPTRUPD			Write '1' to Disable interrupt on *EVENTS_TXPTRUPD* event
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

42.10.4 ENABLE

Address offset: 0x500

Enable I²S module.

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A
Reset 0x00000000			**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

Id	RW	Field	Value Id	Value	Description
A	RW	ENABLE			Enable I²S module.
			DISABLE	0	Disabl
			ENABLE	1	Enable

42.10.5 CONFIG.MODE

Address offset: 0x504

I²S mode.

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A
Reset 0x00000000			**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

Id	RW	Field	Value Id	Value	Description
A	RW	MODE			I²S mode.
			MASTER	0	Master mode. SCK and LRCK generated from internal master clcok (MCK) and output on pins defined by PSEL.xxx.
			SLAVE	1	Slave mode. SCK and LRCK generated by external master and received on pins defined by PSEL.xxx

42.10.6 CONFIG.RXEN

Address offset: 0x508

Reception (RX) enable.

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A
Reset 0x00000000			**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

Id	RW	Field	Value Id	Value	Description
A	RW	RXEN			Reception (RX) enable.
			DISABLE	0	Reception disabled and now data will be written to the RXD.PTR address.
			ENABLE	1	Reception enabled.

42.10.7 CONFIG.TXEN

Address offset: 0x50C

Transmission (TX) enable.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000001				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	TXEN																																	
			DISABLE	0																															
			ENABLE	1																															

42.10.8 CONFIG.MCKEN

Address offset: 0x510

Master clock generator enable.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			A
Reset 0x00000001				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	MCKEN																																	
			DISABLE	0																															
			ENABLE	1																															

42.10.9 CONFIG.MCKFREQ

Address offset: 0x514

Master clock generator frequency.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x20000000				**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	MCKFREQ																																	
			32MDIV2	0x80000000																															
			32MDIV3	0x50000000																															
			32MDIV4	0x40000000																															
			32MDIV5	0x30000000																															
			32MDIV6	0x28000000																															
			32MDIV8	0x20000000																															
			32MDIV10	0x18000000																															
			32MDIV11	0x16000000																															
			32MDIV15	0x11000000																															
			32MDIV16	0x10000000																															
			32MDIV21	0x0C000000																															
			32MDIV23	0x0B000000																															
			32MDIV31	0x08200000																															
			32MDIV42	0x06000000																															
			32MDIV63	0x04100000																															
			32MDIV125	0x020C0000																															

42.10.10 CONFIG.RATIO

Address offset: 0x518

MCK / LRCK ratio.

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															A	A	A	A
Reset 0x00000006			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	RW	RATIO																									MCK / LRCK ratio.							
			32X								0																LRCK = MCK / 32							
			48X								1																LRCK = MCK / 48							
			64X								2																LRCK = MCK / 64							
			96X								3																LRCK = MCK / 96x							
			128X								4																LRCK = MCK / 128							
			192X								5																LRCK = MCK / 192							
			256X								6																LRCK = MCK / 256							
			384X								7																LRCK = MCK / 384							
			512X								8																LRCK = MCK / 512							

42.10.11 CONFIG.SWIDTH

Address offset: 0x51C

Sample width.

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																	A	A
Reset 0x00000001			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	RW	SWIDTH																									Sample width.							
			8BIT								0																8 bit.							
			16BIT								1																16 bit.							
			24BIT								2																24 bit.							

42.10.12 CONFIG.ALIGN

Address offset: 0x520

Alignment of sample within a frame.

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	RW	ALIGN																									Alignment of sample within a frame.							
			LEFT								0																Left-aligned.							
			RIGHT								1																Right-aligned.							

42.10.13 CONFIG.FORMAT

Address offset: 0x524

Frame format.

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	RW	FORMAT																									Frame format.							
			I2S								0																Original I²S format.							
			DSP								1																Alternate (DSP) format.							

42.10.14 CONFIG.CHANNELS

Address offset: 0x528

Enable channels.

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A
Reset 0x00000000			**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

Id	RW	Field	Value Id	Value	Description
A	RW	CHANNELS			Enable channels.
			STEREO	0	Stereo.
			LEFT	1	Left only.
			RIGHT	2	Right only.

42.10.15 RXD.PTR

Address offset: 0x538

Receive buffer RAM start address.

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000			**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

Id	RW	Field	Value Id	Value	Description
A	RW	PTR			Receive buffer Data RAM start address. When receiving, words containing samples will be written to this address. This address is a word aligned Data RAM address.

42.10.16 TXD.PTR

Address offset: 0x540

Transmit buffer RAM start address.

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000			**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

Id	RW	Field	Value Id	Value	Description
A	RW	PTR			Transmit buffer Data RAM start address. When transmitting, words containing samples will be fetched from this address. This address is a word aligned Data RAM address.

42.10.17 RXTXD.MAXCNT

Address offset: 0x550

Size of RXD and TXD buffers.

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A A A A A A A A
Reset 0x00000000			**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

Id	RW	Field	Value Id	Value	Description
A	RW	MAXCNT			Size of RXD and TXD buffers in number of 32 bit words.

42.10.18 PSEL.MCK

Address offset: 0x560

Pin select for MCK signal.

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			C A A A A
Reset 0xFFFFFFFF			**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**

Id	RW	Field	Value Id	Value	Description
A	RW	PIN		[0..31]	Pin number
C	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

42.10.19 PSEL.SCK

Address offset: 0x564

Pin select for SCK signal.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				C																											A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PIN		[0..31]																															
C	RW	CONNECT																																	
			Disconnected	1																															
			Connected	0																															

42.10.20 PSEL.LRCK

Address offset: 0x568

Pin select for LRCK signal.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				C																											A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PIN		[0..31]																															
C	RW	CONNECT																																	
			Disconnected	1																															
			Connected	0																															

42.10.21 PSEL.SDIN

Address offset: 0x56C

Pin select for SDIN signal.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				C																											A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PIN		[0..31]																															
C	RW	CONNECT																																	
			Disconnected	1																															
			Connected	0																															

42.10.22 PSEL.SDOUT

Address offset: 0x570

Pin select for SDOUT signal.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				C																											A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PIN		[0..31]																															
C	RW	CONNECT																																	
			Disconnected	1																															
			Connected	0																															

42.11 Electrical Specification

42.11.1 "I2S timing specification"

Symbol	Description	Min.	Typ.	Max.	Units
t_{S_SDIN}	SDIN setup time before SCK rising	20			ns
t_{H_SDIN}	SDIN hold time after SCK rising	30			ns
t_{S_SDOUT}	SDOUT setup time after SCK falling	10			ns
t_{H_SDOUT}	SDOUT hold time before SCK falling	0			ns
t_{SCK_LRCK}	SCLK falling to LRCK edge	-10	0	10	ns
f_{MCK}	MCK frequency			4000	kHz
f_{LRCK}	LRCK frequency			48	kHz
f_{SCK}	SCK frequency			2000	kHz
DEV_{MCK}	MCK generator frequency deviation				%
DC_{CK}	Clock duty cycle (MCK, LRCK, SCK)	45		55	%

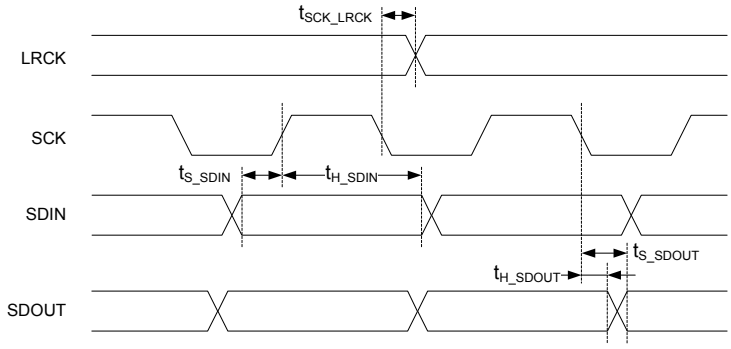


Figure 134: I2S timing diagram

43 Memory watch unit (MWU)

The Memory watch unit (MWU) can be used to generate events when a memory region is accessed by the CPU via read, write or both read and write. The MWU can be configured to trigger events for access to SRAM and Peripheral memory segments. The MWU allows an application developer to generate memory access events during development for debugging or during production execution for failure detection and recovery.

Listed here are the main features for MWU:

- Six memory regions, four user-configurable and two fixed regions in peripheral address space
- Flexible configuration of regions with START and END addresses
- Generate events on CPU read and/or write to a defined region of SRAM or peripheral memory address space
- Programmable maskable or non-maskable (NMI) interrupt on events
- Peripheral interfaces can be watched for read and write access using subregions of the two fixed memory regions

Table 103: Memory regions

Memory region	START address	END address
REGION[0..3]	Configurable	Configurable
PREGION[0]	0x40000000	0x4001FFFF
PREGION[1]	0x40020000	0x4003FFFF

Each MWU region is defined by a start address and an end address, configured by the START and END registers respectively. Only word addresses are allowed in START and END. The END register value has to be greater or equal to the START register value. If it is smaller, the operation of the MWU is undefined. If the END register value is zero or equal to the START value, the region is one byte long relative to the start address. Each region is associated with a pair of events that indicate that either a write access or a read access from the CPU has been detected inside the region.

For regions containing sub regions (see below), a set of status registers PERREGION[0..1].SUBSTATWA and PERREGION[0..1].SUBSTATRA indicate which subregion(s) caused the EVENT_PREGION[0..1].WA and EVENT_PREGION[0..1].RA respectively.

The MWU is only able to detect memory accesses in the SRAM and Peripheral memory segments from the CPU, see *Memory* on page 34 for more information about the different memory segments. EasyDMA accesses are not monitored by the MWU. The MWU requires two HCLK cycles to detect and generate the event.

The peripheral regions, PREGION[0...1], are divided into 32 equally sized subregions, SR[0...31]. All subregions are excluded in the main region by default, and any can be included by specifying them in the SUBS register. When a subregion is excluded from the main region, the memory watch mechanism will not trigger any events when that subregion is accessed.

Subregions in PREGION[0..1] cannot be individually configured for read or write access watch. Watch configuration is only possible for a region as a whole. The PRGNiRA and PRGNiWA (i=0..1) fields in the REGIONEN register control watching read and write access.

REGION[0..3] can be individually enabled for read and/or write access watching through their respective RGNiRA and RGNiWA (i=0..3) fields in the REGIONEN register.

REGIONENSET and REGIONENCLR allow respectively enabling and disabling one or multiple REGIONs or PREGIONs watching in a single write access.

43.1 Registers

Table 104: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40020000	MWU	MWU	Memory Watch Unit	

Table 105: Register Overview

Register	Offset	Description
EVENTS_REGION[0].WA	0x100	Write access to region 0 detected
EVENTS_REGION[0].RA	0x104	Read access to region 0 detected
EVENTS_REGION[1].WA	0x108	Write access to region 1 detected
EVENTS_REGION[1].RA	0x10C	Read access to region 1 detected
EVENTS_REGION[2].WA	0x110	Write access to region 2 detected
EVENTS_REGION[2].RA	0x114	Read access to region 2 detected
EVENTS_REGION[3].WA	0x118	Write access to region 3 detected
EVENTS_REGION[3].RA	0x11C	Read access to region 3 detected
EVENTS_PREGION[0].WA	0x160	Write access to peripheral region 0 detected
EVENTS_PREGION[0].RA	0x164	Read access to peripheral region 0 detected
EVENTS_PREGION[1].WA	0x168	Write access to peripheral region 1 detected
EVENTS_PREGION[1].RA	0x16C	Read access to peripheral region 1 detected
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
NMIEN	0x320	Enable or disable non-maskable interrupt
NMIENSET	0x324	Enable non-maskable interrupt
NMIENCLR	0x328	Disable non-maskable interrupt
PERREGION[0].SUBSTAT\	0x400	Source of interrupt in region 0, write access detected while corresponding subregion was enabled for watching
PERREGION[0].SUBSTATI	0x404	Source of interrupt in region 0, read access detected while corresponding subregion was enabled for watching
PERREGION[1].SUBSTAT\	0x408	Source of interrupt in region 1, write access detected while corresponding subregion was enabled for watching
PERREGION[1].SUBSTATI	0x40C	Source of interrupt in region 1, read access detected while corresponding subregion was enabled for watching
REGIONEN	0x510	Enable/disable regions watch
REGIONENSET	0x514	Enable regions watch
REGIONENCLR	0x518	Disable regions watch
REGION[0].START	0x600	Start address for region 0
REGION[0].END	0x604	End address of region 0
REGION[1].START	0x610	Start address for region 1
REGION[1].END	0x614	End address of region 1
REGION[2].START	0x620	Start address for region 2
REGION[2].END	0x624	End address of region 2
REGION[3].START	0x630	Start address for region 3
REGION[3].END	0x634	End address of region 3
PREGION[0].START	0x6C0	Reserved for future use
PREGION[0].END	0x6C4	Reserved for future use
PREGION[0].SUBS	0x6C8	Sub regions of region 0
PREGION[1].START	0x6D0	Reserved for future use
PREGION[1].END	0x6D4	Reserved for future use
PREGION[1].SUBS	0x6D8	Sub regions of region 1

43.1.1 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id								L	K	J	I																	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
A	RW	REGION0WA																										Enable or disable interrupt on *EVENTS_REGION[0].WA* event							
			Disabled	0																								Disable							
			Enabled	1																								Enable							
B	RW	REGION0RA																										Enable or disable interrupt on *EVENTS_REGION[0].RA* event							
			Disabled	0																								Disable							
			Enabled	1																								Enable							
C	RW	REGION1WA																										Enable or disable interrupt on *EVENTS_REGION[1].WA* event							
			Disabled	0																								Disable							
			Enabled	1																								Enable							
D	RW	REGION1RA																										Enable or disable interrupt on *EVENTS_REGION[1].RA* event							
			Disabled	0																								Disable							
			Enabled	1																								Enable							
E	RW	REGION2WA																										Enable or disable interrupt on *EVENTS_REGION[2].WA* event							
			Disabled	0																								Disable							
			Enabled	1																								Enable							
F	RW	REGION2RA																										Enable or disable interrupt on *EVENTS_REGION[2].RA* event							
			Disabled	0																								Disable							
			Enabled	1																								Enable							
G	RW	REGION3WA																										Enable or disable interrupt on *EVENTS_REGION[3].WA* event							
			Disabled	0																								Disable							
			Enabled	1																								Enable							
H	RW	REGION3RA																										Enable or disable interrupt on *EVENTS_REGION[3].RA* event							
			Disabled	0																								Disable							
			Enabled	1																								Enable							
I	RW	PREGION0WA																										Enable or disable interrupt on *EVENTS_PREGION[0].WA* event							
			Disabled	0																								Disable							
			Enabled	1																								Enable							
J	RW	PREGION0RA																										Enable or disable interrupt on *EVENTS_PREGION[0].RA* event							
			Disabled	0																								Disable							
			Enabled	1																								Enable							
K	RW	PREGION1WA																										Enable or disable interrupt on *EVENTS_PREGION[1].WA* event							
			Disabled	0																								Disable							
			Enabled	1																								Enable							
L	RW	PREGION1RA																										Enable or disable interrupt on *EVENTS_PREGION[1].RA* event							
			Disabled	0																								Disable							
			Enabled	1																								Enable							

43.1.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id								L	K	J	I																	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
A	RW	REGION0WA																										Write '1' to Enable interrupt on *EVENTS_REGION[0].WA* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
B	RW	REGION0RA																										Write '1' to Enable interrupt on *EVENTS_REGION[0].RA* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
C	RW	REGION1WA																										Write '1' to Enable interrupt on *EVENTS_REGION[1].WA* event							

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id								L	K	J	I																	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
D	RW	REGION1RA																										Write '1' to Enable interrupt on *EVENTS_REGION[1].RA* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
E	RW	REGION2WA																										Write '1' to Enable interrupt on *EVENTS_REGION[2].WA* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
F	RW	REGION2RA																										Write '1' to Enable interrupt on *EVENTS_REGION[2].RA* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
G	RW	REGION3WA																										Write '1' to Enable interrupt on *EVENTS_REGION[3].WA* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
H	RW	REGION3RA																										Write '1' to Enable interrupt on *EVENTS_REGION[3].RA* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
I	RW	PREGION0WA																										Write '1' to Enable interrupt on *EVENTS_PREGION[0].WA* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
J	RW	PREGION0RA																										Write '1' to Enable interrupt on *EVENTS_PREGION[0].RA* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
K	RW	PREGION1WA																										Write '1' to Enable interrupt on *EVENTS_PREGION[1].WA* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
L	RW	PREGION1RA																										Write '1' to Enable interrupt on *EVENTS_PREGION[1].RA* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							

43.1.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id								L	K	J	I																	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
A	RW	REGION0WA																										Write '1' to Disable interrupt on *EVENTS_REGION[0].WA* event							
			Clear	1																								Disable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
B	RW	REGION0RA																										Write '1' to Disable interrupt on *EVENTS_REGION[0].RA* event							
			Clear	1																								Disable							

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id								L	K	J	I																	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**								**Description**																							
			Disabled	0								Read: Disabled																							
			Enabled	1								Read: Enabled																							
C	RW	REGION1WA										Write '1' to Disable interrupt on *EVENTS_REGION[1].WA* event																							
			Clear	1								Disable																							
			Disabled	0								Read: Disabled																							
			Enabled	1								Read: Enabled																							
D	RW	REGION1RA										Write '1' to Disable interrupt on *EVENTS_REGION[1].RA* event																							
			Clear	1								Disable																							
			Disabled	0								Read: Disabled																							
			Enabled	1								Read: Enabled																							
E	RW	REGION2WA										Write '1' to Disable interrupt on *EVENTS_REGION[2].WA* event																							
			Clear	1								Disable																							
			Disabled	0								Read: Disabled																							
			Enabled	1								Read: Enabled																							
F	RW	REGION2RA										Write '1' to Disable interrupt on *EVENTS_REGION[2].RA* event																							
			Clear	1								Disable																							
			Disabled	0								Read: Disabled																							
			Enabled	1								Read: Enabled																							
G	RW	REGION3WA										Write '1' to Disable interrupt on *EVENTS_REGION[3].WA* event																							
			Clear	1								Disable																							
			Disabled	0								Read: Disabled																							
			Enabled	1								Read: Enabled																							
H	RW	REGION3RA										Write '1' to Disable interrupt on *EVENTS_REGION[3].RA* event																							
			Clear	1								Disable																							
			Disabled	0								Read: Disabled																							
			Enabled	1								Read: Enabled																							
I	RW	PREGION0WA										Write '1' to Disable interrupt on *EVENTS_PREGION[0].WA* event																							
			Clear	1								Disable																							
			Disabled	0								Read: Disabled																							
			Enabled	1								Read: Enabled																							
J	RW	PREGION0RA										Write '1' to Disable interrupt on *EVENTS_PREGION[0].RA* event																							
			Clear	1								Disable																							
			Disabled	0								Read: Disabled																							
			Enabled	1								Read: Enabled																							
K	RW	PREGION1WA										Write '1' to Disable interrupt on *EVENTS_PREGION[1].WA* event																							
			Clear	1								Disable																							
			Disabled	0								Read: Disabled																							
			Enabled	1								Read: Enabled																							
L	RW	PREGION1RA										Write '1' to Disable interrupt on *EVENTS_PREGION[1].RA* event																							
			Clear	1								Disable																							
			Disabled	0								Read: Disabled																							
			Enabled	1								Read: Enabled																							

43.1.4 NMIEN

Address offset: 0x320

Enable or disable non-maskable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id								L	K	J	I																	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**								**Description**																							
A	RW	REGION0WA										Enable or disable non-maskable interrupt on *EVENTS_REGION[0].WA* event																							
			Disabled	0								Disable																							

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id								L	K	J	I																	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**								**Description**																							
			Enabled	1								Enable																							
B	RW	REGION0RA										Enable or disable non-maskable interrupt on *EVENTS_REGION[0].RA* event																							
			Disabled	0								Disable																							
			Enabled	1								Enable																							
C	RW	REGION1WA										Enable or disable non-maskable interrupt on *EVENTS_REGION[1].WA* event																							
			Disabled	0								Disable																							
			Enabled	1								Enable																							
D	RW	REGION1RA										Enable or disable non-maskable interrupt on *EVENTS_REGION[1].RA* event																							
			Disabled	0								Disable																							
			Enabled	1								Enable																							
E	RW	REGION2WA										Enable or disable non-maskable interrupt on *EVENTS_REGION[2].WA* event																							
			Disabled	0								Disable																							
			Enabled	1								Enable																							
F	RW	REGION2RA										Enable or disable non-maskable interrupt on *EVENTS_REGION[2].RA* event																							
			Disabled	0								Disable																							
			Enabled	1								Enable																							
G	RW	REGION3WA										Enable or disable non-maskable interrupt on *EVENTS_REGION[3].WA* event																							
			Disabled	0								Disable																							
			Enabled	1								Enable																							
H	RW	REGION3RA										Enable or disable non-maskable interrupt on *EVENTS_REGION[3].RA* event																							
			Disabled	0								Disable																							
			Enabled	1								Enable																							
I	RW	PREGION0WA										Enable or disable non-maskable interrupt on *EVENTS_PREGION[0].WA* event																							
			Disabled	0								Disable																							
			Enabled	1								Enable																							
J	RW	PREGION0RA										Enable or disable non-maskable interrupt on *EVENTS_PREGION[0].RA* event																							
			Disabled	0								Disable																							
			Enabled	1								Enable																							
K	RW	PREGION1WA										Enable or disable non-maskable interrupt on *EVENTS_PREGION[1].WA* event																							
			Disabled	0								Disable																							
			Enabled	1								Enable																							
L	RW	PREGION1RA										Enable or disable non-maskable interrupt on *EVENTS_PREGION[1].RA* event																							
			Disabled	0								Disable																							
			Enabled	1								Enable																							

43.1.5 NMIENSET

Address offset: 0x324

Enable non-maskable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id								L	K	J	I																	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
A	RW	REGION0WA																										Write '1' to Enable non-maskable interrupt on *EVENTS_REGION[0].WA* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
B	RW	REGION0RA																										Write '1' to Enable non-maskable interrupt on *EVENTS_REGION[0].RA* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
C	RW	REGION1WA																										Write '1' to Enable non-maskable interrupt on *EVENTS_REGION[1].WA* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
D	RW	REGION1RA																										Write '1' to Enable non-maskable interrupt on *EVENTS_REGION[1].RA* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
E	RW	REGION2WA																										Write '1' to Enable non-maskable interrupt on *EVENTS_REGION[2].WA* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
F	RW	REGION2RA																										Write '1' to Enable non-maskable interrupt on *EVENTS_REGION[2].RA* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
G	RW	REGION3WA																										Write '1' to Enable non-maskable interrupt on *EVENTS_REGION[3].WA* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
H	RW	REGION3RA																										Write '1' to Enable non-maskable interrupt on *EVENTS_REGION[3].RA* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
I	RW	PREGION0WA																										Write '1' to Enable non-maskable interrupt on *EVENTS_PREGION[0].WA* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
J	RW	PREGION0RA																										Write '1' to Enable non-maskable interrupt on *EVENTS_PREGION[0].RA* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
K	RW	PREGION1WA																										Write '1' to Enable non-maskable interrupt on *EVENTS_PREGION[1].WA* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id								L	K	J	I																	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
L	RW	PREGION1RA																										Write '1' to Enable non-maskable interrupt on *EVENTS_PREGION[1].RA* event							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							

43.1.6 NMIENCLR

Address offset: 0x328

Disable non-maskable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id								L	K	J	I																	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
A	RW	REGION0WA																										Write '1' to Disable non-maskable interrupt on *EVENTS_REGION[0].WA* event							
			Clear	1																								Disable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
B	RW	REGION0RA																										Write '1' to Disable non-maskable interrupt on *EVENTS_REGION[0].RA* event							
			Clear	1																								Disable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
C	RW	REGION1WA																										Write '1' to Disable non-maskable interrupt on *EVENTS_REGION[1].WA* event							
			Clear	1																								Disable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
D	RW	REGION1RA																										Write '1' to Disable non-maskable interrupt on *EVENTS_REGION[1].RA* event							
			Clear	1																								Disable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
E	RW	REGION2WA																										Write '1' to Disable non-maskable interrupt on *EVENTS_REGION[2].WA* event							
			Clear	1																								Disable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
F	RW	REGION2RA																										Write '1' to Disable non-maskable interrupt on *EVENTS_REGION[2].RA* event							
			Clear	1																								Disable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
G	RW	REGION3WA																										Write '1' to Disable non-maskable interrupt on *EVENTS_REGION[3].WA* event							
			Clear	1																								Disable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
H	RW	REGION3RA																										Write '1' to Disable non-maskable interrupt on *EVENTS_REGION[3].RA* event							
			Clear	1																								Disable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id								L	K	J	I																	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
I	RW	PREGION0WA																										Write '1' to Disable non-maskable interrupt on *EVENTS_PREGION[0].WA* event							
			Clear	1																								Disable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
J	RW	PREGION0RA																										Write '1' to Disable non-maskable interrupt on *EVENTS_PREGION[0].RA* event							
			Clear	1																								Disable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
K	RW	PREGION1WA																										Write '1' to Disable non-maskable interrupt on *EVENTS_PREGION[1].WA* event							
			Clear	1																								Disable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
L	RW	PREGION1RA																										Write '1' to Disable non-maskable interrupt on *EVENTS_PREGION[1].RA* event							
			Clear	1																								Disable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							

43.1.7 PERREGION[0].SUBSTATWA

Address offset: 0x400

Source of interrupt in region 0, write access detected while corresponding subregion was enabled for watching

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
A	RW	SR0																										Sub region 0 in region 0 (write '1' to clear)							
			NoAccess	0																								No write access occurred in this subregion							
			Access	1																								Write access(es) occurred in this subregion							
B	RW	SR1																										Sub region 1 in region 0 (write '1' to clear)							
			NoAccess	0																								No write access occurred in this subregion							
			Access	1																								Write access(es) occurred in this subregion							
C	RW	SR2																										Sub region 2 in region 0 (write '1' to clear)							
			NoAccess	0																								No write access occurred in this subregion							
			Access	1																								Write access(es) occurred in this subregion							
D	RW	SR3																										Sub region 3 in region 0 (write '1' to clear)							
			NoAccess	0																								No write access occurred in this subregion							
			Access	1																								Write access(es) occurred in this subregion							
E	RW	SR4																										Sub region 4 in region 0 (write '1' to clear)							
			NoAccess	0																								No write access occurred in this subregion							
			Access	1																								Write access(es) occurred in this subregion							
F	RW	SR5																										Sub region 5 in region 0 (write '1' to clear)							
			NoAccess	0																								No write access occurred in this subregion							
			Access	1																								Write access(es) occurred in this subregion							
G	RW	SR6																										Sub region 6 in region 0 (write '1' to clear)							
			NoAccess	0																								No write access occurred in this subregion							
			Access	1																								Write access(es) occurred in this subregion							
H	RW	SR7																										Sub region 7 in region 0 (write '1' to clear)							
			NoAccess	0																								No write access occurred in this subregion							
			Access	1																								Write access(es) occurred in this subregion							

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
I	RW	SR8																																	
			NoAccess	0																															
			Access	1																															
J	RW	SR9																																	
			NoAccess	0																															
			Access	1																															
K	RW	SR10																																	
			NoAccess	0																															
			Access	1																															
L	RW	SR11																																	
			NoAccess	0																															
			Access	1																															
M	RW	SR12																																	
			NoAccess	0																															
			Access	1																															
N	RW	SR13																																	
			NoAccess	0																															
			Access	1																															
O	RW	SR14																																	
			NoAccess	0																															
			Access	1																															
P	RW	SR15																																	
			NoAccess	0																															
			Access	1																															
Q	RW	SR16																																	
			NoAccess	0																															
			Access	1																															
R	RW	SR17																																	
			NoAccess	0																															
			Access	1																															
S	RW	SR18																																	
			NoAccess	0																															
			Access	1																															
T	RW	SR19																																	
			NoAccess	0																															
			Access	1																															
U	RW	SR20																																	
			NoAccess	0																															
			Access	1																															
V	RW	SR21																																	
			NoAccess	0																															
			Access	1																															
W	RW	SR22																																	
			NoAccess	0																															
			Access	1																															
X	RW	SR23																																	
			NoAccess	0																															
			Access	1																															
Y	RW	SR24																																	
			NoAccess	0																															
			Access	1																															
Z	RW	SR25																																	
			NoAccess	0																															
			Access	1																															
a	RW	SR26																																	

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			NoAccess	0																															
			Access	1																															
b	RW	SR27																																	
			NoAccess	0																															
			Access	1																															
c	RW	SR28																																	
			NoAccess	0																															
			Access	1																															
d	RW	SR29																																	
			NoAccess	0																															
			Access	1																															
e	RW	SR30																																	
			NoAccess	0																															
			Access	1																															
f	RW	SR31																																	
			NoAccess	0																															
			Access	1																															

43.1.8 PERREGION[0].SUBSTATRA

Address offset: 0x404

Source of interrupt in region 0, read access detected while corresponding subregion was enabled for watching

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	SR0																																	
			NoAccess	0																															
			Access	1																															
B	RW	SR1																																	
			NoAccess	0																															
			Access	1																															
C	RW	SR2																																	
			NoAccess	0																															
			Access	1																															
D	RW	SR3																																	
			NoAccess	0																															
			Access	1																															
E	RW	SR4																																	
			NoAccess	0																															
			Access	1																															
F	RW	SR5																																	
			NoAccess	0																															
			Access	1																															
G	RW	SR6																																	
			NoAccess	0																															
			Access	1																															
H	RW	SR7																																	
			NoAccess	0																															
			Access	1																															
I	RW	SR8																																	
			NoAccess	0																															
			Access	1																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
J	RW	SR9																																	
			NoAccess	0																															
			Access	1																															
K	RW	SR10																																	
			NoAccess	0																															
			Access	1																															
L	RW	SR11																																	
			NoAccess	0																															
			Access	1																															
M	RW	SR12																																	
			NoAccess	0																															
			Access	1																															
N	RW	SR13																																	
			NoAccess	0																															
			Access	1																															
O	RW	SR14																																	
			NoAccess	0																															
			Access	1																															
P	RW	SR15																																	
			NoAccess	0																															
			Access	1																															
Q	RW	SR16																																	
			NoAccess	0																															
			Access	1																															
R	RW	SR17																																	
			NoAccess	0																															
			Access	1																															
S	RW	SR18																																	
			NoAccess	0																															
			Access	1																															
T	RW	SR19																																	
			NoAccess	0																															
			Access	1																															
U	RW	SR20																																	
			NoAccess	0																															
			Access	1																															
V	RW	SR21																																	
			NoAccess	0																															
			Access	1																															
W	RW	SR22																																	
			NoAccess	0																															
			Access	1																															
X	RW	SR23																																	
			NoAccess	0																															
			Access	1																															
Y	RW	SR24																																	
			NoAccess	0																															
			Access	1																															
Z	RW	SR25																																	
			NoAccess	0																															
			Access	1																															
a	RW	SR26																																	
			NoAccess	0																															
			Access	1																															
b	RW	SR27																																	

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			NoAccess	0																															
			Access	1																															
c	RW	SR28																																	
			NoAccess	0																															
			Access	1																															
d	RW	SR29																																	
			NoAccess	0																															
			Access	1																															
e	RW	SR30																																	
			NoAccess	0																															
			Access	1																															
f	RW	SR31																																	
			NoAccess	0																															
			Access	1																															

43.1.9 PERREGION[1].SUBSTATWA

Address offset: 0x408

Source of interrupt in region 1, write access detected while corresponding subregion was enabled for watching

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	SR0																																	
			NoAccess	0																															
			Access	1																															
B	RW	SR1																																	
			NoAccess	0																															
			Access	1																															
C	RW	SR2																																	
			NoAccess	0																															
			Access	1																															
D	RW	SR3																																	
			NoAccess	0																															
			Access	1																															
E	RW	SR4																																	
			NoAccess	0																															
			Access	1																															
F	RW	SR5																																	
			NoAccess	0																															
			Access	1																															
G	RW	SR6																																	
			NoAccess	0																															
			Access	1																															
H	RW	SR7																																	
			NoAccess	0																															
			Access	1																															
I	RW	SR8																																	
			NoAccess	0																															
			Access	1																															
J	RW	SR9																																	
			NoAccess	0																															
			Access	1																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
K	RW	SR10																																	
			NoAccess	0																															
			Access	1																															
L	RW	SR11																																	
			NoAccess	0																															
			Access	1																															
M	RW	SR12																																	
			NoAccess	0																															
			Access	1																															
N	RW	SR13																																	
			NoAccess	0																															
			Access	1																															
O	RW	SR14																																	
			NoAccess	0																															
			Access	1																															
P	RW	SR15																																	
			NoAccess	0																															
			Access	1																															
Q	RW	SR16																																	
			NoAccess	0																															
			Access	1																															
R	RW	SR17																																	
			NoAccess	0																															
			Access	1																															
S	RW	SR18																																	
			NoAccess	0																															
			Access	1																															
T	RW	SR19																																	
			NoAccess	0																															
			Access	1																															
U	RW	SR20																																	
			NoAccess	0																															
			Access	1																															
V	RW	SR21																																	
			NoAccess	0																															
			Access	1																															
W	RW	SR22																																	
			NoAccess	0																															
			Access	1																															
X	RW	SR23																																	
			NoAccess	0																															
			Access	1																															
Y	RW	SR24																																	
			NoAccess	0																															
			Access	1																															
Z	RW	SR25																																	
			NoAccess	0																															
			Access	1																															
a	RW	SR26																																	
			NoAccess	0																															
			Access	1																															
b	RW	SR27																																	
			NoAccess	0																															
			Access	1																															
c	RW	SR28																																	

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			NoAccess	0																															
			Access	1																															
d	RW	SR29																																	
			NoAccess	0																															
			Access	1																															
e	RW	SR30																																	
			NoAccess	0																															
			Access	1																															
f	RW	SR31																																	
			NoAccess	0																															
			Access	1																															

43.1.10 PERREGION[1].SUBSTATRA

Address offset: 0x40C

Source of interrupt in region 1, read access detected while corresponding subregion was enabled for watching

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	SR0																																	
			NoAccess	0																															
			Access	1																															
B	RW	SR1																																	
			NoAccess	0																															
			Access	1																															
C	RW	SR2																																	
			NoAccess	0																															
			Access	1																															
D	RW	SR3																																	
			NoAccess	0																															
			Access	1																															
E	RW	SR4																																	
			NoAccess	0																															
			Access	1																															
F	RW	SR5																																	
			NoAccess	0																															
			Access	1																															
G	RW	SR6																																	
			NoAccess	0																															
			Access	1																															
H	RW	SR7																																	
			NoAccess	0																															
			Access	1																															
I	RW	SR8																																	
			NoAccess	0																															
			Access	1																															
J	RW	SR9																																	
			NoAccess	0																															
			Access	1																															
K	RW	SR10																																	
			NoAccess	0																															
			Access	1																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
				Description																															
L	RW	SR11																																	
			NoAccess	0																															
			Access	1																															
M	RW	SR12																																	
			NoAccess	0																															
			Access	1																															
N	RW	SR13																																	
			NoAccess	0																															
			Access	1																															
O	RW	SR14																																	
			NoAccess	0																															
			Access	1																															
P	RW	SR15																																	
			NoAccess	0																															
			Access	1																															
Q	RW	SR16																																	
			NoAccess	0																															
			Access	1																															
R	RW	SR17																																	
			NoAccess	0																															
			Access	1																															
S	RW	SR18																																	
			NoAccess	0																															
			Access	1																															
T	RW	SR19																																	
			NoAccess	0																															
			Access	1																															
U	RW	SR20																																	
			NoAccess	0																															
			Access	1																															
V	RW	SR21																																	
			NoAccess	0																															
			Access	1																															
W	RW	SR22																																	
			NoAccess	0																															
			Access	1																															
X	RW	SR23																																	
			NoAccess	0																															
			Access	1																															
Y	RW	SR24																																	
			NoAccess	0																															
			Access	1																															
Z	RW	SR25																																	
			NoAccess	0																															
			Access	1																															
a	RW	SR26																																	
			NoAccess	0																															
			Access	1																															
b	RW	SR27																																	
			NoAccess	0																															
			Access	1																															
c	RW	SR28																																	
			NoAccess	0																															
			Access	1																															
d	RW	SR29																																	

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
			NoAccess	0																								No read access occurred in this subregion							
			Access	1																								Read access(es) occurred in this subregion							
e	RW	SR30																										Sub region 30 in region 1 (write '1' to clear)							
			NoAccess	0																								No read access occurred in this subregion							
			Access	1																								Read access(es) occurred in this subregion							
f	RW	SR31																										Sub region 31 in region 1 (write '1' to clear)							
			NoAccess	0																								No read access occurred in this subregion							
			Access	1																								Read access(es) occurred in this subregion							

43.1.11 REGIONEN

Address offset: 0x510

Enable/disable regions watch

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id								L	K	J	I																	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
A	RW	RGN0WA																										Enable/disable write access watch in region[0]							
			Disable	0																								Disable write access watch in this region							
			Enable	1																								Enable write access watch in this region							
B	RW	RGN0RA																										Enable/disable read access watch in region[0]							
			Disable	0																								Disable read access watch in this region							
			Enable	1																								Enable read access watch in this region							
C	RW	RGN1WA																										Enable/disable write access watch in region[1]							
			Disable	0																								Disable write access watch in this region							
			Enable	1																								Enable write access watch in this region							
D	RW	RGN1RA																										Enable/disable read access watch in region[1]							
			Disable	0																								Disable read access watch in this region							
			Enable	1																								Enable read access watch in this region							
E	RW	RGN2WA																										Enable/disable write access watch in region[2]							
			Disable	0																								Disable write access watch in this region							
			Enable	1																								Enable write access watch in this region							
F	RW	RGN2RA																										Enable/disable read access watch in region[2]							
			Disable	0																								Disable read access watch in this region							
			Enable	1																								Enable read access watch in this region							
G	RW	RGN3WA																										Enable/disable write access watch in region[3]							
			Disable	0																								Disable write access watch in this region							
			Enable	1																								Enable write access watch in this region							
H	RW	RGN3RA																										Enable/disable read access watch in region[3]							
			Disable	0																								Disable read access watch in this region							
			Enable	1																								Enable read access watch in this region							
I	RW	PRGN0WA																										Enable/disable write access watch in PREGION[0]							
			Disable	0																								Disable write access watch in this PREGION							
			Enable	1																								Enable write access watch in this PREGION							
J	RW	PRGN0RA																										Enable/disable read access watch in PREGION[0]							
			Disable	0																								Disable read access watch in this PREGION							
			Enable	1																								Enable read access watch in this PREGION							
K	RW	PRGN1WA																										Enable/disable write access watch in PREGION[1]							
			Disable	0																								Disable write access watch in this PREGION							
			Enable	1																								Enable write access watch in this PREGION							
L	RW	PRGN1RA																										Enable/disable read access watch in PREGION[1]							
			Disable	0																								Disable read access watch in this PREGION							
			Enable	1																								Enable read access watch in this PREGION							

43.1.12 REGIONENSET

Address offset: 0x514

Enable regions watch

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id								L	K	J	I																	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**								**Description**																							
A	RW	RGN0WA										Enable write access watch in region[0]																							
			Set	1								Enable write access watch in this region																							
			Disabled	0								Write access watch in this region is disabled																							
			Enabled	1								Write access watch in this region is enabled																							
B	RW	RGN0RA										Enable read access watch in region[0]																							
			Set	1								Enable read access watch in this region																							
			Disabled	0								Read access watch in this region is disabled																							
			Enabled	1								Read access watch in this region is enabled																							
C	RW	RGN1WA										Enable write access watch in region[1]																							
			Set	1								Enable write access watch in this region																							
			Disabled	0								Write access watch in this region is disabled																							
			Enabled	1								Write access watch in this region is enabled																							
D	RW	RGN1RA										Enable read access watch in region[1]																							
			Set	1								Enable read access watch in this region																							
			Disabled	0								Read access watch in this region is disabled																							
			Enabled	1								Read access watch in this region is enabled																							
E	RW	RGN2WA										Enable write access watch in region[2]																							
			Set	1								Enable write access watch in this region																							
			Disabled	0								Write access watch in this region is disabled																							
			Enabled	1								Write access watch in this region is enabled																							
F	RW	RGN2RA										Enable read access watch in region[2]																							
			Set	1								Enable read access watch in this region																							
			Disabled	0								Read access watch in this region is disabled																							
			Enabled	1								Read access watch in this region is enabled																							
G	RW	RGN3WA										Enable write access watch in region[3]																							
			Set	1								Enable write access watch in this region																							
			Disabled	0								Write access watch in this region is disabled																							
			Enabled	1								Write access watch in this region is enabled																							
H	RW	RGN3RA										Enable read access watch in region[3]																							
			Set	1								Enable read access watch in this region																							
			Disabled	0								Read access watch in this region is disabled																							
			Enabled	1								Read access watch in this region is enabled																							
I	RW	PRGN0WA										Enable write access watch in PREGION[0]																							
			Set	1								Enable write access watch in this PREGION																							
			Disabled	0								Write access watch in this PREGION is disabled																							
			Enabled	1								Write access watch in this PREGION is enabled																							
J	RW	PRGN0RA										Enable read access watch in PREGION[0]																							
			Set	1								Enable read access watch in this PREGION																							
			Disabled	0								Read access watch in this PREGION is disabled																							
			Enabled	1								Read access watch in this PREGION is enabled																							
K	RW	PRGN1WA										Enable write access watch in PREGION[1]																							
			Set	1								Enable write access watch in this PREGION																							
			Disabled	0								Write access watch in this PREGION is disabled																							
			Enabled	1								Write access watch in this PREGION is enabled																							
L	RW	PRGN1RA										Enable read access watch in PREGION[1]																							
			Set	1								Enable read access watch in this PREGION																							
			Disabled	0								Read access watch in this PREGION is disabled																							
			Enabled	1								Read access watch in this PREGION is enabled																							

43.1.13 REGIONENCLR

Address offset: 0x518

Disable regions watch

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id								L	K	J	I																	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	RGN0WA			Disable write access watch in region[0]
			Clear	1	Disable write access watch in this region
			Disabled	0	Write access watch in this region is disabled
			Enabled	1	Write access watch in this region is enabled
B	RW	RGN0RA			Disable read access watch in region[0]
			Clear	1	Disable read access watch in this region
			Disabled	0	Read access watch in this region is disabled
			Enabled	1	Read access watch in this region is enabled
C	RW	RGN1WA			Disable write access watch in region[1]
			Clear	1	Disable write access watch in this region
			Disabled	0	Write access watch in this region is disabled
			Enabled	1	Write access watch in this region is enabled
D	RW	RGN1RA			Disable read access watch in region[1]
			Clear	1	Disable read access watch in this region
			Disabled	0	Read access watch in this region is disabled
			Enabled	1	Read access watch in this region is enabled
E	RW	RGN2WA			Disable write access watch in region[2]
			Clear	1	Disable write access watch in this region
			Disabled	0	Write access watch in this region is disabled
			Enabled	1	Write access watch in this region is enabled
F	RW	RGN2RA			Disable read access watch in region[2]
			Clear	1	Disable read access watch in this region
			Disabled	0	Read access watch in this region is disabled
			Enabled	1	Read access watch in this region is enabled
G	RW	RGN3WA			Disable write access watch in region[3]
			Clear	1	Disable write access watch in this region
			Disabled	0	Write access watch in this region is disabled
			Enabled	1	Write access watch in this region is enabled
H	RW	RGN3RA			Disable read access watch in region[3]
			Clear	1	Disable read access watch in this region
			Disabled	0	Read access watch in this region is disabled
			Enabled	1	Read access watch in this region is enabled
I	RW	PRGN0WA			Disable write access watch in PREGION[0]
			Clear	1	Disable write access watch in this PREGION
			Disabled	0	Write access watch in this PREGION is disabled
			Enabled	1	Write access watch in this PREGION is enabled
J	RW	PRGN0RA			Disable read access watch in PREGION[0]
			Clear	1	Disable read access watch in this PREGION
			Disabled	0	Read access watch in this PREGION is disabled
			Enabled	1	Read access watch in this PREGION is enabled
K	RW	PRGN1WA			Disable write access watch in PREGION[1]
			Clear	1	Disable write access watch in this PREGION
			Disabled	0	Write access watch in this PREGION is disabled
			Enabled	1	Write access watch in this PREGION is enabled
L	RW	PRGN1RA			Disable read access watch in PREGION[1]
			Clear	1	Disable read access watch in this PREGION
			Disabled	0	Read access watch in this PREGION is disabled
			Enabled	1	Read access watch in this PREGION is enabled

43.1.14 REGION[0].START

Address offset: 0x600

Start address for region 0

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	START																																	
				Start address for region																															

43.1.15 REGION[0].END

Address offset: 0x604

End address of region 0

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	END																																	
				End address of region. Value 0 has a special meaning, see below.																															
			OneByte	0																															
				Region is 1 byte long (End address = Start address)																															

43.1.16 REGION[1].START

Address offset: 0x610

Start address for region 1

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	START																																	
				Start address for region																															

43.1.17 REGION[1].END

Address offset: 0x614

End address of region 1

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	END																																	
				End address of region. Value 0 has a special meaning, see below.																															
			OneByte	0																															
				Region is 1 byte long (End address = Start address)																															

43.1.18 REGION[2].START

Address offset: 0x620

Start address for region 2

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	START																																	
				Start address for region																															

43.1.19 REGION[2].END

Address offset: 0x624

End address of region 2

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																						**Description**									
A	RW	END																								End address of region. Value 0 has a special meaning, see below.									
			OneByte	0																						Region is 1 byte long (End address = Start address)									

43.1.20 REGION[3].START

Address offset: 0x630

Start address for region 3

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																						**Description**									
A	RW	START																								Start address for region									

43.1.21 REGION[3].END

Address offset: 0x634

End address of region 3

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																						**Description**									
A	RW	END																								End address of region. Value 0 has a special meaning, see below.									
			OneByte	0																						Region is 1 byte long (End address = Start address)									

43.1.22 PREGION[0].START

Address offset: 0x6C0

Reserved for future use

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																						**Description**									
A	R	START																								Reserved for future use									

43.1.23 PREGION[0].END

Address offset: 0x6C4

Reserved for future use

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																						**Description**									
A	R	END																								Reserved for future use									

43.1.24 PREGION[0].SUBS

Address offset: 0x6C8

Sub regions of region 0

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	SR0																																	Include or exclude subregion 0 in region
			Exclude	0																															Exclude
			Include	1																															Include
B	RW	SR1																																	Include or exclude subregion 1 in region
			Exclude	0																															Exclude
			Include	1																															Include
C	RW	SR2																																	Include or exclude subregion 2 in region
			Exclude	0																															Exclude
			Include	1																															Include
D	RW	SR3																																	Include or exclude subregion 3 in region
			Exclude	0																															Exclude
			Include	1																															Include
E	RW	SR4																																	Include or exclude subregion 4 in region
			Exclude	0																															Exclude
			Include	1																															Include
F	RW	SR5																																	Include or exclude subregion 5 in region
			Exclude	0																															Exclude
			Include	1																															Include
G	RW	SR6																																	Include or exclude subregion 6 in region
			Exclude	0																															Exclude
			Include	1																															Include
H	RW	SR7																																	Include or exclude subregion 7 in region
			Exclude	0																															Exclude
			Include	1																															Include
I	RW	SR8																																	Include or exclude subregion 8 in region
			Exclude	0																															Exclude
			Include	1																															Include
J	RW	SR9																																	Include or exclude subregion 9 in region
			Exclude	0																															Exclude
			Include	1																															Include
K	RW	SR10																																	Include or exclude subregion 10 in region
			Exclude	0																															Exclude
			Include	1																															Include
L	RW	SR11																																	Include or exclude subregion 11 in region
			Exclude	0																															Exclude
			Include	1																															Include
M	RW	SR12																																	Include or exclude subregion 12 in region
			Exclude	0																															Exclude
			Include	1																															Include
N	RW	SR13																																	Include or exclude subregion 13 in region
			Exclude	0																															Exclude
			Include	1																															Include
O	RW	SR14																																	Include or exclude subregion 14 in region
			Exclude	0																															Exclude
			Include	1																															Include
P	RW	SR15																																	Include or exclude subregion 15 in region
			Exclude	0																															Exclude
			Include	1																															Include
Q	RW	SR16																																	Include or exclude subregion 16 in region
			Exclude	0																															Exclude

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Include	1																															
R	RW	SR17																																	
			Exclude	0																															
			Include	1																															
S	RW	SR18																																	
			Exclude	0																															
			Include	1																															
T	RW	SR19																																	
			Exclude	0																															
			Include	1																															
U	RW	SR20																																	
			Exclude	0																															
			Include	1																															
V	RW	SR21																																	
			Exclude	0																															
			Include	1																															
W	RW	SR22																																	
			Exclude	0																															
			Include	1																															
X	RW	SR23																																	
			Exclude	0																															
			Include	1																															
Y	RW	SR24																																	
			Exclude	0																															
			Include	1																															
Z	RW	SR25																																	
			Exclude	0																															
			Include	1																															
a	RW	SR26																																	
			Exclude	0																															
			Include	1																															
b	RW	SR27																																	
			Exclude	0																															
			Include	1																															
c	RW	SR28																																	
			Exclude	0																															
			Include	1																															
d	RW	SR29																																	
			Exclude	0																															
			Include	1																															
e	RW	SR30																																	
			Exclude	0																															
			Include	1																															
f	RW	SR31																																	
			Exclude	0																															
			Include	1																															

43.1.25 PREGION[1].START

Address offset: 0x6D0

Reserved for future use

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	START																																	
				Reserved for future use																																	

43.1.26 PREGION[1].END

Address offset: 0x6D4

Reserved for future use

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	END																																	
				Reserved for future use																																	

43.1.27 PREGION[1].SUBS

Address offset: 0x6D8

Sub regions of region 1

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	SR0																																	
			Exclude	0																															
			Include	1																															
B	RW	SR1																																	
			Exclude	0																															
			Include	1																															
C	RW	SR2																																	
			Exclude	0																															
			Include	1																															
D	RW	SR3																																	
			Exclude	0																															
			Include	1																															
E	RW	SR4																																	
			Exclude	0																															
			Include	1																															
F	RW	SR5																																	
			Exclude	0																															
			Include	1																															
G	RW	SR6																																	
			Exclude	0																															
			Include	1																															
H	RW	SR7																																	
			Exclude	0																															
			Include	1																															
I	RW	SR8																																	
			Exclude	0																															
			Include	1																															
J	RW	SR9																																	
			Exclude	0																															
			Include	1																															
K	RW	SR10																																	
			Exclude	0																															
			Include	1																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
L	RW	SR11																																	
			Exclude	0																															
			Include	1																															
M	RW	SR12																																	
			Exclude	0																															
			Include	1																															
N	RW	SR13																																	
			Exclude	0																															
			Include	1																															
O	RW	SR14																																	
			Exclude	0																															
			Include	1																															
P	RW	SR15																																	
			Exclude	0																															
			Include	1																															
Q	RW	SR16																																	
			Exclude	0																															
			Include	1																															
R	RW	SR17																																	
			Exclude	0																															
			Include	1																															
S	RW	SR18																																	
			Exclude	0																															
			Include	1																															
T	RW	SR19																																	
			Exclude	0																															
			Include	1																															
U	RW	SR20																																	
			Exclude	0																															
			Include	1																															
V	RW	SR21																																	
			Exclude	0																															
			Include	1																															
W	RW	SR22																																	
			Exclude	0																															
			Include	1																															
X	RW	SR23																																	
			Exclude	0																															
			Include	1																															
Y	RW	SR24																																	
			Exclude	0																															
			Include	1																															
Z	RW	SR25																																	
			Exclude	0																															
			Include	1																															
a	RW	SR26																																	
			Exclude	0																															
			Include	1																															
b	RW	SR27																																	
			Exclude	0																															
			Include	1																															
c	RW	SR28																																	
			Exclude	0																															
			Include	1																															
d	RW	SR29																																	

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Exclude	0																															
			Include	1																															
e	RW	SR30																																	
			Exclude	0																															
			Include	1																															
f	RW	SR31																																	
			Exclude	0																															
			Include	1																															

44 Event generator unit (EGU)

The Event generator unit (EGU) provides support for inter-layer signaling. This means support for atomic triggering of both CPU execution and hardware tasks from both firmware (by CPU) and hardware (by PPI). This feature can, for instance, be used for triggering CPU execution at a lower priority execution from a higher priority execution, or to handle a peripheral's ISR execution at a lower priority for some of its events. However, triggering any priority from any priority is possible.

Listed here are the main EGU features:

- Enables SW triggering of interrupts
- 6 EGU instances – separate interrupt vectors
- Up to 16 separate event flags per interrupt for multiplexing

The EGU implements a set of tasks which can individually be triggered to generate the corresponding event, i.e., the corresponding event for TASKS_TRIGGER[n] is EVENTS_TRIGGERED[n].

Table 106: EGU configuration

EGU instance	Number of event flags
0-5	16

44.1 Registers

Table 107: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40014000	EGU	EGU0	Event Generator Unit 0	
0x40015000	EGU	EGU1	Event Generator Unit 1	
0x40016000	EGU	EGU2	Event Generator Unit 2	
0x40017000	EGU	EGU3	Event Generator Unit 3	
0x40018000	EGU	EGU4	Event Generator Unit 4	
0x40019000	EGU	EGU5	Event Generator Unit 5	

Table 108: Register Overview

Register	Offset	Description
TASKS_TRIGGER[0]	0x000	Trigger 0 for triggering the corresponding TRIGGERED[0] event
TASKS_TRIGGER[1]	0x004	Trigger 1 for triggering the corresponding TRIGGERED[1] event
TASKS_TRIGGER[2]	0x008	Trigger 2 for triggering the corresponding TRIGGERED[2] event
TASKS_TRIGGER[3]	0x00C	Trigger 3 for triggering the corresponding TRIGGERED[3] event
TASKS_TRIGGER[4]	0x010	Trigger 4 for triggering the corresponding TRIGGERED[4] event
TASKS_TRIGGER[5]	0x014	Trigger 5 for triggering the corresponding TRIGGERED[5] event
TASKS_TRIGGER[6]	0x018	Trigger 6 for triggering the corresponding TRIGGERED[6] event
TASKS_TRIGGER[7]	0x01C	Trigger 7 for triggering the corresponding TRIGGERED[7] event
TASKS_TRIGGER[8]	0x020	Trigger 8 for triggering the corresponding TRIGGERED[8] event
TASKS_TRIGGER[9]	0x024	Trigger 9 for triggering the corresponding TRIGGERED[9] event
TASKS_TRIGGER[10]	0x028	Trigger 10 for triggering the corresponding TRIGGERED[10] event
TASKS_TRIGGER[11]	0x02C	Trigger 11 for triggering the corresponding TRIGGERED[11] event
TASKS_TRIGGER[12]	0x030	Trigger 12 for triggering the corresponding TRIGGERED[12] event
TASKS_TRIGGER[13]	0x034	Trigger 13 for triggering the corresponding TRIGGERED[13] event
TASKS_TRIGGER[14]	0x038	Trigger 14 for triggering the corresponding TRIGGERED[14] event
TASKS_TRIGGER[15]	0x03C	Trigger 15 for triggering the corresponding TRIGGERED[15] event
EVENTS_TRIGGERED[0]	0x100	Event number 0 generated by triggering the corresponding TRIGGER[0] task
EVENTS_TRIGGERED[1]	0x104	Event number 1 generated by triggering the corresponding TRIGGER[1] task
EVENTS_TRIGGERED[2]	0x108	Event number 2 generated by triggering the corresponding TRIGGER[2] task
EVENTS_TRIGGERED[3]	0x10C	Event number 3 generated by triggering the corresponding TRIGGER[3] task
EVENTS_TRIGGERED[4]	0x110	Event number 4 generated by triggering the corresponding TRIGGER[4] task

Register	Offset	Description
EVENTS_TRIGGERED[5]	0x114	Event number 5 generated by triggering the corresponding TRIGGER[5] task
EVENTS_TRIGGERED[6]	0x118	Event number 6 generated by triggering the corresponding TRIGGER[6] task
EVENTS_TRIGGERED[7]	0x11C	Event number 7 generated by triggering the corresponding TRIGGER[7] task
EVENTS_TRIGGERED[8]	0x120	Event number 8 generated by triggering the corresponding TRIGGER[8] task
EVENTS_TRIGGERED[9]	0x124	Event number 9 generated by triggering the corresponding TRIGGER[9] task
EVENTS_TRIGGERED[10]	0x128	Event number 10 generated by triggering the corresponding TRIGGER[10] task
EVENTS_TRIGGERED[11]	0x12C	Event number 11 generated by triggering the corresponding TRIGGER[11] task
EVENTS_TRIGGERED[12]	0x130	Event number 12 generated by triggering the corresponding TRIGGER[12] task
EVENTS_TRIGGERED[13]	0x134	Event number 13 generated by triggering the corresponding TRIGGER[13] task
EVENTS_TRIGGERED[14]	0x138	Event number 14 generated by triggering the corresponding TRIGGER[14] task
EVENTS_TRIGGERED[15]	0x13C	Event number 15 generated by triggering the corresponding TRIGGER[15] task
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt

44.1.1 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	TRIGGERED0			Enable or disable interrupt on *EVENTS_TRIGGERED[0]* event
			Disabled	0	Disable
			Enabled	1	Enable
B	RW	TRIGGERED1			Enable or disable interrupt on *EVENTS_TRIGGERED[1]* event
			Disabled	0	Disable
			Enabled	1	Enable
C	RW	TRIGGERED2			Enable or disable interrupt on *EVENTS_TRIGGERED[2]* event
			Disabled	0	Disable
			Enabled	1	Enable
D	RW	TRIGGERED3			Enable or disable interrupt on *EVENTS_TRIGGERED[3]* event
			Disabled	0	Disable
			Enabled	1	Enable
E	RW	TRIGGERED4			Enable or disable interrupt on *EVENTS_TRIGGERED[4]* event
			Disabled	0	Disable
			Enabled	1	Enable
F	RW	TRIGGERED5			Enable or disable interrupt on *EVENTS_TRIGGERED[5]* event
			Disabled	0	Disable
			Enabled	1	Enable
G	RW	TRIGGERED6			Enable or disable interrupt on *EVENTS_TRIGGERED[6]* event
			Disabled	0	Disable
			Enabled	1	Enable
H	RW	TRIGGERED7			Enable or disable interrupt on *EVENTS_TRIGGERED[7]* event
			Disabled	0	Disable
			Enabled	1	Enable
I	RW	TRIGGERED8			Enable or disable interrupt on *EVENTS_TRIGGERED[8]* event
			Disabled	0	Disable
			Enabled	1	Enable
J	RW	TRIGGERED9			Enable or disable interrupt on *EVENTS_TRIGGERED[9]* event
			Disabled	0	Disable
			Enabled	1	Enable
K	RW	TRIGGERED10			Enable or disable interrupt on *EVENTS_TRIGGERED[10]* event
			Disabled	0	Disable
			Enabled	1	Enable
L	RW	TRIGGERED11			Enable or disable interrupt on *EVENTS_TRIGGERED[11]* event

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																				P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Disabled	0																															
			Enabled	1																															
M	RW	TRIGGERED12																																	
			Disabled	0																															
			Enabled	1																															
N	RW	TRIGGERED13																																	
			Disabled	0																															
			Enabled	1																															
O	RW	TRIGGERED14																																	
			Disabled	0																															
			Enabled	1																															
P	RW	TRIGGERED15																																	
			Disabled	0																															
			Enabled	1																															

44.1.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																				P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	TRIGGERED0																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	TRIGGERED1																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	TRIGGERED2																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
D	RW	TRIGGERED3																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
E	RW	TRIGGERED4																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
F	RW	TRIGGERED5																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
G	RW	TRIGGERED6																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
H	RW	TRIGGERED7																																	
			Set	1																															
			Disabled	0																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																				P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Enabled	1																															
I	RW	TRIGGERED8																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
J	RW	TRIGGERED9																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
K	RW	TRIGGERED10																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
L	RW	TRIGGERED11																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
M	RW	TRIGGERED12																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
N	RW	TRIGGERED13																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
O	RW	TRIGGERED14																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
P	RW	TRIGGERED15																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															

44.1.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																				P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	TRIGGERED0																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	TRIGGERED1																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	TRIGGERED2																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																				P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
				Description																															
D	RW	TRIGGERED3																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
E	RW	TRIGGERED4																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
F	RW	TRIGGERED5																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
G	RW	TRIGGERED6																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
H	RW	TRIGGERED7																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
I	RW	TRIGGERED8																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
J	RW	TRIGGERED9																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
K	RW	TRIGGERED10																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
L	RW	TRIGGERED11																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
M	RW	TRIGGERED12																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
N	RW	TRIGGERED13																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
O	RW	TRIGGERED14																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
P	RW	TRIGGERED15																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															

44.2 Electrical Specification

44.2.1 EGU Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
I_{EGU}	Current drawn by the EGU module		0		µA
$t_{EGU,EVT}$	Latency between setting an EGU event flag and the system setting an interrupt		1		cycles

45 Pulse Width Modulation (PWM)

The PWM module enables the generation of pulse width modulated signals on GPIO. The module implements an up or up-and-down counter with four PWM channels that drive assigned GPIOs.

Three PWM modules can provide up to 12 PWM channels with individual frequency control in groups of up to four channels. Furthermore, a built-in decoder and EasyDMA capabilities make it possible to manipulate the PWM duty cycles without CPU intervention. Arbitrary duty-cycle sequences are read from Data RAM and can be chained to implement ping-pong buffering or repeated into complex loops.

Listed here are the main features of one PWM module:

- Fixed PWM base frequency with programmable clock divider
- Up to four PWM channels with individual polarity and duty-cycle values
- Edge or center-aligned pulses across PWM channels
- Multiple duty-cycle arrays (sequences) defined in Data RAM
- Autonomous and glitch-free update of duty cycle values directly from memory through EasyDMA
- Change of polarity, duty-cycle, and base frequency possibly on every PWM period
- Data RAM sequences can be repeated or connected into loops

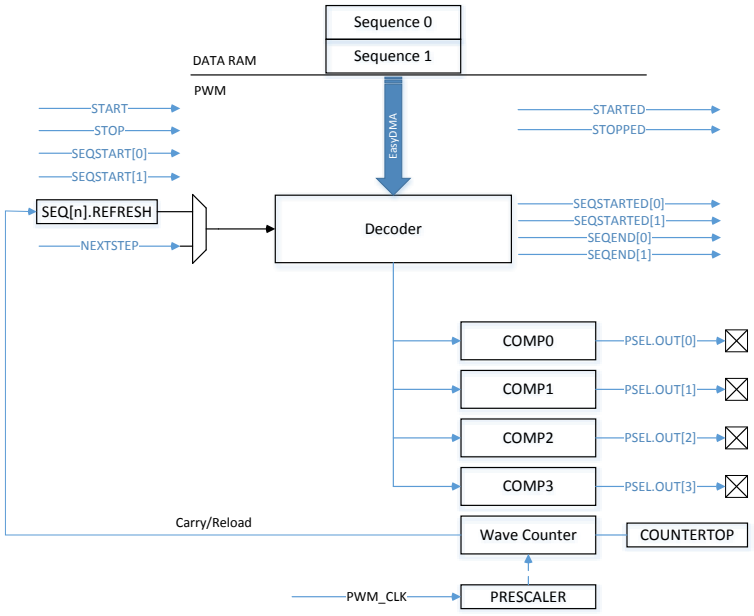


Figure 135: PWM Module

45.1 Pin configuration

The OUT[n] (n=0..3) signals associated to each channel of the PWM module are mapped to physical pins according to the configuration specified in the respective PSEL.OUT[n] registers. If a PSEL.OUT[n].CONNECT is set to Disconnected, the associated PWM module signal will not be connected to any physical pins.

The PSEL.OUT[n] registers and their configurations are only used as long as the PWM module is enabled and PWM generation is active (wave counter started), and retained only as long as the device is in System ON mode, see *POWER* chapter for more information about power modes.

To ensure correct behaviour in the PWM module, the pins used by the PWM module must be configured in the GPIO peripheral as described in *Table 109: GPIO configuration* on page 474 prior to enabling the PWM module. The pins' idle state is defined by the OUT registers in the GPIO module. The reason for this is to ensure that the pins used by the PWM module are driven correctly if PWM generation is stopped through a STOP task, the PWM module itself is temporarily disabled or the device temporarily enters system

OFF. This configuration must be retained in the GPIO for the selected IOs as long as the PWM module is supposed to be connected to an external PWM circuit.

Only one peripheral can be assigned to drive a particular GPIO pin at a time, failing to do so may result in unpredictable behaviour.

Table 109: GPIO configuration

PWM signal	PWM pin	Direction	Function	Comment
OUT[n]	As specified in PSEL.OUT[n] (n=0..3)	Output	PWM output	idle state defined in GPIO->OUT

45.2 Wave Counter

The wave counter is responsible for generating the pulses at a duty-cycle that depends on the compare values, and at a frequency that depends on COUNTERTOP.

There is one common 15-bit counter with four compare channels. Thus, all four channels will share the same period (PWM frequency), but can have individual duty-cycle and polarity. The polarity is set by the value read from RAM (see *Figure 138: Decoder memory access modes* on page 477), while the MODE register controls if the counter counts up or up and down. The timer top value is controlled by the COUNTERTOP register. This register value in conjunction with the selected PRESCALER of the PWM_CLK will result in a given PWM period. A COUNTERTOP value smaller than the compare setting will result in state where no PWM edges are generated. Respectively OUT[n] is held high given that the polarity is set to FallingEdge. All the compare registers are internal and can only be configured through the decoder presented later.

COUNTERTOP can be safely written at any time. It will get sampled following a START task. If DECODER.LOAD is anything else than WaveForm, it will also get sampled following a STARTSEQ[n] task, and when loading a new value from RAM during a sequence playback. If DECODER.LOAD=WaveForm, the register value is ignored, and taken from RAM instead (see *Decoder* on page 476 below).

Figure 136: PWM up counter example - FallingEdge polarity on page 475 shows the counter operating in up (MODE=PWM_MODE_Up) mode with three PWM channels with the same frequency but different duty cycle. The counter is automatically reset to zero when COUNTERTOP is reached and OUT[n] will invert. OUT[n] is held low if the compare value is 0 and held high respectively if set to COUNTERTOP given that the polarity is set to FallingEdge. Running in up counter mode will result in pulse widths that are edge-aligned. See the code example below:

```
uint16_t pwm_seq[2] = {PWM_CH0_DUTY, PWM_CH1_DUTY};
NRF_PWM->PSEL.OUT[0].PIN = GPIO_OUT_PIN0_Msk;
NRF_PWM->PSEL.OUT[0].CONNECT = PWM_PSEL_Connected;
NRF_PWM->PSEL.OUT[1].PIN = GPIO_OUT_PIN1_Msk;
NRF_PWM->PSEL.OUT[1].CONNECT = PWM_PSEL_Connected;
NRF_PWM->ENABLE = PWM_ENABLE_Enabled;
NRF_PWM->MODE.UPDOWN = PWM_MODE_Up; //Up Counting mode
NRF_PWM->COUNTERTOP = PWM_1MSEC_PER; //1msec period
NRF_PWM->SEQ[0].PTR = pwm_seq;
NRF_PWM->SEQ[0].CNT = sizeof(pwm_seq) / sizeof(uint16_t);
NRF_PWM->SEQ[0].REFRESH = 0;
NRF_PWM->LOOP.CNT = 0;
NRF_PWM->DECODER.LOAD = PWM_DECODER_LOAD_Individual;
NRF_PWM->DECODER.MODE = PWM_DECODER_MODE_RefreshCount;
NRF_PWM->TASKS_SEQSTART[0] = 1;
```

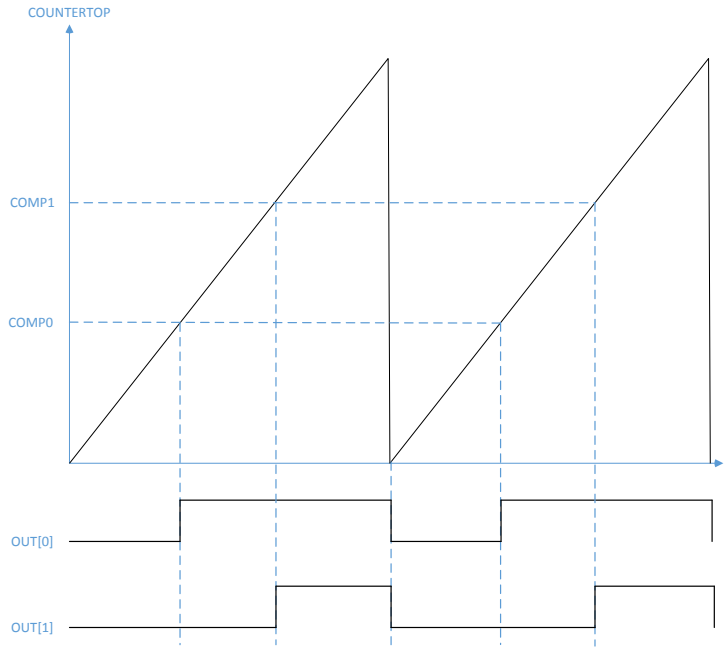


Figure 136: PWM up counter example - FallingEdge polarity

In up counting mode, the following formula can be used to compute PWM period and step size:

PWM period: $T_{PWM(Up)} = T_{PWM\_CLK} * COUNTERTOP$

Step width/Resolution: $T_{steps} = T_{PWM\_CLK}$

Figure 137: PWM up and down counter example on page 476 shows the counter operating in up and down mode with (MODE=PWM_MODE_UpAndDown) two PWM channels with the same frequency but different duty cycle and output polarity. The counter starts decrementing to zero when COUNTERTOP is reached and will invert the OUT[n] when compare value is hit for the second time. This results in a set of pulses that are center- aligned.

```
uint16_t pwm_seq[2] = {PWM_CH0_DUTY, PWM_CH1_DUTY};
NRF_PWM->PSEL.OUT[0].PIN = GPIO_OUT_PIN0_Msk;
NRF_PWM->PSEL.OUT[0].CONNECT = PWM_PSEL_Connected;
NRF_PWM->PSEL.OUT[1].PIN = GPIO_OUT_PIN1_Msk;
NRF_PWM->PSEL.OUT[1].CONNECT = PWM_PSEL_Connected;
NRF_PWM->ENABLE = PWM_ENABLE_Enabled;
NRF_PWM->MODE.UPDOWN = PWM_MODE_UpAndDown; //Up and down mode
NRF_PWM->COUNTERTOP = PWM_1MSEC_PER; //1msec period
NRF_PWM->SEQ[0].PTR = pwm_seq;
NRF_PWM->SEQ[0].CNT = sizeof(pwm_seq) / sizeof(uint16_t);
NRF_PWM->SEQ[0].REFRESH = 0;
NRF_PWM->LOOP.CNT = 0;
NRF_PWM->DECODER.LOAD = PWM_DECODER_LOAD_Individual;
NRF_PWM->DECODER.MODE = PWM_DECODER_MODE_RefreshCount;
NRF_PWM->TASKS_SEQSTART[0] = 1;
```

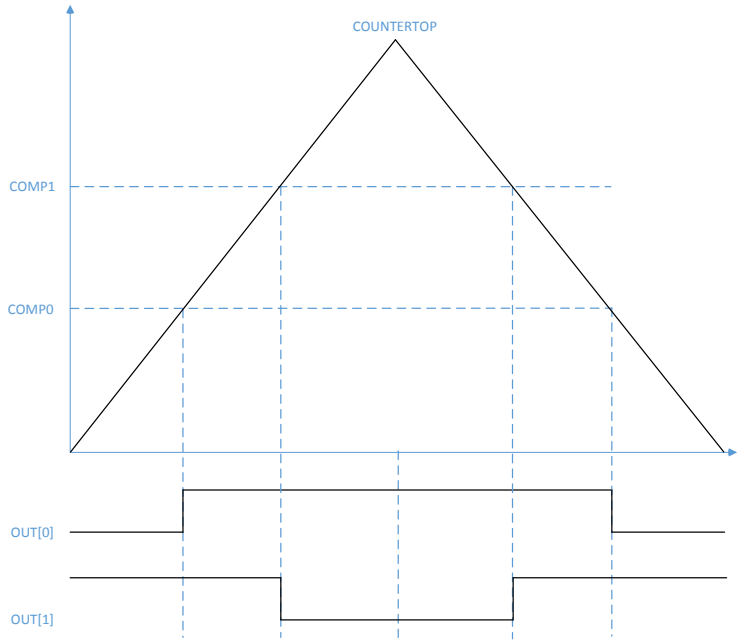


Figure 137: PWM up and down counter example

In up and down counting modes, the following formula can be used to compute PWM period and step size:
$T_{PWM(Up\ And\ Down)} = T_{PWM\_CLK} * 2 * COUNTERTOP$

Step width/Resolution: $T_{steps} = T_{PWM\_CLK} * 2$

45.3 Decoder

The decoder uses EasyDMA to take PWM parameters stored in Data RAM by ways of EasyDMA and updates the internal compare registers of the wave counter based on mode of operation.

The mentioned PWM parameters are organized into a sequence containing at least one half word (16-bit). Its most significant bit[15] denotes the polarity of the OUT[n] while bit[14:0] is the 15-bit compare value. See below for further details of these RAM defined registers.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																				B	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																**Description**															
A	RW	COMPARE																																	Duty cycle setting - value loaded to internal compare register
B	RW	POLARITY																																	Edge polarity of GPIO.
			RisingEdge	0																															First edge within the PWM period is rising
			FallingEdge	1																															First edge within the PWM period is falling

The DECODER register controls how the RAM content is interpreted and loaded to the internal compare registers. The LOAD field can be used to control if the RAM values are loaded to all compare channels - or alternatively to update a group or all channels with individual values. *Figure 138: Decoder memory access modes* on page 477 illustrates how the parameters stored in RAM are organized and routed to the various compare channels in the different modes.

A special mode of operation is available when DECODER.LOAD is set to WaveForm. In this mode, up to three PWM channels can be enabled - OUT[0] to OUT[2]. In RAM, four values are loaded at a time: the first, second and third location are used to load the values, and the fourth RAM location is used to load the COUNTERTOP register. This way one can have up to three PWM channels with a frequency base that changes on a per PWM period basis. This mode of operation is useful for arbitrary wave form generation in applications such as LED lighting.

The register SEQ[n].REFRESH=N (one per sequence n=0 or 1) will instruct a new RAM stored pulse width value on every $(N+1)^{th}$ PWM period. Setting the register to zero will result in a new duty cycle update every PWM period as long as the minimum PWM period is observed.

Note that registers SEQ[n].REFRESH and SEQ[n].ENDDELAY are ignored when DECODER.MODE=NextStep . The next value is loaded upon receiving every NEXTSTEP task.

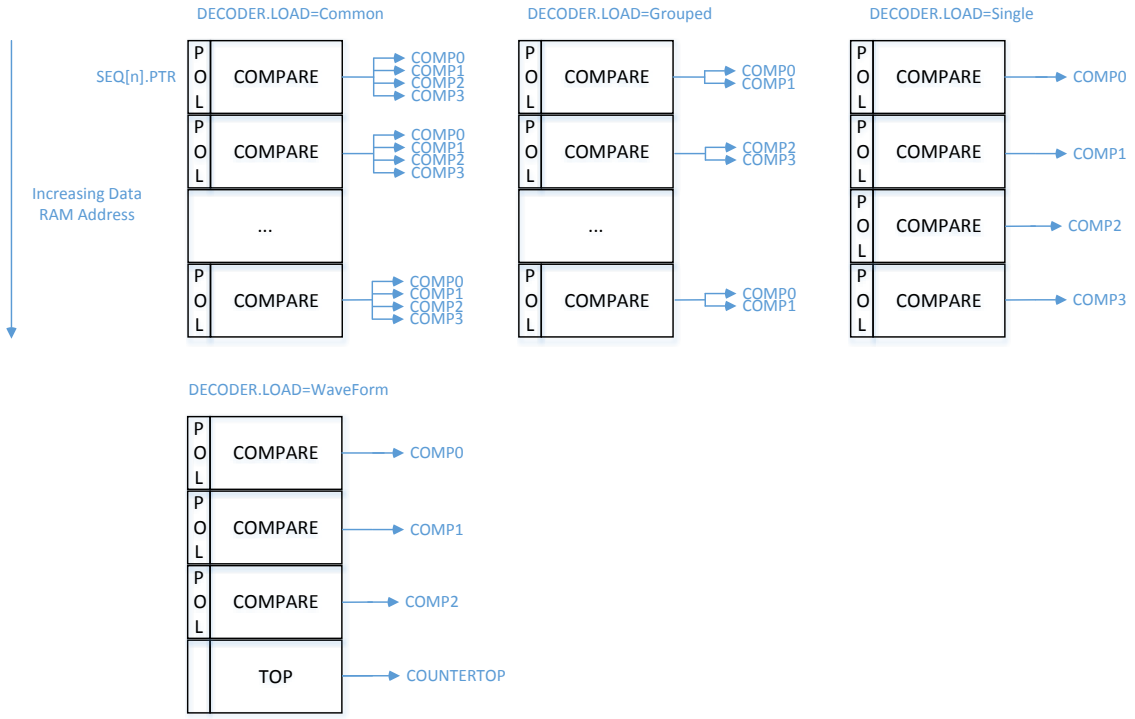


Figure 138: Decoder memory access modes

SEQ[n].PTR is the pointer used to fetch COMPARE values form RAM. If the SEQ[n].PTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 34 for more information about the different memory regions.

After the SEQ[n].PTR is set to the desired RAM location, the SEQ[n].CNT register must be set to the number of 16-bit half words in the sequence. It is important to observe that the Grouped and Single modes require one half word per group or one half word per channel respectively, and thus increases RAM size occupation. If PWM generation was not running yet at that point, sending the SEQSTART[n] task will load the first value from RAM, then start the PWM generation. A SEQSTARTED[n] event is generated as soon as the EasyDMA has read the first PWM parameter from RAM and the wave counter has started executing it. When LOOP.CNT=0, sequence n=0 or 1 is played back once. After the last value in the sequence has been loaded and started executing, a SEQEND[n] event is generated. The PWM generation will then continue with the last loaded value. See *Figure 139: Simple sequence example* on page 479 for an example of such simple playback.

To completely stop the PWM generation and force the associated pins to a defined state, a STOP task can be fired at any time. A STOPPED event is generated when the PWM generation has stopped at the end of currently running PWM period, and the pins go into their idle state as defined in GPIO->OUT. PWM generation can then only be restarted through a SEQSTART[n] task. SEQSTART[n] will resume PWM generation after having loaded the first value from the RAM buffer defined in the SEQ[n].PTR register.

The table below provides indication of when specific registers get sampled by the hardware. Care should be taken when updating these registers to avoid values to be applied earlier than expected.

Table 110: When to safely update PWM registers

Register	Taken into account by hardware	Recommended (safe) update
SEQ[n].PTR	When sending the SEQSTART[n] task	After having received the SEQSTARTED[n] event
SEQ[n].CNT	When sending the SEQSTART[n] task	After having received the SEQSTARTED[n] event
SEQ[0].ENDDELAY	When sending the SEQSTART[0] task	Before starting sequence [0] through a SEQSTART[0] task
	Every time a new value from sequence [0] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event)	When no more value from sequence [0] gets loaded from RAM (indicated by the SEQEND[0] event)
		At any time during sequence [1] (which starts when the SEQSTARTED[1] event is fired)
SEQ[1].ENDDELAY	When sending the SEQSTART[1] task	Before starting sequence [1] through a SEQSTART[1] task

Register	Taken into account by hardware	Recommended (safe) update
	Every time a new value from sequence [1] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event)	When no more value from sequence [1] gets loaded from RAM (indicated by the SEQEND[1] event) At any time during sequence [0] (which starts when the SEQSTARTED[0] event is fired)
SEQ[0].REFRESH	When sending the SEQSTART[0] task Every time a new value from sequence [0] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event)	Before starting sequence [0] through a SEQSTART[0] task At any time during sequence [1] (which starts when the SEQSTARTED[1] event is fired)
SEQ[1].REFRESH	When sending the SEQSTART[1] task Every time a new value from sequence [1] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event)	Before starting sequence [1] through a SEQSTART[1] task At any time during sequence [0] (which starts when the SEQSTARTED[0] event is fired)
COUNTERTOP	In DECODER.LOAD=WaveForm: this register is ignored. In all other LOAD modes: at the end of current PWM period (indicated by the PWMPERIODEND event)	Before starting PWM generation through a SEQSTART[n] task After a STOP task has been issued, and the STOPPED event has been received.
MODE	Immediately	Before starting PWM generation through a SEQSTART[n] task After a STOP task has been issued, and the STOPPED event has been received.
DECODER	Immediately	Before starting PWM generation through a SEQSTART[n] task After a STOP task has been issued, and the STOPPED event has been received.
PRESCALER	Immediately	Before starting PWM generation through a SEQSTART[n] task After a STOP task has been issued, and the STOPPED event has been received.
LOOP	Immediately	Before starting PWM generation through a SEQSTART[n] task After a STOP task has been issued, and the STOPPED event has been received.
PSEL.OUT[n]	Immediately	Before enabling the PWM instance through the ENABLE register

Note: SEQ[n].REFRESH and SEQ[n].ENDDELAY are ignored at the end of a complex sequence, indicated by a LOOPSDONE event. The reason for this is that the last value loaded from RAM is maintained until further action from software (restarting a new sequence, or stopping PWM generation).

Figure 139: Simple sequence example on page 479 depicts the source code used for configuration and timing details in a sequence where only sequence 0 is used and only run once with a new PWM duty cycle for each period.

```
NRF_PWM->PSEL.OUT[0].PIN = GPIO_OUT_PIN0_Msk;
NRF_PWM->PSEL.OUT[0].CONNECT = PWM_PSEL_Connected;
NRF_PWM->ENABLE = PWM_ENABLE_Enabled;
NRF_PWM->MODE.UPDOWN = PWM_MODE_Up; //Up Counting mode
NRF_PWM->PRESCALER = 0; //No prescaler applied
NRF_PWM->COUNTERTOP = PWM_1MSEC_PER; //1msec period
NRF_PWM->SEQ[0].PTR = seq0_ram;
NRF_PWM->SEQ[0].CNT = sizeof(seq0_ram) / sizeof(uint16_t);
NRF_PWM->SEQ[0].REFRESH = 0;
NRF_PWM->LOOP.CNT = 1;
NRF_PWM->SEQ[0].ENDDELAY = 0;
NRF_PWM->DECODER.LOAD = PWM_DECODER_LOAD_Common;
NRF_PWM->DECODER.MODE = PWM_DECODER_MODE_RefreshCount;
NRF_PWM->TASKS_SEQSTART[0] = 1;
```

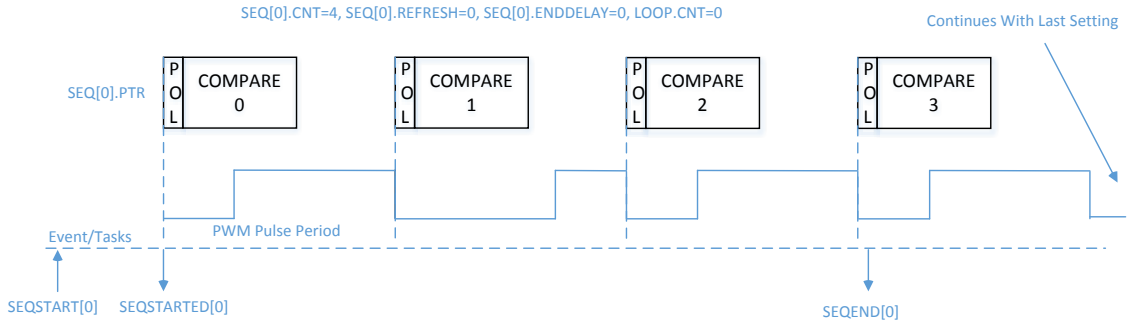


Figure 139: Simple sequence example

A more complex example is shown in *Figure 140: Example using two sequences* on page 480, where LOOP.CNT>0 . In this case, an automated playback takes place, consisting of SEQ[0], delay 0, SEQ[1], delay 1, then again SEQ[0], etc. The complex playback always ends with delay 1.

The two sequences 0 and 1 are defined with address of values tables in Data RAM (pointed by SEQ[n].PTR) and respective buffer size (SEQ[n].CNT). The rate at which a new value is loaded is defined individually for each sequence by SEQ[n].REFRESH . The LOOP.CNT register determines after how many times delay 1has been played the playback stops (and the LOOPSDONE event is generated), while the starting point is either SEQ[0] or SEQ[1], depending on which SEQSTART[n] task is called to start playback.

In the example below, sequence 0 is defined with SEQ[0].REFRESH set to one - that means that a new PWM duty cycle is pushed every second PWM period. This complex sequence is started with the SEQSTART[0] task, so SEQ[0] is played first. Since SEQ[0].ENDDELAY=1 there will be one PWM period delay between last period on sequence 0 and the first period on sequence 1. Since SEQ[1].ENDDELAY=0 there is no delay 1, so SEQ[0] would be started immediately after the end of SEQ[1]. However, as LOOP.CNT is one, the playback stops after having played only once SEQ[1], and both SEQEND[1] and LOOPSDONE are generated (their order is not guaranteed in this case).

```
NRF_PWM->PSEL.OUT[0].PIN = GPIO_OUT_PIN0_Msk;
NRF_PWM->PSEL.OUT[0].CONNECT = PWM_PSEL_Connected;
NRF_PWM->ENABLE = PWM_ENABLE_Enabled;
NRF_PWM->MODE.UPDOWN = PWM_MODE_Up; //Up Counting mode
NRF_PWM->PRESCALER = 0; //No prescaler applied
NRF_PWM->COUNTERTOP = PWM_1MSEC_PER; //1msec period
NRF_PWM->SEQ[0].PTR = seq0_ram;
NRF_PWM->SEQ[0].CNT = sizeof(seq0_ram) / sizeof(uint16_t);
NRF_PWM->SEQ[1].PTR = seq1_ram;
NRF_PWM->SEQ[1].CNT = sizeof(seq1_ram) / sizeof(uint16_t);
NRF_PWM->SEQ[0].REFRESH = 1;
NRF_PWM->SEQ[1].REFRESH = 0;
NRF_PWM->LOOP.CNT = 1;
NRF_PWM->SEQ[0].ENDDELAY = 1;
NRF_PWM->SEQ[1].ENDDELAY = 0;
NRF_PWM->DECODER.LOAD = PWM_DECODER_LOAD_Common;
NRF_PWM->DECODER.MODE = PWM_DECODER_MODE_RefreshCount;
NRF_PWM->TASKS_SEQSTART[0]  = 1;
```

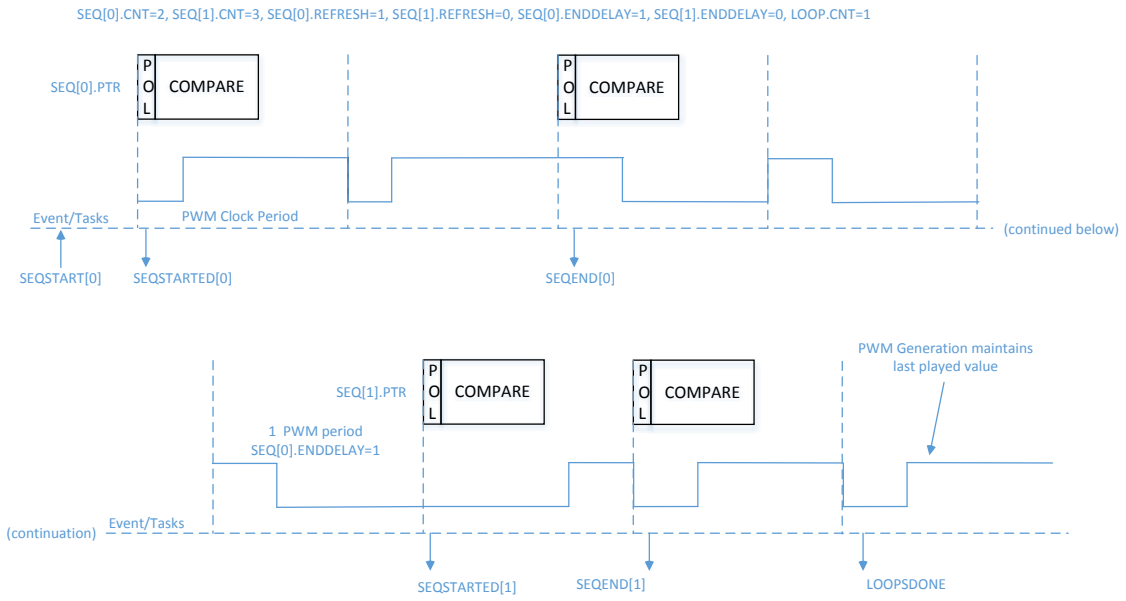


Figure 140: Example using two sequences

The decoder can also be configured to asynchronously load a new PWM duty cycle. If the DECODER.MODE register is set to NextStep - then the NEXTSTEP task will cause an update of the internal compare registers on the next PWM period.

The figures below provide an overview of each part of an arbitrary sequence, in various modes (LOOP.CNT=0 and LOOP.CNT>0). In particular are represented:

- initial and final duty cycle on the PWM output(s)
- chaining of SEQ[0] and SEQ[1] if LOOP.CNT>0
- influence of registers on the sequence
- events fired during a sequence
- DMA activity (loading of next value and applying it to the output(s))

Note that the single-shot example applies also to SEQ[1], only SEQ[0] is represented for simplicity.

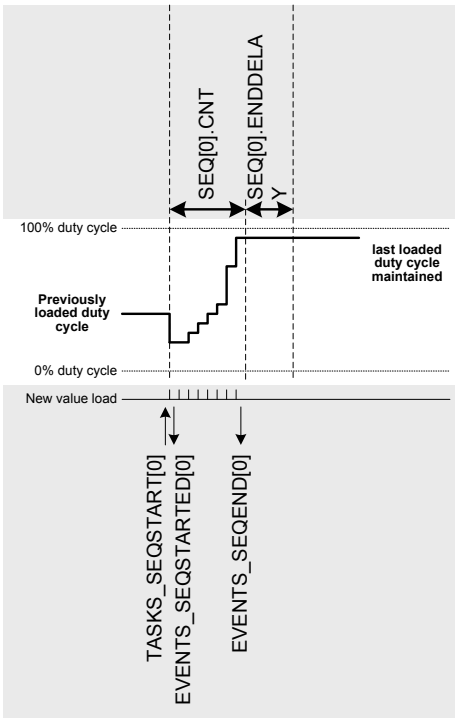


Figure 141: Single shot (LOOP.CNT=0)

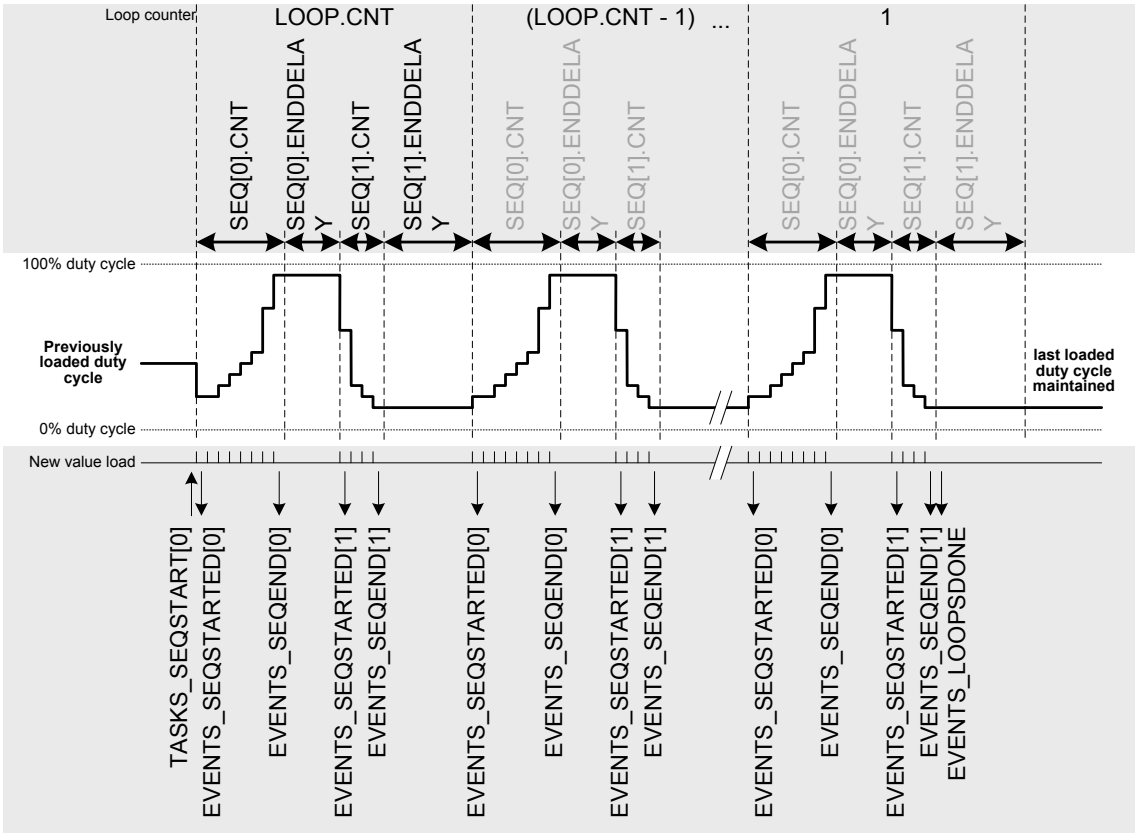


Figure 142: Complex sequence (LOOP.CNT>0) starting with SEQ[0]

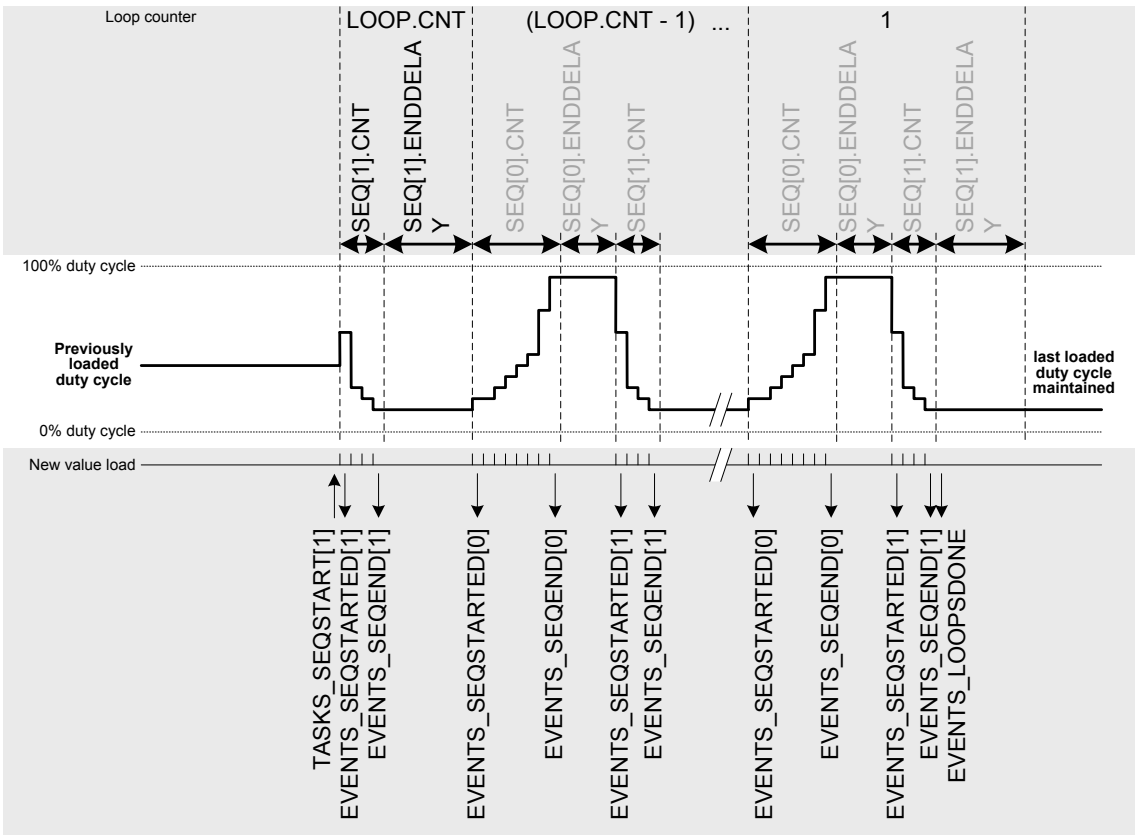


Figure 143: Complex sequence (LOOP.CNT>0) starting with SEQ[1]

45.4 Limitations

The previous compare value will be repeated if the PWM period is selected to be shorter than the time it takes for the EasyDMA to fetch from RAM and update the internal compare registers.

This is to ensure a glitch-free operation even if very short PWM periods are chosen.

45.5 Registers

Table 111: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4001C000	PWM	PWM0	Pulse Width Modulation Unit 0	
0x40021000	PWM	PWM1	Pulse Width Modulation Unit 1	
0x40022000	PWM	PWM2	Pulse Width Modulation Unit 2	

Table 112: Register Overview

Register	Offset	Description
TASKS_STOP	0x004	Stops PWM pulse generation on all channels at the end of current PWM period, and stops sequence playback
TASKS_SEQSTART[0]	0x008	Loads the first PWM value on all enabled channels from sequence 0, and starts playing that sequence at the rate defined in SEQ[0]REFRESH and/or DECODER.MODE. Causes PWM generation to start it was not running.
TASKS_SEQSTART[1]	0x00C	Loads the first PWM value on all enabled channels from sequence 1, and starts playing that sequence at the rate defined in SEQ[1]REFRESH and/or DECODER.MODE. Causes PWM generation to start it was not running.
TASKS_NEXTSTEP	0x010	Steps by one value in the current sequence on all enabled channels if DECODER.MODE=NextStep. Does not cause PWM generation to start it was not running.

Register	Offset	Description
EVENTS_STOPPED	0x104	Response to STOP task, emitted when PWM pulses are no longer generated
EVENTS_SEQSTARTED[0]	0x108	First PWM period started on sequence 0
EVENTS_SEQSTARTED[1]	0x10C	First PWM period started on sequence 1
EVENTS_SEQEND[0]	0x110	Emitted at end of every sequence 0, when last value from RAM has been applied to wave counter
EVENTS_SEQEND[1]	0x114	Emitted at end of every sequence 1, when last value from RAM has been applied to wave counter
EVENTS_PWMPERIODEN	0x118	Emitted at the end of each PWM period
EVENTS_LOOPSDONE	0x11C	Concatenated sequences have been played the amount of times defined in LOOP.CNT
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	PWM module enable register
MODE	0x504	Selects operating mode of the wave counter
COUNTERTOP	0x508	Value up to which the pulse generator counter counts
PRESCALER	0x50C	Configuration for PWM_CLK
DECODER	0x510	Configuration of the decoder
LOOP	0x514	Amount of playback of a loop
SEQ[0].PTR	0x520	Beginning address in Data RAM of sequence A
SEQ[0].CNT	0x524	Amount of values (duty cycles) in sequence A
SEQ[0].REFRESH	0x528	Amount of additional PWM periods between samples loaded to compare register (load every CNT+1 PWM periods)
SEQ[0].ENDDELAY	0x52C	Time added after the sequence
SEQ[1].PTR	0x540	Beginning address in Data RAM of sequence A
SEQ[1].CNT	0x544	Amount of values (duty cycles) in sequence A
SEQ[1].REFRESH	0x548	Amount of additional PWM periods between samples loaded to compare register (load every CNT+1 PWM periods)
SEQ[1].ENDDELAY	0x54C	Time added after the sequence
PSEL.OUT[0]	0x560	Output pin select for PWM channel 0
PSEL.OUT[1]	0x564	Output pin select for PWM channel 1
PSEL.OUT[2]	0x568	Output pin select for PWM channel 2
PSEL.OUT[3]	0x56C	Output pin select for PWM channel 3

45.5.1 SHORTS

Address offset: 0x200

Shortcut register

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												E	D	C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	SEQEND0_STOP			Shortcut between *EVENTS_SEQEND[0]* event and *TASKS_STOP* task
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
B	RW	SEQEND1_STOP			Shortcut between *EVENTS_SEQEND[1]* event and *TASKS_STOP* task
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
C	RW	LOOPSDONE_SEQSTART0			Shortcut between *EVENTS_LOOPSDONE* event and *TASKS_SEQSTART[0]* task
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
D	RW	LOOPSDONE_SEQSTART1			Shortcut between *EVENTS_LOOPSDONE* event and *TASKS_SEQSTART[1]* task
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
E	RW	LOOPSDONE_STOP																																	
			Disabled	0																															
			Enabled	1																															

45.5.2 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												H	G	F	E	D	C	B	
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
B	RW	STOPPED																																	
			Disabled	0																															
			Enabled	1																															
C	RW	SEQSTARTED0																																	
			Disabled	0																															
			Enabled	1																															
D	RW	SEQSTARTED1																																	
			Disabled	0																															
			Enabled	1																															
E	RW	SEQEND0																																	
			Disabled	0																															
			Enabled	1																															
F	RW	SEQEND1																																	
			Disabled	0																															
			Enabled	1																															
G	RW	PWMPERIODEND																																	
			Disabled	0																															
			Enabled	1																															
H	RW	LOOPSDONE																																	
			Disabled	0																															
			Enabled	1																															

45.5.3 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												H	G	F	E	D	C	B	
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
B	RW	STOPPED																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	SEQSTARTED0																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
D	RW	SEQSTARTED1																																	
			Set	1																															

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				H G F E D C B
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
E	RW	SEQEND0			Write '1' to Enable interrupt on *EVENTS_SEQEND[0]* event
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW	SEQEND1			Write '1' to Enable interrupt on *EVENTS_SEQEND[1]* event
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
G	RW	PWMPERIODEND			Write '1' to Enable interrupt on *EVENTS_PWMPERIODEND* event
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
H	RW	LOOPSDONE			Write '1' to Enable interrupt on *EVENTS_LOOPSDONE* event
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

45.5.4 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				H G F E D C B
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
B	RW	STOPPED			Write '1' to Disable interrupt on *EVENTS_STOPPED* event
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
C	RW	SEQSTARTED0			Write '1' to Disable interrupt on *EVENTS_SEQSTARTED[0]* event
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	SEQSTARTED1			Write '1' to Disable interrupt on *EVENTS_SEQSTARTED[1]* event
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
E	RW	SEQEND0			Write '1' to Disable interrupt on *EVENTS_SEQEND[0]* event
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW	SEQEND1			Write '1' to Disable interrupt on *EVENTS_SEQEND[1]* event
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
G	RW	PWMPERIODEND			Write '1' to Disable interrupt on *EVENTS_PWMPERIODEND* event
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
H	RW	LOOPSDONE			Write '1' to Disable interrupt on *EVENTS_LOOPSDONE* event
			Clear	1	Disable

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																											H	G	F	E	D	C	B	
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
			Disabled								0																Read: Disabled							
			Enabled								1																Read: Enabled							

45.5.5 ENABLE

Address offset: 0x500

PWM module enable register

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	RW	ENABLE																									Enable or disable PWM module							
			Disabled								0																Disabled							
			Enabled								1																Enable							

45.5.6 MODE

Address offset: 0x504

Selects operating mode of the wave counter

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	RW	UPDOWN																									Selects up or up and down as wave counter mode							
			Up								0																Up counter - edge aligned PWM duty-cycle							
			UpAndDown								1																Up and down counter - center aligned PWM duty cycle							

45.5.7 COUNTERTOP

Address offset: 0x508

Value up to which the pulse generator counter counts

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x000003FF			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	RW	COUNTERTOP									[3..32767]																Value up to which the pulse generator counter counts. This register is ignored when DECODER.MODE=WaveForm and only values from RAM will be used.							

45.5.8 PRESCALER

Address offset: 0x50C

Configuration for PWM_CLK

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																A	A	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	RW	PRESCALER																									Pre-scaler of PWM_CLK							
			DIV_1								0																Divide by 1 (16MHz)							
			DIV_2								1																Divide by 2 (8MHz)							
			DIV_4								2																Divide by 4 (4MHz)							
			DIV_8								3																Divide by 8 (2MHz)							

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A
Reset 0x00000000			**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
			DIV_16	4	Divide by 16 (1MHz)
			DIV_32	5	Divide by 32 (500kHz)
			DIV_64	6	Divide by 64 (250kHz)
			DIV_128	7	Divide by 128 (125kHz)

45.5.9 DECODER

Address offset: 0x510

Configuration of the decoder

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			B A A A
Reset 0x00000000			**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	LOAD			How a sequence is read from RAM and spread to the compare register
			Common	0	1st half word (16-bit) used in all PWM channels 0..3
			Grouped	1	1st half word (16-bit) used in channel 0..1; 2nd word in channel 2..3
			Individual	2	1st half word (16-bit) in ch.0; 2nd in ch.1; ...; 4th in ch.3
			WaveForm	3	1st half word (16-bit) in ch.0; 2nd in ch.1; ...; 4th in COUNTERTOP
B	RW	MODE			Selects source for advancing the active sequence
			RefreshCount	0	SEQ[n].REFRESH is used to determine loading internal compare registers
			NextStep	1	NEXTSTEP task causes a new value to be loaded to internal compare registers

45.5.10 LOOP

Address offset: 0x514

Amount of playback of a loop

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A A A A A A A A A
Reset 0x00000000			**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	CNT			Amount of playback of pattern cycles
			Disabled	0	Looping disabled (stop at the end of the sequence)

45.5.11 SEQ[0].PTR

Address offset: 0x520

Beginning address in Data RAM of sequence A

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000			**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	PTR			Beginning address in Data RAM of sequence A

45.5.12 SEQ[0].CNT

Address offset: 0x524

Amount of values (duty cycles) in sequence A

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																					A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	CNT																																	
			Disabled	0																															

45.5.13 SEQ[0].REFRESH

Address offset: 0x528

Amount of additional PWM periods between samples loaded to compare register (load every CNT+1 PWM periods)

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id												A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000001				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	CNT																																	
			Continuous	0																															

45.5.14 SEQ[0].ENDDELAY

Address offset: 0x52C

Time added after the sequence

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id												A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	CNT																																	

45.5.15 SEQ[1].PTR

Address offset: 0x540

Beginning address in Data RAM of sequence A

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PTR																																	

45.5.16 SEQ[1].CNT

Address offset: 0x544

Amount of values (duty cycles) in sequence A

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																					A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	CNT																																	
			Disabled	0																															

45.5.17 SEQ[1].REFRESH

Address offset: 0x548

Amount of additional PWM periods between samples loaded to compare register (load every CNT+1 PWM periods)

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000001			**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1**
Id	**Value Id**	**Value**	**Description**
A			Amount of additional PWM periods between samples loaded to compare register (load every CNT+1 PWM periods)
	Continuous	0	Update every PWM period

45.5.18 SEQ[1].ENDDELAY

Address offset: 0x54C

Time added after the sequence

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000			**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**Value Id**	**Value**	**Description**
A			Time added after the sequence in PWM periods

45.5.19 PSEL.OUT[0]

Address offset: 0x560

Output pin select for PWM channel 0

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			C A A A A A
Reset 0xFFFFFFFF			**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Id	**Value Id**	**Value**	**Description**
A		[0..31]	Pin number
C			Connection
	Disconnected	1	Disconnect
	Connected	0	Connect

45.5.20 PSEL.OUT[1]

Address offset: 0x564

Output pin select for PWM channel 1

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			C A A A A A
Reset 0xFFFFFFFF			**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Id	**Value Id**	**Value**	**Description**
A		[0..31]	Pin number
C			Connection
	Disconnected	1	Disconnect
	Connected	0	Connect

45.5.21 PSEL.OUT[2]

Address offset: 0x568

Output pin select for PWM channel 2

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			C A A A A A
Reset 0xFFFFFFFF			**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Id	**Value Id**	**Value**	**Description**
A		[0..31]	Pin number
C			Connection
	Disconnected	1	Disconnect
	Connected	0	Connect

45.5.22 PSEL.OUT[3]

Address offset: 0x56C

Output pin select for PWM channel 3

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				C																											A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PIN		[0..31]																															
C	RW	CONNECT																																	
			Disconnected	1																															
			Connected	0																															

45.6 Electrical Specification

45.6.1 PWM Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
$I_{PWM,16MHz}$	PWM run current, Prescaler set to DIV_1 (16 MHz)		200		µA
$I_{PWM,8MHz}$	PWM run current, Prescaler set to DIV_2 (8 MHz)		100		µA
$I_{PWM,125kHz}$	PWM run current, Prescaler set to DIV_128 (125 MHz)		50		µA

46 Serial Peripheral Interface (SPI) Master

The SPI master provides a simple CPU interface which includes a TXD register for sending data and an RXD register for receiving data. This section is added for legacy support for now.

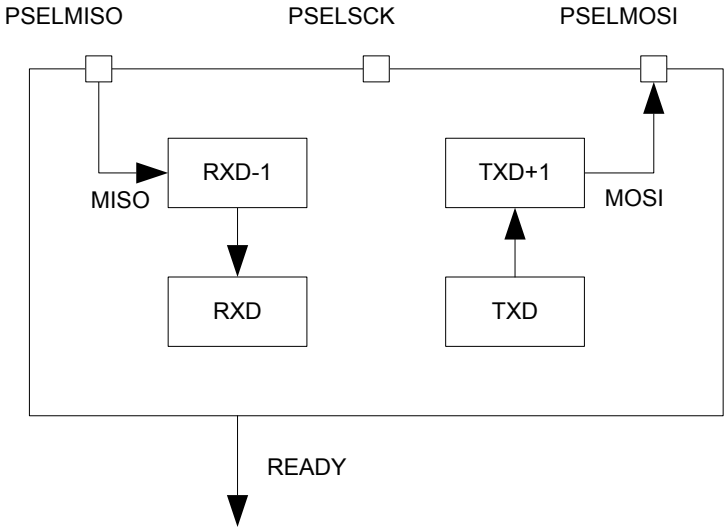


Figure 144: SPI master

RXD-1 and TXD+1 illustrate the double buffered version of RXD and TXD respectively.

46.1 Functional description

The TXD and RXD registers are double-buffered to enable some degree of uninterrupted data flow in and out of the SPI master.

The SPI master does not implement support for chip select directly. Therefore, the CPU must use available GPIOs to select the correct slave and control this independently of the SPI master. The SPI master supports SPI modes 0 through 3.

Table 113: SPI modes

Mode	Clock polarity CPOL	Clock phase CPHA
SPI_MODE	0 (Leading)	0 (Active High)
SPI_MODE	0 (Leading)	1 (Active Low)
SPI_MODE	1 (Trailing)	0 (Active High)
SPI_MODE	1 (Trailing)	1 (Active Low)

46.1.1 SPI master mode pin configuration

The different signals SCK, MOSI, and MISO associated with the SPI master are mapped to physical pins.

This mapping is according to the configuration specified in the PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers respectively. If a value of 0xFFFFFFFF is specified in any of these registers, the associated SPI master signal is not connected to any physical pin. The PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers and their configurations are only used as long as the SPI master is enabled, and retained only as long as the device is in ON mode. PSEL.SCK, PSEL.MOSI, and PSEL.MISO must only be configured when the SPI master is disabled.

To secure correct behavior in the SPI, the pins used by the SPI must be configured in the GPIO peripheral as described in *Table 114: GPIO configuration* on page 492 prior to enabling the SPI. The SCK must always be connected to a pin, and that pin's input buffer must always be connected for the SPI to work. This configuration must be retained in the GPIO for the selected IOs as long as the SPI is enabled.

Only one peripheral can be assigned to drive a particular GPIO pin at a time, failing to do so may result in unpredictable behavior.

Table 114: GPIO configuration

SPI master signal	SPI master pin	Direction	Output value
SCK	As specified in PSEL.SCK	Output	Same as CONFIG.CPOL
MOSI	As specified in PSEL.MOSI	Output	0
MISO	As specified in PSEL.MISO	Input	Not applicable

46.1.2 Shared resources

The SPI shares registers and other resources with other peripherals that have the same ID as the SPI. Therefore, the user must disable all peripherals that have the same ID as the SPI before the SPI can be configured and used.

Disabling a peripheral that has the same ID as the SPI will not reset any of the registers that are shared with the SPI. It is therefore important to configure all relevant SPI registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 36 for details on peripherals and their IDs.

46.1.3 SPI master transaction sequence

An SPI master transaction is started by writing the first byte, which is to be transmitted by the SPI master, to the TXD register.

Since the transmitter is double buffered, the second byte can be written to the TXD register immediately after the first one. The SPI master will then send these bytes in the order they are written to the TXD register.

The SPI master is a synchronous interface, and for every byte that is sent, a different byte will be received at the same time; this is illustrated in . Bytes that are received will be moved to the RXD register where the CPU can extract them by reading the register. The RXD register is double buffered in the same way as the TXD register, and a second byte can therefore be received at the *Figure 145: SPI master transaction* on page 493 same time as the first byte is being extracted from RXD by the CPU. The SPI master will generate a READY event every time a new byte is moved to the RXD register. The double buffered byte will be moved from RXD-1 to RXD as soon as the first byte is extracted from RXD. The SPI master will stop when there are no more bytes to send in TXD and TXD+1.

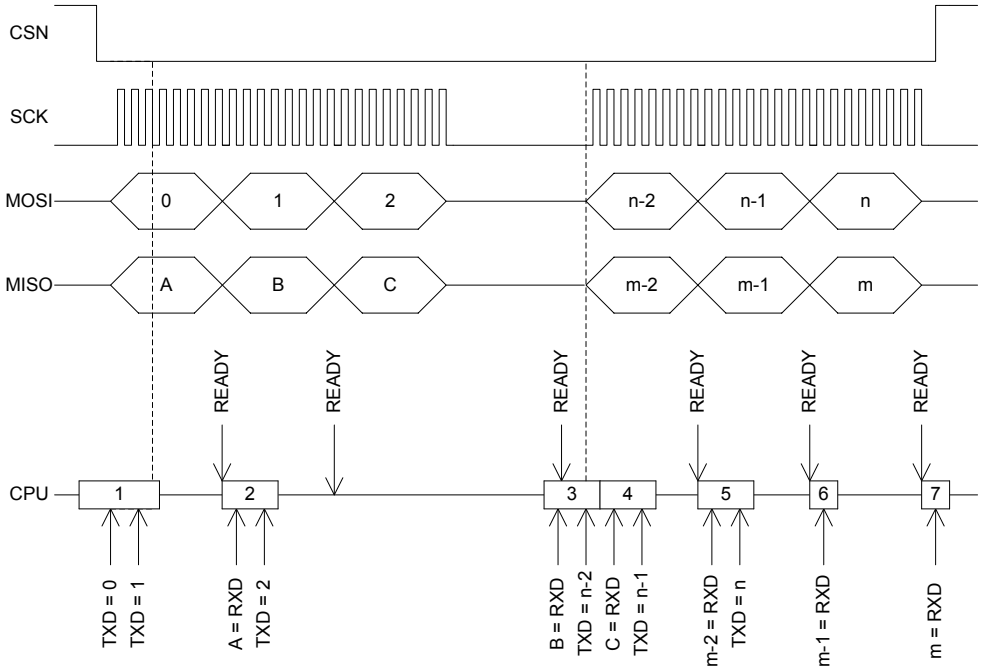


Figure 145: SPI master transaction

The READY event of the third byte transaction is delayed until B is extracted from RXD in occurrence number 3 on the horizontal lifeline. The reason for this is that the third event is generated first when C is moved from RXD-1 to RXD after B is read.

The SPI master will move the incoming byte to the RXD register after a short delay following the SCK clock period of the last bit in the byte. This also means that the READY event will be delayed accordingly, see *Figure 146: SPI master transaction* on page 493. Therefore, it is important that you always clear the READY event, even if the RXD register and the data that is being received is not used.

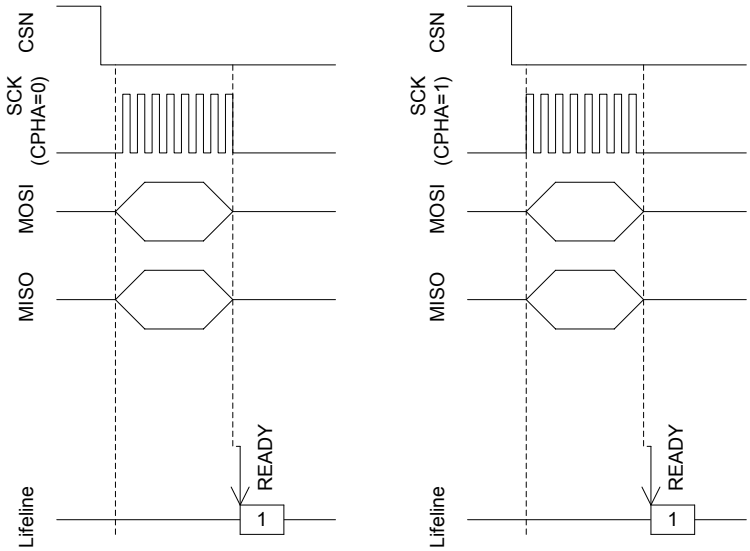


Figure 146: SPI master transaction

46.2 Registers

Table 115: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40003000	SPI	SPI0	SPI master 0		Deprecated
0x40004000	SPI	SPI1	SPI master 1		Deprecated
0x40023000	SPI	SPI2	SPI master 2.		Deprecated

Table 116: Register Overview

Register	Offset	Description
EVENTS_READY	0x108	TXD byte sent and RXD byte received
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	Enable SPI
PSEL.SCK	0x508	Pin select for SCK
PSEL.MOSI	0x50C	Pin select for MOSI
PSEL.MISO	0x510	Pin select for MISO
RXD	0x518	RXD register
TXD	0x51C	TXD register
FREQUENCY	0x524	SPI frequency
CONFIG	0x554	Configuration register

46.2.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit number																																
Id																															A		
Reset 0x00000000																															**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																											
A	RW	READY			Write '1' to Enable interrupt on *EVENTS_READY* event																													
			Set	1	Enable																											
			Disabled	0	Read: Disabled																											
			Enabled	1	Read: Enabled																											

46.2.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number																																
Id																															A		
Reset 0x00000000																															**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																											
A	RW	READY			Write '1' to Disable interrupt on *EVENTS_READY* event																													
			Clear	1	Disable																											
			Disabled	0	Read: Disabled																											
			Enabled	1	Read: Enabled																											

46.2.3 ENABLE

Address offset: 0x500

Enable SPI

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	ENABLE			Enable or disable SPI
			Disabled	0	Disable SPI
			Enabled	1	Enable SPI

46.2.4 PSEL.SCK

Address offset: 0x508

Pin select for SCK

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFFF				**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	PSELSCK		[0..31]	Pin number configuration for SPI SCK signal
			Disconnected	0xFFFFFFFF	Disconnect

46.2.5 PSEL.MOSI

Address offset: 0x50C

Pin select for MOSI

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFFF				**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	PSELMOSI		[0..31]	Pin number configuration for SPI MOSI signal
			Disconnected	0xFFFFFFFF	Disconnect

46.2.6 PSEL.MISO

Address offset: 0x510

Pin select for MISO

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFFF				**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	RW	PSELMISO		[0..31]	Pin number configuration for SPI MISO signal
			Disconnected	0xFFFFFFFF	Disconnect

46.2.7 RXD

Address offset: 0x518

RXD register

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**
A	R	RXD			RX data received. Double buffered

46.2.8 TXD

Address offset: 0x51C

TXD register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	TXD																																	
				TX data to send. Double buffered																															

46.2.9 FREQUENCY

Address offset: 0x524

SPI frequency

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x04000000				**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	FREQUENCY																																	
				SPI master data rate																															
			K125	0x02000000																															
				125 kbps																															
			K250	0x04000000																															
				250 kbps																															
			K500	0x08000000																															
				500 kbps																															
			M1	0x10000000																															
				1 Mbps																															
			M2	0x20000000																															
				2 Mbps																															
			M4	0x40000000																															
				4 Mbps																															
			M8	0x80000000																															
				8 Mbps																															

46.2.10 CONFIG

Address offset: 0x554

Configuration register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	ORDER																																	
				Bit order																															
			MsbFirst	0																															
				Most significant bit shifted out first																															
			LsbFirst	1																															
				Least significant bit shifted out first																															
B	RW	CPHA																																	
				Serial clock (SCK) phase																															
			Leading	0																															
				Sample on leading edge of clock, shift serial data on trailing edge																															
			Trailing	1																															
				Sample on trailing edge of clock, shift serial data on leading edge																															
C	RW	CPOL																																	
				Serial clock (SCK) polarity																															
			ActiveHigh	0																															
				Active high																															
			ActiveLow	1																															
				Active low																															

46.3 Electrical Specification

46.3.1 SPI master interface

Symbol	Description	Min.	Typ.	Max.	Units
f_{SPI}	Bit rates for SPI[34]			8	Mbps
$I_{SPI,2Mbps}$	Run current for SPI, 2 Mbps			50	µA
$I_{SPI,8Mbps}$	Run current for SPI, 8 Mbps			50	µA
$I_{SPI,IDLE}$	Idle current for SPI (STARTed, no CSN activity)		<1		µA
$t_{SPI,START,LP}$	Time from STARTRX/STARTTX task to RX/TX active, low power mode		3	5	µs

[34] Higher bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

Symbol	Description	Min.	Typ.	Max.	Units
$t_{SPI,START,CL}$	Time from STARTRX/STARTTX task to RX/TX active, constant latency mode		1	1	µs

46.3.2 Serial Peripheral Interface (SPI) Master timing specifications

Symbol	Description	Min.	Typ.	Max.	Units
$t_{SPI,CSCK,8Mbps}$	SCK period at 8Mbps		125		ns
$t_{SPI,CSCK,4Mbps}$	SCK period at 4Mbps		250		ns
$t_{SPI,CSCK,2Mbps}$	SCK period at 2Mbps		500		ns
$t_{SPI,RSCK,LD}$	SCK rise time, low drive[a]			$t_{RF,25pF}$	
$t_{SPI,RSCK,HD}$	SCK rise time, high drive[a]			$t_{HRF,25pF}$	
$t_{SPI,FSCK,LD}$	SCK fall time, low drive[a]			$t_{RF,25pF}$	
$t_{SPI,FSCK,HD}$	SCK fall time, high drive[a]			$t_{HRF,25pF}$	
$t_{SPI,WHSCK}$	SCK high time[a]	$(0.5*t_{CSCK})$ $- t_{RSCK}$			
$t_{SPI,WLSCK}$	SCK low time[a]	$(0.5*t_{CSCK})$ $- t_{FSCK}$			
$t_{SPI,SUMI}$	MISO to CLK edge setup time	5			ns
$t_{SPI,HMI}$	CLK edge to MISO hold time	5			ns
$t_{SPI,VMO}$	CLK edge to MOSI valid			40	ns
$t_{SPI,HMO}$	MOSI hold time after CLK edge	0			ns

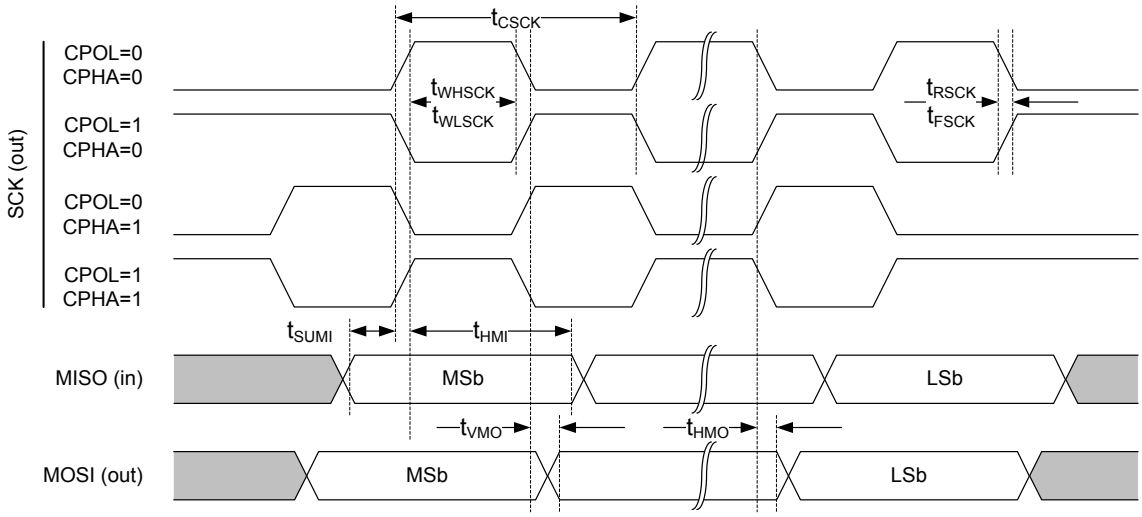


Figure 147: SPI master timing diagram

[a] At 25pF load, including GPIO capacitance, see GPIO spec.

47 I2C compatible Two Wire Interface (TWI)

The TWI master is compatible with I2C operating at 100 kHz and 400 kHz. This section is added for legacy support for now.

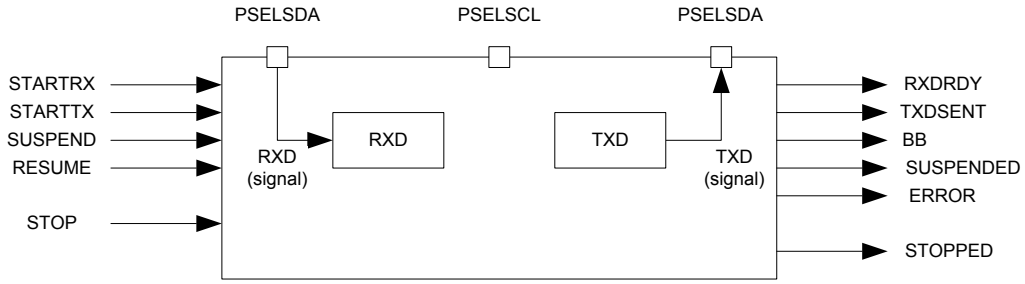


Figure 148: TWI master's main features

47.1 Functional description

This TWI master is not compatible with CBUS. The TWI transmitter and receiver are single buffered.

See, *Figure 148: TWI master's main features* on page 498.

A TWI setup comprising one master and three slaves is illustrated in *Figure 149: A typical TWI setup comprising one master and three slaves* on page 498. This TWI master is only able to operate as the only master on the TWI bus.

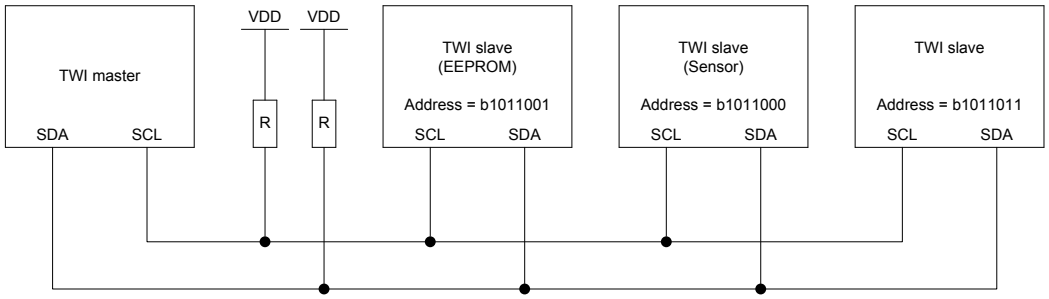


Figure 149: A typical TWI setup comprising one master and three slaves

This TWI master supports clock stretching performed by the slaves. The TWI master is started by triggering the STARTTX or STARTRX tasks, and stopped by triggering the STOP task.

If a NACK is clocked in from the slave, the TWI master will generate an ERROR event.

47.2 Master mode pin configuration

The different signals SCL and SDA associated with the TWI master are mapped to physical pins according to the configuration specified in the PSELSCL and PSELSDA registers respectively.

If a value of 0xFFFFFFFF is specified in any of these registers, the associated TWI master signal is not connected to any physical pin. The PSELSCL and PSELSDA registers and their configurations are only used

as long as the TWI master is enabled, and retained only as long as the device is in ON mode. PSELSCL and PSELSDA must only be configured when the TWI is disabled.

To secure correct signal levels on the pins used by the TWI master when the system is in OFF mode, and when the TWI master is disabled, these pins must be configured in the GPIO peripheral as described in *Table 117: GPIO configuration* on page 499.

Only one peripheral can be assigned to drive a particular GPIO pin at a time, failing to do so may result in unpredictable behavior.

Table 117: GPIO configuration

TWI master signal	TWI master pin	Direction	Drive strength	Output value
SCL	As specified in PSELSCL	Input	S0D1	Not applicable
SDA	As specified in PSELSDA	Input	S0D1	Not applicable

47.3 Shared resources

The TWI shares registers and other resources with other peripherals that have the same ID as the TWI.

Therefore, you must disable all peripherals that have the same ID as the TWI before the TWI can be configured and used. Disabling a peripheral that has the same ID as the TWI will not reset any of the registers that are shared with the TWI. It is therefore important to configure all relevant TWI registers explicitly to secure that it operates correctly.

The Instantiation table in *Instantiation* on page 36 shows which peripherals have the same ID as the TWI.

47.4 Master write sequence

A TWI master write sequence is started by triggering the STARTTX task. After the STARTTX task has been triggered, the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 0 (WRITE=0, READ=1).

The address must match the address of the slave device that the master wants to write to. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) generated by the slave.

After receiving the ACK bit, the TWI master will clock out the data bytes that are written to the TXD register. Each byte clocked out from the master will be followed by an ACK/NACK bit clocked in from the slave. A TXDSENT event will be generated each time the TWI master has clocked out a TXD byte, and the associated ACK/NACK bit has been clocked in from the slave.

The TWI master transmitter is single buffered, and a second byte can only be written to the TXD register after the previous byte has been clocked out and the ACK/NACK bit clocked in, that is, after the TXDSENT event has been generated.

If the CPU is prevented from writing to TXD when the TWI master is ready to clock out a byte, the TWI master will stretch the clock until the CPU has written a byte to the TXD register.

A typical TWI master write sequence is illustrated in *Figure 150: The TWI master writing data to a slave* on page 500. Occurrence 3 in the figure illustrates delayed processing of the TXDSENT event associated with TXD byte 1. In this scenario the TWI master will stretch the clock to prevent writing erroneous data to the slave.

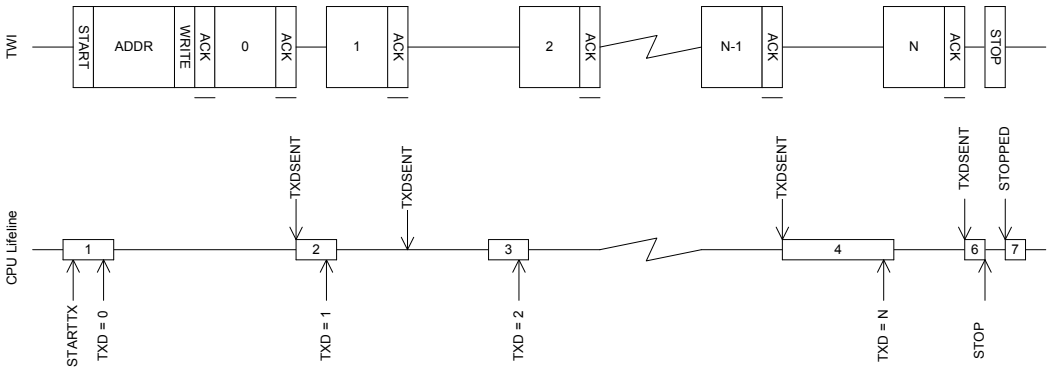


Figure 150: The TWI master writing data to a slave

The TWI master write sequence is stopped when the STOP task is triggered whereupon the TWI master will generate a stop condition on the TWI bus.

47.5 Master read sequence

A TWI master read sequence is started by triggering the STARTRX task. After the STARTRX task has been triggered the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 1 (WRITE = 0, READ = 1).

The address must match the address of the slave device that the master wants to read from. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK = 1) generated by the slave.

After having sent the ACK bit the TWI slave will send data to the master using the clock generated by the master.

The TWI master will generate a RXDRDY event every time a new byte is received in the RXD register.

After receiving a byte, the TWI master will delay sending the ACK/NACK bit by stretching the clock until the CPU has extracted the received byte, that is, by reading the RXD register.

The TWI master read sequence is stopped by triggering the STOP task. This task must be triggered before the last byte is extracted from RXD to ensure that the TWI master sends a NACK back to the slave before generating the stop condition.

A typical TWI master read sequence is illustrated in *Figure 151: The TWI master reading data from a slave* on page 501. Occurrence 3 in this figure illustrates delayed processing of the RXDRDY event associated with RXD byte B. In this scenario the TWI master will stretch the clock to prevent the slave from overwriting the contents of the RXD register.

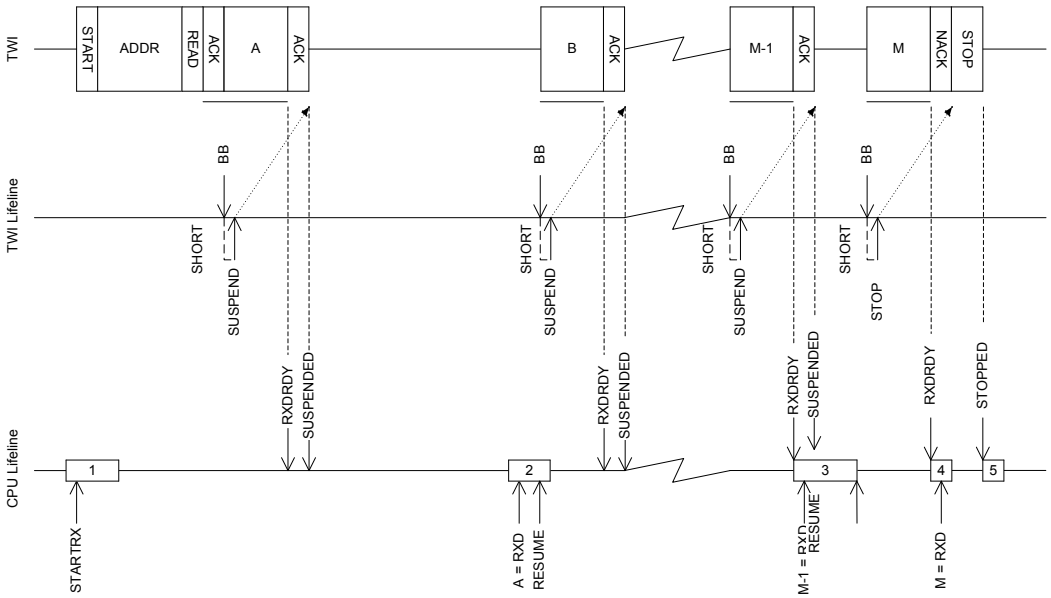


Figure 151: The TWI master reading data from a slave

47.6 Master repeated start sequence

A typical repeated start sequence is one in which the TWI master writes one byte to the slave followed by reading M bytes from the slave. Any combination and number of transmit and receive sequences can be combined in this fashion. Only one shortcut to STOP can be enabled at any given time.

The figure below illustrates a repeated start sequence where the TWI master writes one byte, followed by reading M bytes from the slave without performing a stop in-between.

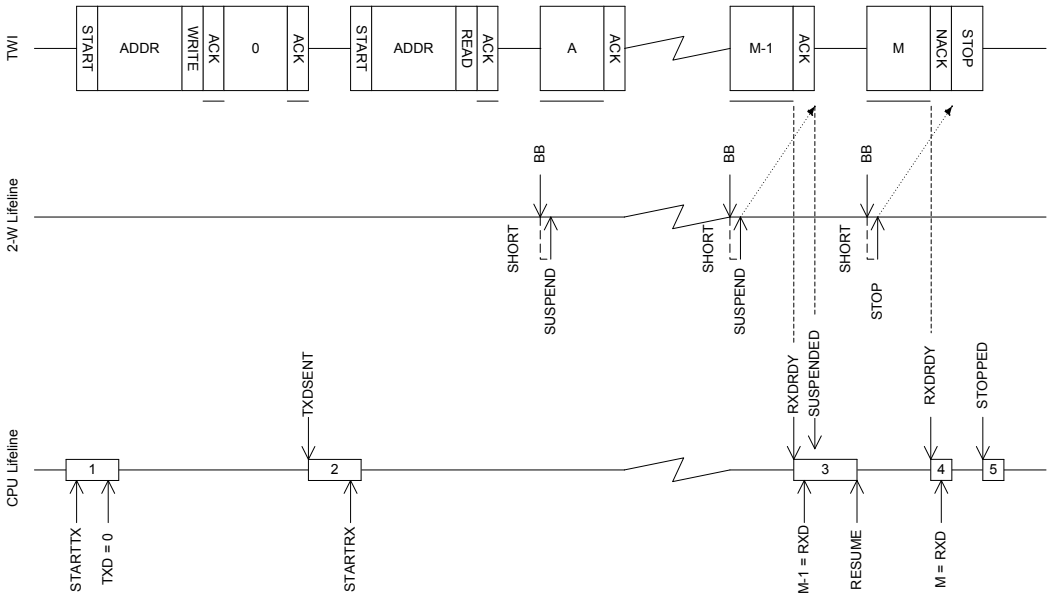


Figure 152: A repeated start sequence, where the TWI master writes one byte, followed by reading M bytes from the slave without performing a stop in-between

To generate a repeated start after a read sequence, a second start task must be triggered instead of the STOP task, that is, STARTRX or STARTTX. This start task must be triggered before the last byte is extracted from RXD to ensure that the TWI master sends a NACK back to the slave before generating the repeated start condition.

47.7 Registers

Table 118: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40003000	TWI	TWI0	Two-wire interface master 0		Deprecated
0x40004000	TWI	TWI1	Two-wire interface master 1		Deprecated

Table 119: Register Overview

Register	Offset	Description
TASKS_STARTRX	0x000	Start TWI receive sequence
TASKS_STARTTX	0x008	Start TWI transmit sequence
TASKS_STOP	0x014	Stop TWI transaction
TASKS_SUSPEND	0x01C	Suspend TWI transaction
TASKS_RESUME	0x020	Resume TWI transaction
EVENTS_STOPPED	0x104	TWI stopped
EVENTS_RXDREADY	0x108	TWI RXD byte received
EVENTS_TXDSENT	0x11C	TWI TXD byte sent
EVENTS_ERROR	0x124	TWI error
EVENTS_BB	0x138	TWI byte boundary, generated before each byte that is sent or received
EVENTS_SUSPENDED	0x148	TWI entered the suspended state
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x4C4	Error source
ENABLE	0x500	Enable TWI
PSELSCL	0x508	Pin select for SCL
PSELSDA	0x50C	Pin select for SDA
RXD	0x518	RXD register
TXD	0x51C	TXD register
FREQUENCY	0x524	TWI frequency
ADDRESS	0x588	Address used in the TWI transfer

47.7.1 SHORTS

Address offset: 0x200

Shortcut register

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															B	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Id	RW	Field	Value Id	Value	Description
A	RW	BB_SUSPEND			Shortcut between *EVENTS_BB* event and *TASKS_SUSPEND* task
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
B	RW	BB_STOP			Shortcut between *EVENTS_BB* event and *TASKS_STOP* task
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut

47.7.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																	F				E					D		C						B	A	
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	STOPPED																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	RXDREADY																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	TXDSENT																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
D	RW	ERROR																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
E	RW	BB																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
F	RW	SUSPENDED																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															

47.7.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																	F				E					D		C						B	A	
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	STOPPED																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	RXDREADY																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	TXDSENT																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
D	RW	ERROR																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
E	RW	BB																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
F	RW	SUSPENDED																																	

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																F				E					D		C					B	A	
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
			Clear								1																Disable							
			Disabled								0																Read: Disabled							
			Enabled								1																Read: Enabled							

47.7.4 ERRORSRC

Address offset: 0x4C4

Error source

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																C	B	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	RW	OVERRUN																									Overrun error							
																											A new byte was received before previous byte got read by software from the RXD register. (Previous data is lost)							
			NotPresent								0																Read: no overrun occured							
			Present								1																Read: overrun occured							
B	RW	ANACK																									NACK received after sending the address (write '1' to clear)							
			NotPresent								0																Read: error not present							
			Present								1																Read: error present							
C	RW	DNACK																									NACK received after sending a data byte (write '1' to clear)							
			NotPresent								0																Read: error not present							
			Present								1																Read: error present							

47.7.5 ENABLE

Address offset: 0x500

Enable TWI

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															A	A	A	A
Reset 0x00000000			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	RW	ENABLE																									Enable or disable TWI							
			Disabled								0																Disable TWI							
			Enabled								5																Enable TWI							

47.7.6 PSELSCL

Address offset: 0x508

Pin select for SCL

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id			A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF			**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**								**Value**																**Description**							
A	RW	PSELSCL									[0..31]																Pin number configuration for TWI SCL signal							
			Disconnected								0xFFFFFFFF																Disconnect							

47.7.7 PSELSDA

Address offset: 0x50C

Pin select for SDA

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
A	RW	PSELSDA		[0..31]																								Pin number configuration for TWI SDA signal							
			Disconnected	0xFFFFFFFF																								Disconnect							

47.7.8 RXD

Address offset: 0x518

RXD register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
A	R	RXD																										RXD register							

47.7.9 TXD

Address offset: 0x51C

TXD register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
A	RW	TXD																										TXD register							

47.7.10 FREQUENCY

Address offset: 0x524

TWI frequency

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x04000000				**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
A	RW	FREQUENCY																										TWI master clock frequency							
			K100	0x01980000																								100 kbps							
			K250	0x04000000																								250 kbps							
			K400	0x06680000																								400 kbps (actual rate 410.256 kbps)							

47.7.11 ADDRESS

Address offset: 0x588

Address used in the TWI transfer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																														A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																								**Description**							
A	RW	ADDRESS																										Address used in the TWI transfer							

47.8 Electrical Specification

47.8.1 TWI interface electrical specifications

Symbol	Description	Min.	Typ.	Max.	Units
f_{TWI}	Bit rates for TWI[35]	100		400	kbps
$I_{TWI,100kbps}$	Run current for TWI, 100 kbps		50		µA
$I_{TWI,400kbps}$	Run current for TWI, 400 kbps		50		µA
$t_{TWI,START,LP}$	Time from STARTRX/STARTTX task to RX/TX active, Low power mode		3		µs
$t_{TWI,START,CL}$	Time from STARTRX/STARTTX task to RX/TX active, Constant latency mode		1		µs

47.8.2 Two Wire Interface (TWI) timing specifications

Symbol	Description	Min.	Typ.	Max.	Units
$f_{TWI,SCL,100kbps}$	SCL clock frequency, 100 kbps		100		kHz
$f_{TWI,SCL,250kbps}$	SCL clock frequency, 250 kbps		250		kHz
$f_{TWI,SCL,400kbps}$	SCL clock frequency, 400 kbps		400		kHz
t_{TWI,SU_DAT}	Data setup time before positive edge on SCL – all modes	300			ns
t_{TWI,HD_DAT}	Data hold time after negative edge on SCL – all modes	300			ns
$t_{TWI,HD\_STA,100kbps}$	TWI master hold time for START and repeated START condition, 100 kbps	5200			ns
$t_{TWI,HD\_STA,250kbps}$	TWI master hold time for START and repeated START condition, 250kbps				ns
$t_{TWI,HD\_STA,400kbps}$	TWI master hold time for START and repeated START condition, 400 kbps	1300			ns
$t_{TWI,SU\_STO,100kbps}$	TWI master setup time from SCL high to STOP condition, 100 kbps	5200			ns
$t_{TWI,SU\_STO,250kbps}$	TWI master setup time from SCL high to STOP condition, 250 kbps				ns
$t_{TWI,SU\_STO,400kbps}$	TWI master setup time from SCL high to STOP condition, 400 kbps	1300			ns
$t_{TWI,BUF,100kbps}$	TWI master bus free time between STOP and START conditions, 100 kbps	4700			ns
$t_{TWI,BUF,250kbps}$	TWI master bus free time between STOP and START conditions, 250 kbps				ns
$t_{TWI,BUF,400kbps}$	TWI master bus free time between STOP and START conditions, 400 kbps	1300			ns

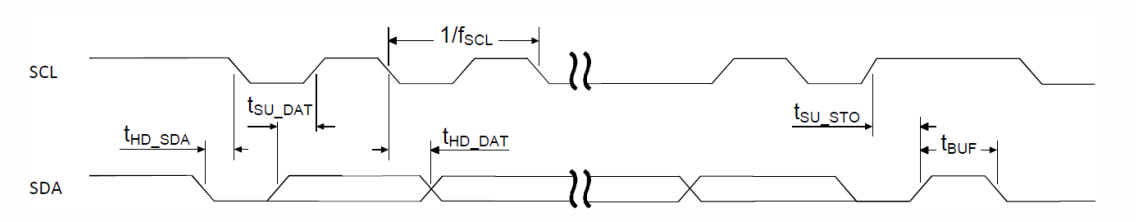


Figure 153: TWI timing diagram, 1 byte transaction

[35] Higher bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see GPIO chapter for more details.

48 Universal Asynchronous Receiver/Transmitter (UART)

This section is added for legacy support for now.

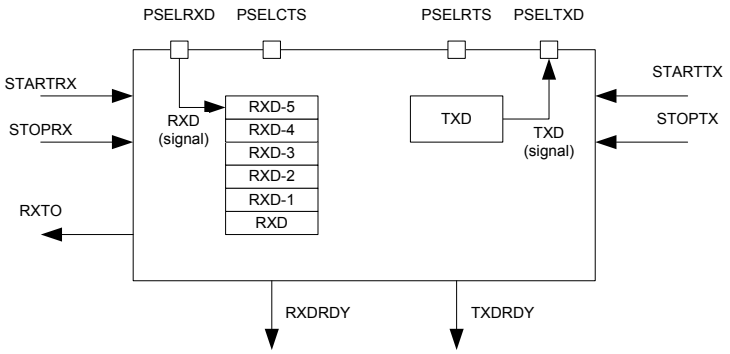


Figure 154: UART configuration

48.1 Functional description

Listed here are the main features of UART.

The UART implements support for the following features:

- Full-duplex operation
- Automatic flow control
- Parity checking and generation for the 9th data bit

As illustarated in *Figure 154: UART configuration* on page 507, the UART uses the TXD and RXD registers directly to transmit and receive data. The UART uses one stop bit.

48.2 Pin configuration

The different signals RXD, CTS (Clear To Send, active low), RTS (Request To Send, active low), and TXD associated with the UART are mapped to physical pins according to the configuration specified in the PSELRXD, PSELCTS, PSELRTS, and PSELTXD registers respectively.

If a value of 0xFFFFFFFF is specified in any of these registers, the associated UART signal will not be connected to any physical pin. The PSELRXD, PSELCTS, PSELRTS, and PSELTXD registers and their configurations are only used as long as the UART is enabled, and retained only for the duration the device is in ON mode. PSELRXD, PSELCTS, PSELRTS and PSELTXD must only be configured when the UART is disabled.

To secure correct signal levels on the pins by the UART when the system is in OFF mode, the pins must be configured in the GPIO peripheral as described in *Pin configuration* on page 507.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 120: GPIO configuration

UART pin	Direction	Output value
RXD	Input	Not applicable
CTS	Input	Not applicable
RTS	Output	1
TXD	Output	1

48.3 Shared resources

The UART shares registers and other resources with other peripherals that have the same ID as the UART.

Therefore, you must disable all peripherals that have the same ID as the UART before the UART can be configured and used. Disabling a peripheral that has the same ID as the UART will not reset any of the registers that are shared with the UART. It is therefore important to configure all relevant UART registers explicitly to ensure that it operates correctly.

See the Instantiation table in *Instantiation* on page 36 for details on peripherals and their IDs.

48.4 Transmission

A UART transmission sequence is started by triggering the STARTTX task.

Bytes are transmitted by writing to the TXD register. When a byte has been successfully transmitted the UART will generate a TXDRDY event after which a new byte can be written to the TXD register. A UART transmission sequence is stopped immediately by triggering the STOPTX task.

If flow control is enabled a transmission will be automatically suspended when CTS is deactivated and resumed when CTS is activated again, as illustrated in *Figure 155: UART transmission* on page 508.
A byte that is in transmission when CTS is deactivated will be fully transmitted before the transmission is suspended.

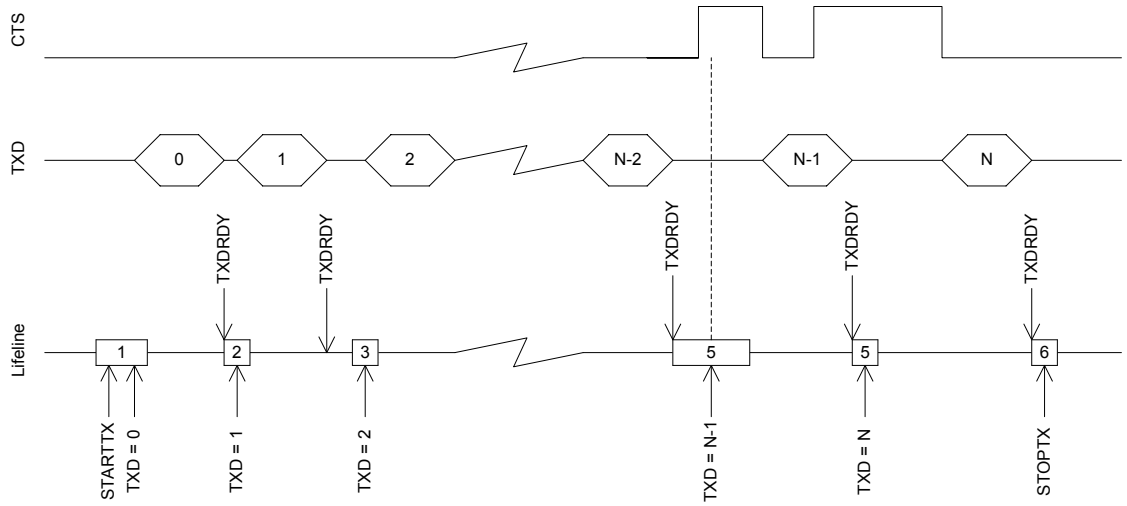


Figure 155: UART transmission

48.5 Reception

A UART reception sequence is started by triggering the STARTRX task.

The UART receiver chain implements a FIFO capable of storing six incoming RXD bytes before data is overwritten. Bytes are extracted from this FIFO by reading the RXD register. When a byte is extracted from the FIFO a new byte pending in the FIFO will be moved to the RXD register. The UART will generate an RXDRDY event every time a new byte is moved to the RXD register.

When flow control is enabled, the UART will deactivate the RTS signal when there is only space for four more bytes in the receiver FIFO. The counterpart transmitter is therefore able to send up to four bytes after the RTS signal is deactivated before data is being overwritten. To prevent overwriting data in the FIFO, the counterpart UART transmitter must therefore make sure to stop transmitting data within four bytes after the RTS line is deactivated.

The RTS signal will first be activated again when the FIFO has been emptied, that is, when all bytes in the FIFO have been read by the CPU, see *Figure 156: UART reception* on page 509.

The RTS signal will also be deactivated when the receiver is stopped through the STOPRX task as illustrated in *Figure 156: UART reception* on page 509. The UART is able to receive four to five additional bytes if they are sent in succession immediately after the RTS signal has been deactivated. This is possible because the UART is, even after the STOPRX task is triggered, able to receive bytes for an extended period of time dependent on the configured baud rate. The UART will generate a receiver timeout event (RXTO) when this period has elapsed.

To prevent loss of incoming data the RXD register must only be read one time following every RXDRDY event.

To secure that the CPU can detect all incoming RXDRDY events through the RXDRDY event register, the RXDRDY event register must be cleared before the RXD register is read. The reason for this is that the UART is allowed to write a new byte to the RXD register, and therefore can also generate a new event, immediately after the RXD register is read (emptied) by the CPU.

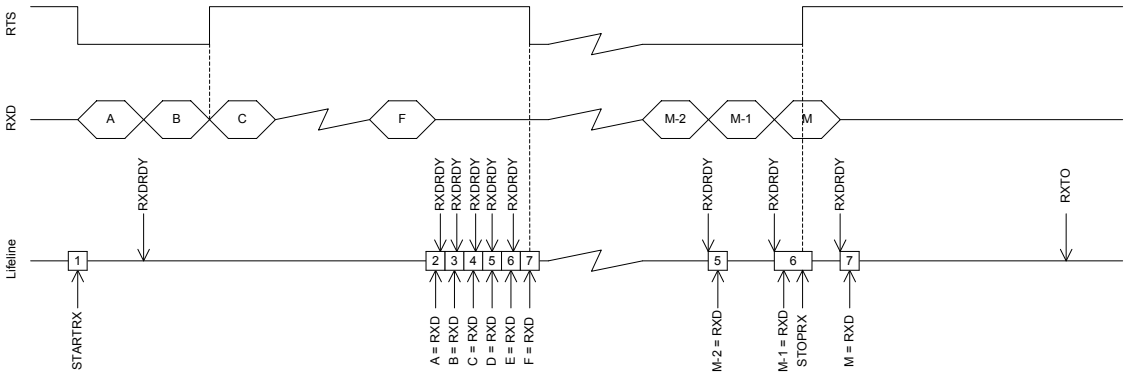


Figure 156: UART reception

As indicated in occurrence 2 in the figure, the RXDRDY event associated with byte B is generated first after byte A has been extracted from RXD.

48.6 Suspending the UART

The UART can be suspended by triggering the SUSPEND task.

SUSPEND will affect both the UART receiver and the UART transmitter, i.e. the transmitter will stop transmitting and the receiver will stop receiving. UART transmission and reception can be resumed, after being suspended, by triggering STARTTX and STARTRX respectively.

Following a SUSPEND task, an ongoing TXD byte transmission will be completed before the UART is suspended.

When the SUSPEND task is triggered, the UART receiver will behave in the same way as it does when the STOPRX task is triggered.

48.7 Error conditions

An ERROR event, in the form of a framing error, will be generated if a valid stop bit is not detected in a frame. Another ERROR event, in the form of a break condition, will be generated if the RXD line is held active low for longer than the length of a data frame. Effectively, a framing error is always generated before a break condition occurs.

48.8 Using the UART without flow control

If flow control is not enabled, the interface will behave as if the CTS and RTS lines are kept active all the time.

48.9 Parity configuration

When parity is enabled, the parity will be generated automatically from the even parity of TXD and RXD for transmission and reception respectively.

48.10 Registers

Table 121: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40002000	UART	UART0	Universal Asynchronous Receiver/ Transmitter		Deprecated

Table 122: Register Overview

Register	Offset	Description
TASKS_STARTRX	0x000	Start UART receiver
TASKS_STOPRX	0x004	Stop UART receiver
TASKS_STARTTX	0x008	Start UART transmitter
TASKS_STOPTX	0x00C	Stop UART transmitter
TASKS_SUSPEND	0x01C	Suspend UART
EVENTS_CTS	0x100	CTS is activated (set low). Clear To Send.
EVENTS_NCTS	0x104	CTS is deactivated (set high). Not Clear To Send.
EVENTS_RXDRDY	0x108	Data received in RXD
EVENTS_TXDRDY	0x11C	Data sent from TXD
EVENTS_ERROR	0x124	Error detected
EVENTS_RXTO	0x144	Receiver timeout
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x480	Error source
ENABLE	0x500	Enable UART
PSELRTS	0x508	Pin select for RTS
PSELTXD	0x50C	Pin select for TXD
PSELCTS	0x510	Pin select for CTS
PSELRXD	0x514	Pin select for RXD
RXD	0x518	RXD register
TXD	0x51C	TXD register
BAUDRATE	0x524	Baud rate
CONFIG	0x56C	Configuration of parity and hardware flow control

48.10.1 SHORTS

Address offset: 0x200

Shortcut register

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												B	A			
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	CTS_STARTRX			Shortcut between *EVENTS_CTS* event and *TASKS_STARTRX* task

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															B	A			
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
			Disabled	0																															
			Enabled	1																															
B	RW	NCTS_STOPRX																																	
			Disabled	0																															
			Enabled	1																															

48.10.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		F								E		D					C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	CTS																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	NCTS																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	RXDRDY																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
D	RW	TXDRDY																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
E	RW	ERROR																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
F	RW	RXTO																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															

48.10.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		F								E		D					C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	CTS																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	NCTS																																	
			Clear	1																															

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		F								E		D						C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																						**Description**									
			Disabled	0																						Read: Disabled									
			Enabled	1																						Read: Enabled									
C	RW	RXDRDY																								Write '1' to Disable interrupt on *EVENTS_RXDRDY* event									
			Clear	1																						Disable									
			Disabled	0																						Read: Disabled									
			Enabled	1																						Read: Enabled									
D	RW	TXDRDY																								Write '1' to Disable interrupt on *EVENTS_TXDRDY* event									
			Clear	1																						Disable									
			Disabled	0																						Read: Disabled									
			Enabled	1																						Read: Enabled									
E	RW	ERROR																								Write '1' to Disable interrupt on *EVENTS_ERROR* event									
			Clear	1																						Disable									
			Disabled	0																						Read: Disabled									
			Enabled	1																						Read: Enabled									
F	RW	RXTO																								Write '1' to Disable interrupt on *EVENTS_RXTO* event									
			Clear	1																						Disable									
			Disabled	0																						Read: Disabled									
			Enabled	1																						Read: Enabled									

48.10.4 ERRORSRC

Address offset: 0x480

Error source

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																						**Description**									
A	RW	OVERRUN																								Overrun error A start bit is received while the previous data still lies in RXD. (Previous data is lost.)									
			NotPresent	0																						Read: error not present									
			Present	1																						Read: error present									
B	RW	PARITY																								Parity error A character with bad parity is received, if HW parity check is enabled.									
			NotPresent	0																						Read: error not present									
			Present	1																						Read: error present									
C	RW	FRAMING																								Framing error occurred A valid stop bit is not detected on the serial data input after all bits in a character have been received.									
			NotPresent	0																						Read: error not present									
			Present	1																						Read: error present									
D	RW	BREAK																								Break condition The serial data input is '0' for longer than the length of a data frame. (The data frame length is 10 bits without parity bit, and 11 bits with parity bit.).									
			NotPresent	0																						Read: error not present									
			Present	1																						Read: error present									

48.10.5 ENABLE

Address offset: 0x500

Enable UART

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	ENABLE																																	
			Disabled	0																															
			Enabled	4																															

48.10.6 PSELRTS

Address offset: 0x508

Pin select for RTS

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PSELRTS		[0..31]																															
			Disconnected	0xFFFFFFFF																															

48.10.7 PSELTXD

Address offset: 0x50C

Pin select for TXD

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PSELTXD		[0..31]																															
			Disconnected	0xFFFFFFFF																															

48.10.8 PSELCTS

Address offset: 0x510

Pin select for CTS

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PSELCTS		[0..31]																															
			Disconnected	0xFFFFFFFF																															

48.10.9 PSELRXD

Address offset: 0x514

Pin select for RXD

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	PSELRXD		[0..31]																															
			Disconnected	0xFFFFFFFF																															

48.10.10 RXD

Address offset: 0x518

RXD register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	R	RXD																										RX data received in previous transfers, double buffered							

48.10.11 TXD

Address offset: 0x51C

TXD register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	W	TXD																										TX data to be transferred							

48.10.12 BAUDRATE

Address offset: 0x524

Baud rate

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x04000000				**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	BAUDRATE																										Baud-rate							
			Baud1200	0x0004F000																								1200 baud (actual rate: 1205)							
			Baud2400	0x0009D000																								2400 baud (actual rate: 2396)							
			Baud4800	0x0013B000																								4800 baud (actual rate: 4808)							
			Baud9600	0x00275000																								9600 baud (actual rate: 9598)							
			Baud14400	0x003B0000																								14400 baud (actual rate: 14414)							
			Baud19200	0x004EA000																								19200 baud (actual rate: 19208)							
			Baud28800	0x0075F000																								28800 baud (actual rate: 28829)							
			Baud38400	0x009D5000																								38400 baud (actual rate: 38462)							
			Baud57600	0x00EBF000																								57600 baud (actual rate: 57762)							
			Baud76800	0x013A9000																								76800 baud (actual rate: 76923)							
			Baud115200	0x01D7E000																								115200 baud (actual rate: 115942)							
			Baud230400	0x03AFB000																								230400 baud (actual rate: 231884)							
			Baud250000	0x04000000																								250000 baud							
			Baud460800	0x075F7000																								460800 baud (actual rate: 470588)							
			Baud921600	0x0EBED000																								921600 baud (actual rate: 941176)							
			Baud1M	0x10000000																								1Mega baud							

48.10.13 CONFIG

Address offset: 0x56C

Configuration of parity and hardware flow control

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																B	B	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**																															
A	RW	HWFC																										Hardware flow control							
			Disabled	0																								Disabled							
			Enabled	1																								Enabled							
B	RW	PARITY																										Parity							
			Excluded	0x0																								Exclude parity bit							

Bit number																																
Id																													B	B	B	A
Reset 0x00000000																													**0**	**0**	**0**	**0**
Id	**RW**	**Field**	**Value Id**	**Value**	**Description**																											
			Included	0x7	Include parity bit																											

48.11 Electrical Specification

48.11.1 UART electrical specification

Symbol	Description	Min.	Typ.	Max.	Units
f_{UART}	Baud rate for UART[36].			1000	kbps
I_{UART1M}	Run current at max baud rate.		55		µA
$I_{UART115k}$	Run current at 115200 bps.		55		µA
$I_{UART1k2}$	Run current at 1200 bps.		55		µA
$I_{UART,IDLE}$	Idle current for UART (STARTed, no XXX activity)		1		µA
$t_{UART,CTSH}$	CTS high time	1			µs
$t_{UART,START,LP}$	Time from STARTRX/STARTTX task to RX/TX active, low power mode		3		µs
$t_{UART,START,CL}$	Time from STARTRX/STARTTX task to RX/TX active, constant latency mode		1		µs

[36] Higher baud rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

49 Ordering information

This chapter contains information on IC marking, ordering codes, and container sizes.

49.1 IC marking

The nRF52832 IC package is marked like described below.

N	5	2	8	3	2
<P	P>	<V	V>	<H>	<P>
<Y	Y>	<W	W>	<L	L>

Figure 157: Package marking

49.2 Box labels

Here are the box labels used for the nRF52832.

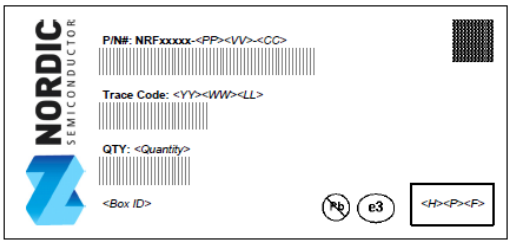


Figure 158: Inner box label

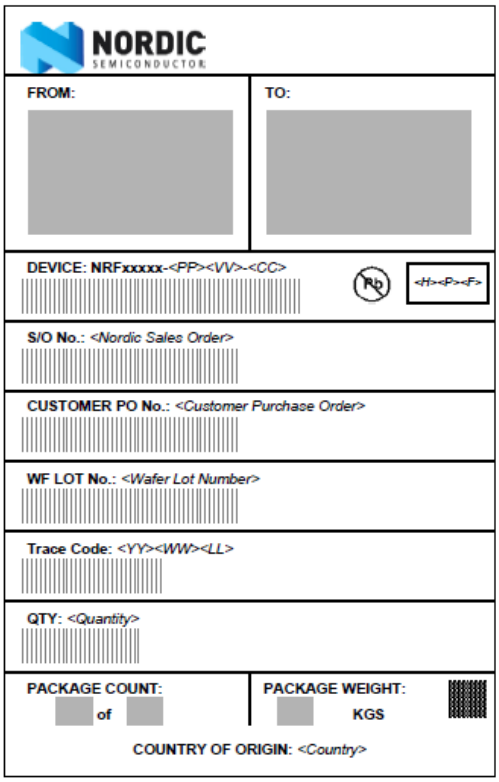


Figure 159: Outer box label

49.3 Order code

Here are the nRF52832 order codes and definitions.

n	R	F	5	2	8	3	2	-	<P	P>	<V	V>	-	<C	C>

Figure 160: Order code

Table 123: Abbreviations

Abbrevitation	Definition and implemented codes
N52/nRF52	nRF52 series product
832	Part code
<PP>	Package variant code
<VV>	Function variant code
<H><P><F>	Build code
	H - Hardware version code
	P - Production configuration code (production site, etc.)
	F - Firmware version code (only visible on shipping container label)
<YY><WW><LL>	Tracking code
	YY - Year code
	WW - Assembly week number
	LL - Wafer lot code
<CC>	Container code

49.4 Code ranges and values

Defined here are the nRF52832 code ranges and values.

Table 124: Package variant codes

<PP>	Packet	Size (mm)	Pin/Ball count	Pitch (mm)
QF	QFN	6 x 6	48	0.4
CE	CSP	3.0 x 3.2	54	0.4

Table 125: Function variant codes

<VV>	Flash (kB)	RAM (kB)
AA	512	64

Table 126: Hardware version codes

<H>	Description
[A . . Z]	Hardware version/revision identifier (incremental)

Table 127: Production configuration codes

<P>	Description
[0 . . 9]	Production device identifier (incremental)
[A . . Z]	Engineering device identifier (incremental)

Table 128: Production version codes

<F>	Description
[A . . N, P . . Z]	Version of preprogrammed firmware
[0]	Delivered without preprogrammed firmware

Table 129: Year codes

<YY>	Description
[15 . . 99]	Production year: 2015 to 2099

Table 130: Week codes

<WW>	Description
[1 . . 52]	Week of production

Table 131: Lot codes

<LL>	Description
[AA . . ZZ]	Wafer production lot identifier

Table 132: Container codes

<CC>	Description
R7	7" Reel
R	13" Reel
T	Tray

49.5 Product options

Defined here are the nRF52832 product options.

Table 133: nRF ICs order code

Order code	MOQ[37]	Comment
nRF52832-QFAA-R7	1000	Availability to be announced.
nRF52832-QFAA-R	3000	
nRF52832-QFAA-T	490	
nRF52832-CEAA-R7	1500	
nRF52832-CEAA-R	7000	
nRF52832-PREVIEW	1	QFN preview version, available now in limited quantities.

Table 134: Development tools order code

Order code	Description
nRF52-PREVIEW-DK	nRF52 Preview Development Kit

50 Reference circuitry

To ensure good RF performance when designing PCBs, it is highly recommended to use the PCB layouts and component values provided by Nordic Semiconductor.

Documentation for the different package reference circuits, including Altium Designer files, PCB layout files, and PCB production files can be downloaded from *www.nordicsemi.com*.

50.1 Schematic QFAA QFN48 with internal LDO setup

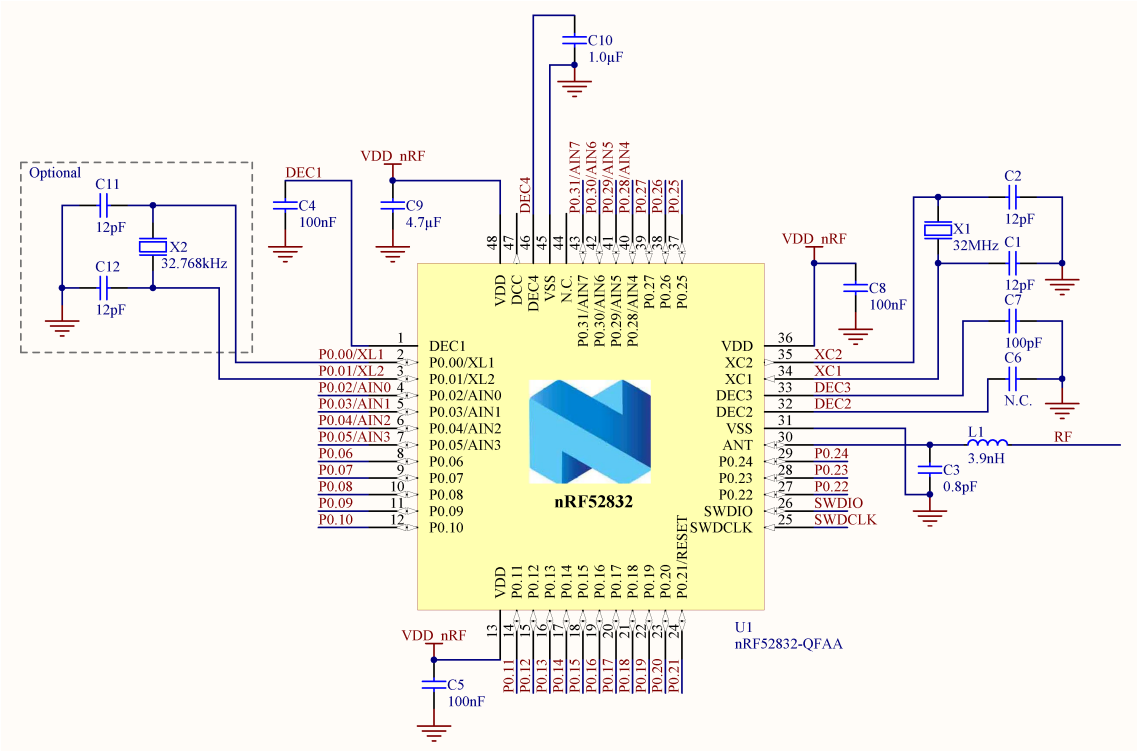


Figure 161: QFAA QFN48 with internal LDO setup

> **Important:** For PCB reference layouts, see the Reference Layout section on the Downloads tab for the nRF52832 on *www.nordicsemi.com*.

Table 135: Bill of material for QFAA QFN48 with internal LDO setup

Designator	Value	Description	Footprint
C1, C2, C11, C12	12 pF	Capacitor, NP0, ±2%	0402
C3	0.8 pF	Capacitor, NP0, ±5%	0402
C4, C5, C8	100 nF	Capacitor, X7R, ±10%	0402
C6	N.C.	Not mounted	0402
C7	100 pF	Capacitor, NP0, ±5%	0402
C9	4.7 µF	Capacitor, X5R, ±10%	0603
C10	1.0 µF	Capacitor, X7R, ±10%	0603
L1	3.9 nH	High frequency chip inductor ±5%	0402
U1	nRF52832-QFAA	Multi-protocol *Bluetooth* low energy and 2.4 GHz proprietary system on chip	QFN-48
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 3215, 32.768 kHz, 9 pF, ±20 ppm	XTAL_3215

50.2 Schematic QFAA QFN48 with DC/DC converter setup

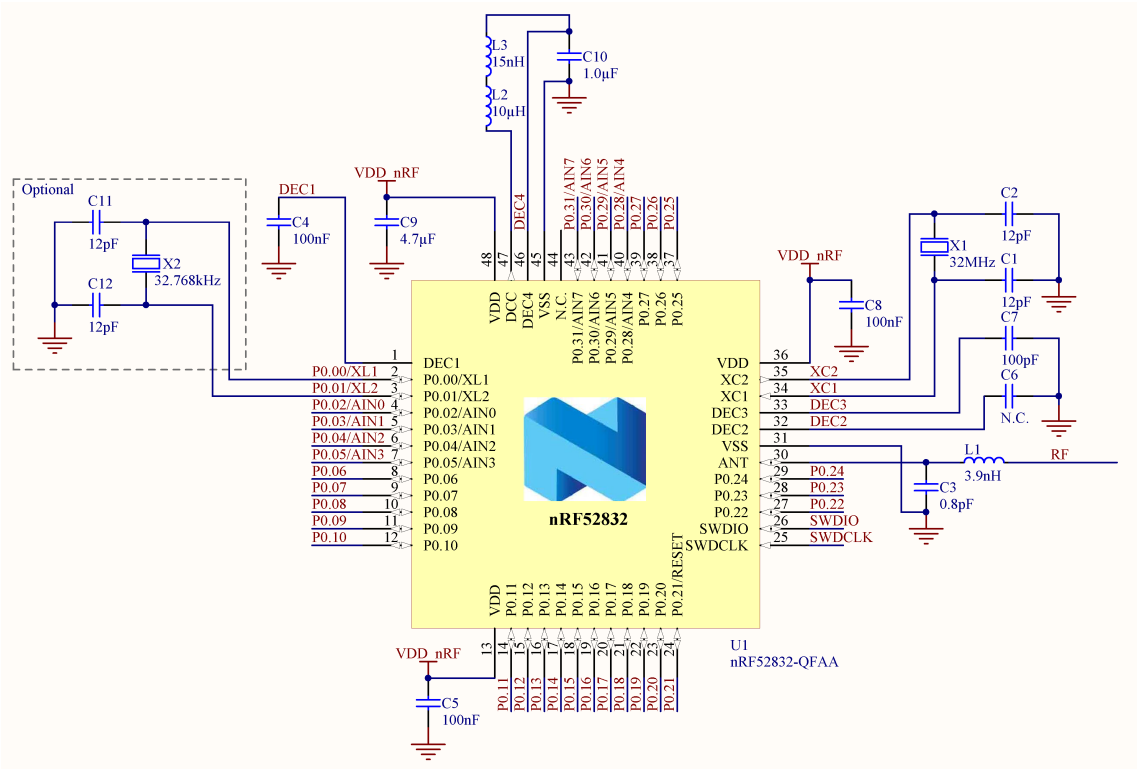


Figure 162: QFAA QFN48 with DC/DC converter setup

Important: For PCB reference layouts, see the Reference Layout section on the Downloads tab for nRF52832 on *www.nordicsemi.com*.

Table 136: Bill of material for QFAA QFN48 with DC/DC converter setup

Designator	Value	Description	Footprint
C1, C2, C11, C12	12 pF	Capacitor, NP0, ±2%	0402
C3	0.8 pF	Capacitor, NP0, ±5%	0402
C4, C5, C8	100 nF	Capacitor, X7R, ±10%	0402
C6	N.C.	Not mounted	0402
C7	100 pF	Capacitor, NP0, ±5%	0402
C9	4.7 µF	Capacitor, X5R, ±10%	0603
C10	1.0 µF	Capacitor, X7R, ±10%	0603
L1	3.9 nH	High frequency chip inductor ±5%	0402
L2	10 µH	Chip inductor, IDC,min = 50 mA, ±20%	0603
L3	15 nH	High frequency chip inductor ±10%	0402
U1	nRF52832-QFAA	Multi-protocol *Bluetooth* low energy and 2.4 GHz proprietary system on chip	QFN-48
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 3215, 32.768 kHz, 9 pF, ±20 ppm	XTAL_3215

50.3 Schematic QFAA QFN48 with DC/DC converter and NFC setup

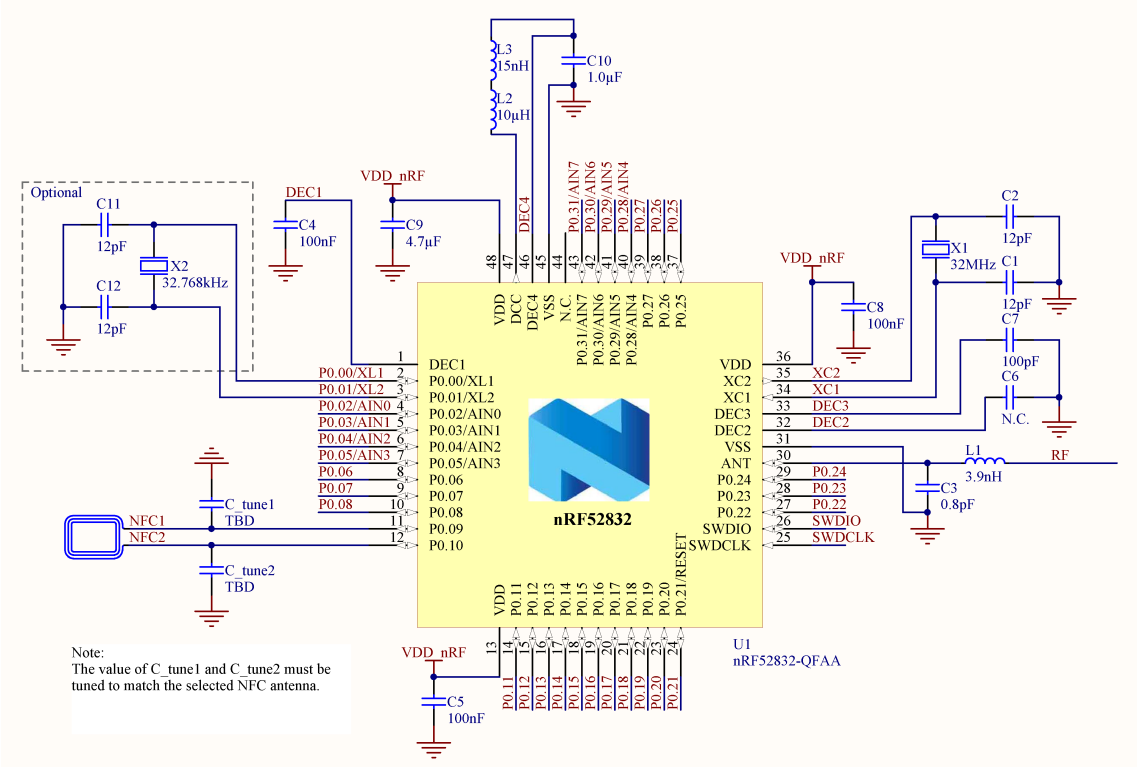


Figure 163: QFAA QFN48 with DC/DC converter and NFC setup

> **Important:** For PCB reference layouts, see the Reference Layout section on the Downloads tab for nRF52832 on *www.nordicsemi.com*.

Table 137: Bill of material for QFAA QFN48 with DC/DC converter and NFC setup

Designator	Value	Description	Footprint
C1, C2, C11, C12	12 pF	Capacitor, NP0, ±2%	0402
C3	0.8 pF	Capacitor, NP0, ±5%	0402
C4, C5, C8	100 nF	Capacitor, X7R, ±10%	0402
C6	N.C.	Not mounted	0402
C7	100 pF	Capacitor, NP0, ±5%	0402
C9	4.7 µF	Capacitor, X5R, ±10%	0603
C10	1.0 µF	Capacitor, X7R, ±10%	0603
C_{tune1}, C_{tune2}	TBD pF	Capacitor, NP0, ±5%	0402
L1	3.9 nH	High frequency chip inductor ±5%	0402
L2	10 µH	Chip inductor, IDC,min = 50 mA, ±20%	0603
L3	15 nH	High frequency chip inductor ±10%	0402
U1	nRF52832-QFAA	Multi-protocol *Bluetooth* low energy and 2.4 GHz proprietary system on chip	QFN-48
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 3215, 32.768 kHz, 9 pF, ±20 ppm	XTAL_3215

50.4 PCB guidelines

A well designed PCB is necessary to achieve good RF performance. A poor layout can lead to loss in performance or functionality.

A qualified RF layout for the IC and its surrounding components, including matching networks, can be downloaded from *www.nordicsemi.com*.

To ensure optimal performance it is essential that you follow the schematics- and layout references closely. Especially in the case of the antenna matching circuitry (components between device pin ANT and the antenna), any changes to the layout can change the behavior, resulting in degradation of RF performance or a need to change component values. All the reference circuits are designed for use with a 50 ohm single end antenna.

A PCB with a minimum of two layers, including a ground plane, is recommended for optimal performance. On PCBs with more than two layers, put a keep-out area on the inner layers directly below the antenna matching circuitry (components between device pin ANT and the antenna) to reduce the stray capacitances that influence RF performance.

A matching network is needed between the RF pin ANT and the antenna, to match the antenna impedance (normally 50 ohm) to the optimum RF load impedance for the chip. For optimum performance, the impedance for the matching network should be set as described in the recommended QFN48 package reference circuitry from *Schematic QFAA QFN48 with internal LDO setup* on page 519.

The DC supply voltage should be decoupled as close as possible to the VDD pins with high performance RF capacitors. See the schematics for recommended decoupling capacitor values. The supply voltage for the chip should be filtered and routed separately from the supply voltages of any digital circuitry.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections, and VDD bypass capacitors must be connected as close as possible to the IC. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to have via holes as close as possible to the VSS pads. A minimum of one via hole should be used for each VSS pin.

Fast switching digital signals should not be routed close to the crystal or the power supply lines. Capacitive loading of fast switching digital output lines should be minimized in order to avoid radio interference.

50.5 PCB layout example

The PCB layout shown below is a reference layout for the QFN package with internal LDO setup.

> **Important:** Pay attention to how the capacitor C3 is grounded. It is not directly connected to the ground plane, but grounded via VSS pin 31. This is done to create additional filtering of harmonic components.

For all available reference layouts, see the Reference Layout section on the Downloads tab for nRF52832 on *www.nordicsemi.com*.

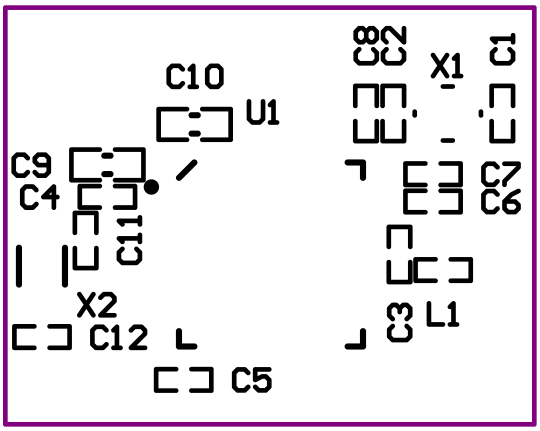


Figure 164: Top silk layer

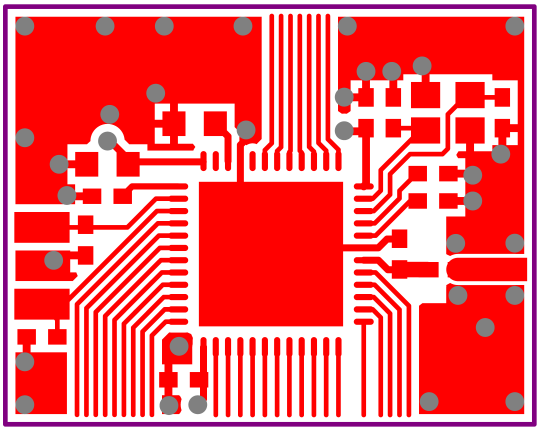


Figure 165: Top layer

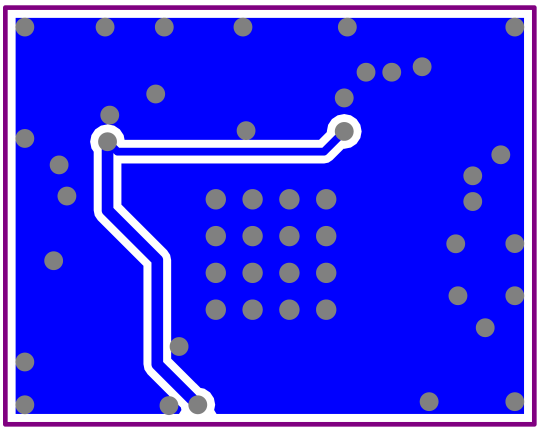


Figure 166: Bottom layer

Important: No components in bottom layer.

51 Liability disclaimer

Liability disclaimer

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