

## Features

- ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5 compliant for 2Mbps and 5Mbps CAN FD with wake-up pattern wake-up
- Fault voltage up to ±42V for bus pins.
- Integrated ESD Transient Voltage Suppressor (TVS) for bus pins
- TVS protection Immunities for bus terminals: ±8kV IEC 61000-4-2, Contact Discharge ±10kV IEC 61000-4-2, Air Discharge
- HBM ±5kV ESD protection for all pins
- MM ±400V ESD protection for all pins
- High CDM protection up to ±800V for all pins
- Latch up immunity up to ±400mA for all pins.
- High IEC 61000-4-4 Electrical Fast Transient (EFT) coupling immunity for bus pins under communication.
- Capability for both low ElectroMagnetic Emission (EME) and high ElectroMagnetic Immunity (EMI)
- Low standby current (12uA, typical) for power saving
- V<sub>IO</sub> input allows for direct interfacing with 1.8V to 5V microcontrollers.
- Ideal passive behavior to CAN bus with supply power off
- Transmit Data (TXD) dominant time-out function
- Undervoltage detection on the pins of V<sub>CC</sub> and V<sub>IO</sub> power
- Current-limitation and thermal shutdown for the driver design

## Applications

- Industrial Control and Instrumentation Networks
- Motor Control
- Building Automation
- Security Systems
- Medical Equipments
- Battery Control

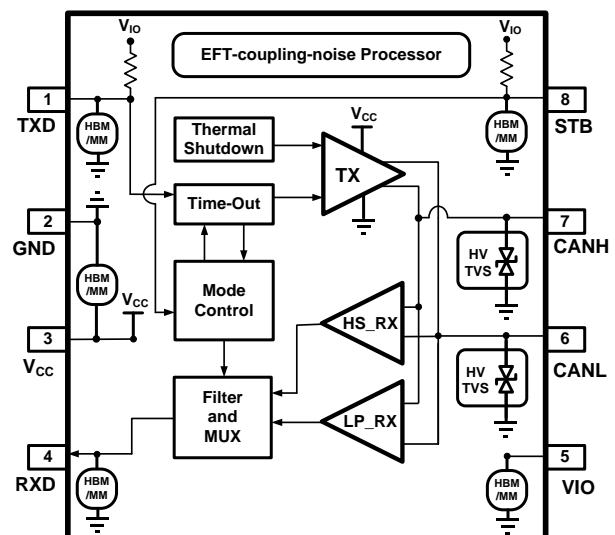
## Description

AZKN9125P is a ±8kV IEC 61000-4-2 protected Controller Area Network (CAN) transceiver IC. It serves as an interface between a CAN protocol controller (MCU) and the physical two-wire CAN bus. This device operates at 5V power supply and is fully compliant with ISO 11898-2:2016 standard for CAN FD application. The data rate of both driver and receiver is up to 5Mbps to support the high-speed application of the CAN FD.

AZKN9125P has the capabilities of both the ±40V common mode range of the receiver and the low EME of the transmitter, which has been patented as the Amazing's intellectual property. Moreover, the whole-chip design of the AZKN9125P can sustain high EFT coupling under communication.

AZKN9125P is a robust CAN transceiver, which features ±42V fault protection to sustain the DC short voltage on the bus pins. In addition, the whole-chip ESD protection immunity of AZKN9125P can sustain HBM ±5kV, MM ±400V and CDM ±800V, which is satisfied to overcome the ESD zapping under the worst manufacture environment.

## Functional Block of AZKN9125P



## Thermal Characteristics

PARAMETER	SYMBOL	Conditions	Value	UNIT
Thermal resistance from virtual junction to ambient	$\theta_{JA}$ <sup>[1]</sup>	$P_H=70mW$ under the air flow rate = 0 (m/s) in the ambient temperature <sup>[2]</sup>	90.97	°C/W

[1] The thermal resistance between virtual junction and ambient is  $\theta_{JA} = (T_J - T_{AMB})/P_H$ , where  $T_J$  is the virtual junction temperature and  $T_{AMB}$  is the ambient temperature under the power dissipation of  $P_H$ .

[2] According to JEDEC JESD51-2,-7 at natural convection on 2s2p board with two inner copper layers (Power/Ground thickness: 35  $\mu m$  ; Signal thickness: 70  $\mu m$ ).

## Absolute Maximum Ratings<sup>[1]</sup>

PARAMETER	SYMBOL	MIN	MAX	UNIT
DC voltage on CANH, CANL	$V_{CANH}, V_{CANL}$	-42	42	V
DC voltage between pin CANH and pin CANL	$V_{(CANH-CANL)}$	-50	50	V
DC voltage on all other pins	$V_X$	-0.3	7	V
Transient voltage on pins CANH and CANL For ISO 7637-2 pulse 1 <sup>[2]</sup>	$V_{trt1}$	-100	-	V
Transient voltage on pins CANH and CANL For ISO 7637-2 pulse 2a <sup>[2]</sup>	$V_{trt2a}$	-	75	V
Transient voltage on pins CANH and CANL For ISO 7637-2 pulse 3a <sup>[2]</sup>	$V_{trt3a}$	-150	-	V
Transient voltage on pins CANH and CANL For ISO 7637-2 pulse 3b <sup>[2]</sup>	$V_{trt3b}$	-	100	V
System-level ESD (IEC 61000-4-2, Contact Discharge) -- at pin CANH, CANL	$V_{ESD(contact)}$	-8	8	kV
System-level ESD (IEC 61000-4-2, Air-Gap Discharge) -- at pin CANH, CANL	$V_{ESD(air)}$	-10	10	kV
HBM ESD ( <u>H</u> uman <u>B</u> ody <u>M</u> odel; 100pF; 1.5 k $\Omega$ ) -- at any pins <sup>[3]</sup>	$V_{HBM}$	-5	5	kV
MM ESD ( <u>M</u> achine <u>M</u> odel; 200pF) -- at any pins <sup>[4]</sup>	$V_{MM}$	-400	400	V
CDM ESD ( <u>C</u> harged <u>D</u> evice <u>M</u> odel; field induced charge) <sup>[5]</sup> -- at any pins	$V_{CDM}$	-800	800	V
Virtual junction temperature	$T_J$	-40	150	°C
Storage temperature	$T_{STO}$	-55	150	°C

[1] Stresses listed above may cause permanent damage to the device under "Maximum Ratings". This is a stress rating only and functional operation of the device at those or other conditions above those indicated in the operational listings of this specification are not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

[2] Verified by thirty-party to ensure both CANH and CANL can withstand ISO 7637-2 automotive transient test pulses 1, 2a, 3a and 3b. The DUT is evaluated by the DCC method with coupling capacitance of 1nF connected between the pulse source and the cable of CANH and CANL respectively, which is shown in [Figure 7](#).

[3] Verified by thirty-party referred to AEC Q100-002

[4] Verified by thirty-party referred to AEC Q100-003

[5] Verified by thirty-party referred to AEC Q100-011

**Preliminary**

## DC Electrical Characteristics

( $V_{CC}=4.75V$  to  $5.25V$ ;  $V_{IO}=1.7V$  to  $5.25V$ ;  $T_{AMB}=-40^{\circ}C$  to  $+125^{\circ}C$ ;  $R_L=60\Omega$  unless otherwise noted. Typical values are at  $V_{CC}=5V$ ;  $V_{IO}=3.3V$  and  $T_{AMB}=25^{\circ}C$ )

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
<b>Internal Supply : <math>V_{CC}</math></b>						
Supply voltage	$V_{CC}$		4.75	-	5.25	V
Undervoltage detection voltage on pin $V_{CC}$	$V_{uvd(VCC)}$		3.5	4.0	4.5	V
Supply current	$I_{CC}$	Standby mode				
		$V_{TXD}=V_{IO}$	-	12	20	$\mu A$
		Normal mode				
		Recessive; $V_{TXD}=V_{IO}$	2.5	5	12	mA
		Dominant; $V_{TXD}=0V$	20	40	70	mA
		Dominant; $V_{TXD}=0V$ ; Short circuit on bus lines; $-3V < (V_{CANH}=V_{CANL}) < +18V$	2.5	90	120	mA
<b>Internal Supply : <math>V_{IO}</math></b>						
Supply voltage on pin $V_{IO}$	$V_{IO}$		1.7	-	5.5	V
Undervoltage detection voltage on pin $V_{IO}$	$V_{uvd(VIO)}$		-	1.4	-	V
Supply current	$I_{IO}$	Standby mode				
		$V_{TXD}=V_{IO}$	-	0.07	1	$\mu A$
		Normal mode				
		Recessive; $V_{TXD}=V_{IO}$	-	20	80	$\mu A$
		Dominant; $V_{TXD}=0V$	-	120	350	$\mu A$
<b>Bus lines : CANH and CANL</b>						
Dominant output voltage	$V_{O(dom)}$	$V_{TXD}=0V$ ; $t < t_{to(dom)TXD}$				
		pin CANH; $R_L = 50\Omega$ to $65\Omega$	2.75	3.5	4.5	V
		pin CANL; $R_L = 50\Omega$ to $65\Omega$	0.5	1.5	2.25	V
Transmitter dominant voltage symmetry	$V_{dom(TX)sym}$	$V_{dom(TX)sym} = V_{CC} - V_{CANH} - V_{CANL}$	-400	-	+400	mV
Transmitter voltage symmetry	$V_{TXsym}$	$V_{TXsym} = V_{CANH} + V_{CANL}$ ; [2] [3] $C_{SPLIT} = 4.7nF$	$0.9V_{CC}$	-	$1.1V_{CC}$	
Bus differential output voltage	$V_{O(dif)bus}$	$V_{TXD}=0V$ ; $t < t_{to(dom)TXD}$				
		$R_L = 50\Omega$ to $65\Omega$	1.5	-	3	V



*Preliminary*

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
		$R_L = 45 \Omega$ to $70 \Omega$	1.4	-	3.3	V
		$R_L = 2240 \Omega$	1.5	-	5	V
		recessive; no load				
		Normal mode; $V_{TXD}=V_{IO}$	-50	-	+50	mV
		Standby mode	-0.2	-	+0.2	V
Recessive output voltage	$V_{O(rec)}$	Normal mode; $V_{TXD}=V_{IO}$ ; no load	2	$0.5V_{CC}$	3	V
		Standby mode; no load	-0.1	-	+0.1	V
Receiver recessive voltage	$V_{rec(RX)}$	$V_{CM(CAN)} = -40V$ to $+40V$ <sup>[1]</sup>				
		Normal mode	-4	-	0.5	V
		Standby mode	-4	-	0.4	V
Receiver dominant voltage	$V_{dom(RX)}$	$V_{CM(CAN)} = -40V$ to $+40V$ <sup>[1]</sup>				
		Normal mode	0.9	-	9	V
		Standby mode	1.15	-	9	V
Differential receiver threshold voltage	$V_{th(RX)dif}$	$V_{CM(CAN)} = -40V$ to $+40V$ <sup>[1]</sup>				
		Normal mode	0.5	0.7	0.9	V
		Standby mode	0.4	0.78	1.15	V
Differential receiver hysteresis voltage	$V_{hys(RX)dif}$	$V_{CM(CAN)} = -40V$ to $+40V$ <sup>[1]</sup> Normal mode		120		mV
Dominant short-circuit output current	$I_{O(SC)dom}$	$V_{TXD}=0V$ ; $t < t_{to(dom)TXD}$ ; $V_{CC}=5V$				
		Pin CANH; $V_{CANH}=-15V$ to $40V$	-115	-80		mA
		Pin CANL; $V_{CANL}=-15V$ to $40V$		80	115	mA
Recessive short-circuit output current	$I_{O(SC)rec}$	Normal mode; $V_{TXD}=V_{IO}$ $V_{CANH}=V_{CANL}=-27V$ to $+32V$	-5	-	+5	mA
Leakage current	$I_L$	$V_{CC}=V_{IO}=0V$ or $V_{CC}=V_{IO}$ = shorted to ground via $47 k\Omega$ ; $V_{CANH}=V_{CANL}=5V$	-5	-	+5	$\mu A$
Input resistance	$R_i$	$-2V \leq V_{CANH} \leq +7V$ ; $-2V \leq V_{CANL} \leq +7V$	9	15	28	$k\Omega$
Input resistance deviation	$\Delta R_i$	$0V \leq V_{CANH} \leq +5V$ ; $0V \leq V_{CANL} \leq +5V$ <sup>[2]</sup>	-3	-	+3	%
Differential input resistance	$R_{i(dif)}$	$-2V \leq V_{CANH} \leq +7V$ ; $-2V \leq V_{CANL} \leq +7V$	19	30	52	$k\Omega$
Common-mode input capacitance	$C_{i(cm)}$	<sup>[2]</sup>	-	-	20	pF
Differential input capacitance	$C_{i(dif)}$	<sup>[2]</sup>	-	-	10	pF
<b>Temperature Protection</b>						
Shutdown temperature	$T_{J(sd)}$	<sup>[2]</sup>	-	190	-	$^{\circ}C$

**Preliminary**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
<b>Standby mode control input : STB</b>						
High-level input voltage	$V_{IH}$		$0.7V_{IO}$	-	$V_{IO}+0.3$	V
Low-level input voltage	$V_{IL}$		$-0.3V_{IO}$	-	$+0.3V_{IO}$	V
High-level input current	$I_{IH}$	$V_{STB}=V_{IO}$	-1	-	+1	$\mu A$
Low-level input current	$I_{IL}$	$V_{STB}=0V$	-15	-4	-0.7	$\mu A$
<b>Transmit data input : TXD</b>						
High-level input voltage	$V_{IH}$		$0.7V_{IO}$	-	$V_{IO}+0.3$	V
Low-level input voltage	$V_{IL}$		$-0.3V_{IO}$	-	$+0.3V_{IO}$	V
High-level input current	$I_{IH}$	$V_{TXD}=V_{IO}$	-5	-	+5	$\mu A$
Low-level input current	$I_{IL}$	$V_{TXD}=0V$	-300	-90	-10	$\mu A$
Input capacitance	$C_i$	[2]	-	5	10	pF
<b>Receive data output : RXD</b>						
High-level output current	$I_{OH}$	$V_{RXD}=V_{IO}-0.4V$	-11	-4.5	-1	mA
Low-level output current	$I_{OL}$	$V_{RXD}=0.4V$ ; bus dominant	0.7	6.5	15	mA

[1]  $V_{CM(CAN)}$  is the common mode voltage of CANH and CANL.

[2] Not tested in production; guaranteed by design.

[3] The test circuit used to measure the bus output voltage symmetry (which includes  $C_{SPLIT}$ ) is shown in [Figure 8](#).

## Switching Characteristics

( $V_{CC}=4.75V$  to  $5.25V$ ;  $V_{IO}=1.7V$  to  $5.25V$ ;  $T_{AMB}=-40^{\circ}C$  to  $+125^{\circ}C$ ;  $R_L=60\Omega$  unless otherwise noted. Typical values are at  $V_{CC}=5V$ ;  $V_{IO}=3.3V$  and  $T_{AMB}=25^{\circ}C$ )

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
<b>Transceiver timing; pins CANH, CANL, TXD and RXD; see <a href="#">Figure 1</a> and <a href="#">Figure 6</a></b>						
Delay time from TXD to bus dominant	$t_{d(TXD-busdom)}$	Normal mode	-	40	-	ns
Delay time from TXD to bus recessive	$t_{d(TXD-busrec)}$	Normal mode	-	55	-	ns
Delay time from bus dominant to RXD	$t_{d(busdom-RXD)}$	Normal mode	-	65	-	ns
Delay time from bus recessive to RXD	$t_{d(busrec-RXD)}$	Normal mode	-	85	-	ns
Propagation delay from TXD to RXD	$t_{PD(TXD-RXD)}$	Normal mode	50	-	230	ns
Bit time on Bus	$t_{bit(Bus)}$	$t_{bit(TXD)}=500ns$ [1]	435	-	530	ns
		$t_{bit(TXD)}=200ns$ [1]	155	-	210	ns
Bit time on pin RXD	$t_{bit(RXD)}$	$t_{bit(TXD)}=500ns$ [1]	400	-	550	ns
		$t_{bit(TXD)}=200ns$ [1]	120	-	220	ns
Receiver timing symmetry	$\Delta t_{Rec}$	$\Delta t_{Rec} = t_{bit(RXD)} - t_{bit(Bus)}$				
		$t_{bit(TXD)}=500ns$	-65	-	+40	ns
		$t_{bit(TXD)}=200ns$	-45	-	+15	ns
TXD dominant time-out time	$t_{to(dom)TXD}$	$V_{TXD}=0V$ ; Normal mode	0.8	3	8	ms
Bus dominant wake-up time	$t_{wake(busdom)}$	Standby mode [2]	0.5	1.7	3	$\mu s$
Bus recessive wake-up time	$t_{wake(busrec)}$	Standby mode [2]	0.5	1.7	3	$\mu s$



*Preliminary*

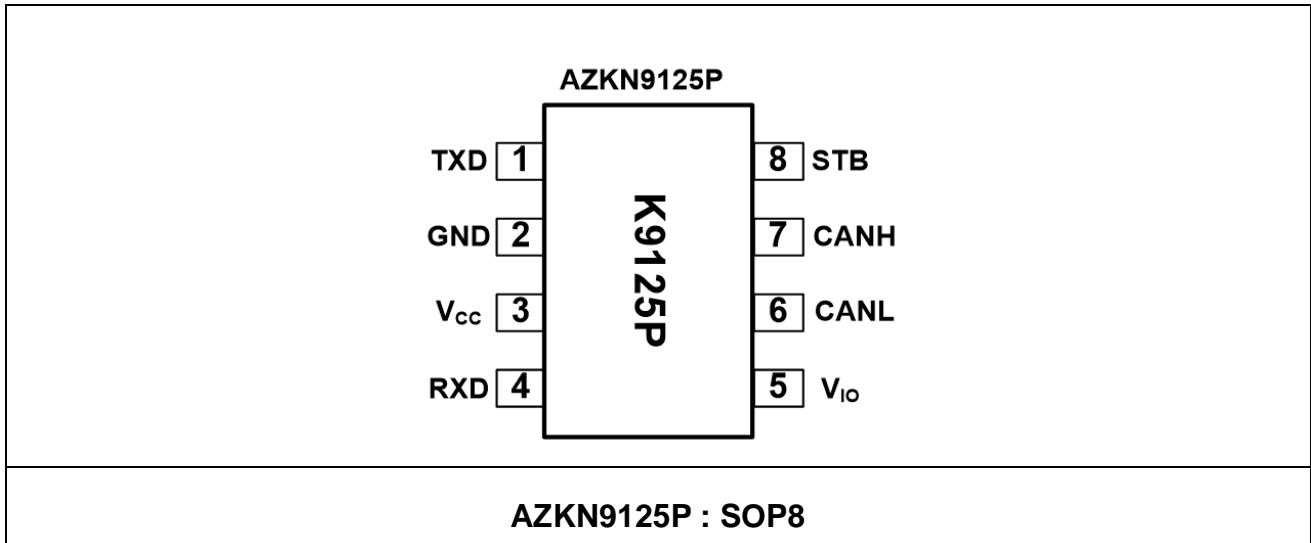
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Bus wake-up time-out time	$t_{to(wake)bus}$	Standby mode <sup>[2]</sup>	0.8	3.5	8	ms
Bus wake-up filter time	$t_{filtr(wake)bus}$	Standby mode <sup>[2]</sup>	0.5	1	3	μs
Standby to normal mode delay time	$t_{d(stb-norm)}$	<sup>[3]</sup>	20	34	55	μs

[1] See [Figure 2](#).

[2] See [Figure 3](#).

[3] See [Figure 4](#).

## Pin Configuration



## Pin Function Description

Pin Number	Mnemonic	Function
1	TXD	Transmit data input
2	GND	Ground supply
3	V <sub>CC</sub>	Supply voltage
4	RXD	Receive data output; reads out data from the bus lines
5	V <sub>IO</sub>	Supply voltage for I/O level adapter.
6	CANL	LOW-level CAN bus line
7	CANH	HIGH-level CAN bus line
8	STB	Standby mode control input



## Detail Description of Part

AZKN9125P is a high-speed CAN transceiver compliant with the ISO 11898-2:2016. The  $V_{IO}$  supply pin should be connected to supply voltage of microcontroller (see [Figure 5](#)). The  $V_{IO}$  allows the supply range from 1.7V to 5.5V of the microcontroller to adjust the I/O signal levels of the TXD, RXD, and STB pins

## Operation Modes

The normal and standby are two operating modes for AZKN9125P, which are selected by STB pin. The detail description of the operating modes related to both bus pins and RXD pin is listed in the [Table 1](#).

### ● Normal mode

When STB pin ties to logic LOW, AZKN9125P will switch to the normal mode. In the normal mode, the driver will translate the logic state of TXD to differential output of HS CAN. The data rate of driver is up to the 5Mbps with both the controlled slew rate and common mode voltage, which is Amazing's property. So that the driver performs the low common mode noise and has the low EME performance, which is evaluated by IEC 61967-4.

The normal receiver with the ±40V common mode range operates in the normal mode, which is also Amazing's property. The normal receiver translates the differential signal of HS CAN to the digital output of RXD with data rate up to 5Mbps. The EM Immunity of normal receiver is evaluated by IEC 62132-4.

The loop delay symmetry from TXD to RXD is optimized by both driver and normal receiver in AZKN9125P.

### ● Standby mode

When the STB ties to logic HIGH, AZKN9125P will switch to the standby mode. In the standby mode, both the driver and normal receiver are turned off so that the bus pins are biased to GND to save  $V_{CC}$  power. Only the low power receiver operates to monitor the activity of the bus so as to inform the microcontroller if go to the normal mode or not.

In standby mode, the wake-up filter on the output of the low-power receiver ensures that only bus dominant and bus recessive states that persist longer than  $t_{\text{filtr(wake)bus}}$  are reflected on pin RXD after

a wake-up pattern has been detected. Therefore, the data on RXD is not exact but is a wake-up signal to microcontroller.

The bus pins of AZKN9125P bias to GND via input resistor so that it is passive behavior in the standby mode.

### ● Remote wake-up via the CAN bus

For avoiding spurious wake-up event, AZKN9125P could be awake from standby mode only when a wake-up pattern defined by ISO 11898-2:2016 is detected on bus.

This dedicated wake-up pattern consists of three states.

- a dominate state  $> t_{\text{wake(busdom)}}$  followed by
- a recessive state  $> t_{\text{wake(busrec)}}$  followed by
- a dominate state  $> t_{\text{wake(busdom)}}$

Before a complete wake-up pattern is detected, dominate and recessive bits which are shorter than  $t_{\text{wake(busdom)}}$  and  $t_{\text{wake(busrec)}}$  respectively will be ignored and pin RXD will be kept logic high.

This dominate-recessive-dominate pattern must be received within  $t_{\text{to(wake)bus}}$  (see [Figure 3](#)). Otherwise, the internal wake-up logic will be reset Therefore, the complete wake-up pattern must be resent again to trigger a valid wake-up event.

After a complete wake-up pattern is detected, bus dominant or bus recessive states that persist longer than  $t_{\text{filtr(wake)bus}}$  will be reflected on pin RXD. AZKN9125P will remain in standby mode until microcontroller ties STB pin to logic LOW.

## Fail-safe Protection

### ● TXD dominant time-out function

The function of "TXD dominant time-out" prevents the failure of the hardware or software from keeping the bus in the dominate state. The failure causes the bus to be blocked all communication. The timer of "TXD dominate time-out" is started when TXD pin is set to LOW. If the time of TXD pin in the LOW state is longer than  $t_{\text{to(dom)TXD}}$ , the driver will be turn off to release the bus. The timer of "TXD dominate time-out" will be reset when TXD pin is set to HIGH. Therefore, the minimum data rate of 25kbps is defined by the function of "TXD dominant time-out".



**Preliminary**

● **Pull-up of TXD and STB input pins**

The pins of both TXD and STB with internal pull-ups to  $V_{IO}$  are safe-guarantee design due to one or both of these pins in floating condition. When TXD pin is internally pulled up, the transmitter is forced into the recessive state. When STB pin is internally pulled up, AZKN9125P is forced into the low power standby mode. By the way, the pull-up currents will be generated if the pins are biased to low state. In standby mode, both pins should be held HIGH to reduce the current.

● **Undervoltage detection on pins  $V_{CC}$  and  $V_{IO}$**

When  $V_{CC}$  drops below the  $V_{CC}$  undervoltage detection level  $V_{uvd(VCC)}$  or  $V_{IO}$  drops below the  $V_{IO}$  undervoltage detection level  $V_{uvd(VIO)}$ , the transceiver will switch to off mode. The logic state of STB and TXD pins will be ignored and the transceiver will switch off and disengage from the bus (zero load) until  $V_{CC}$  and  $V_{IO}$  have been recovered. The undervoltage detection is the protection function to avoid the abnormal operation of  $V_{CC}$  and  $V_{IO}$  power.

● **Overtemperature protection**

When the virtual junction temperature exceeds the shutdown junction temperature,  $T_{J(sd)}$ , the output of the drivers will be disabled to protect AZKN9125P from burn out issue. In this state, both CANH and CANL are biased to the recessive level no matter what the logic level of TXD pin is and the receiver still remains operational. When the temperature falls below  $T_{J(sd)}$ , the overtemperature protection will be released. The typical  $T_{J(sd)}$  is designed as 190°C under  $V_{CC} = 5.0V$ .

**High-Immunity Communication**

● **High EFT coupling Immunity**

AZKN9125P has high EFT coupling immunity on the bus line under the normal operation. The output

of transmitter (CANH and CANL) and the output of receiver (RXD) could be recovered after next bit when the high voltage the pulse of EFT coupled to the bus line through the coupling box (CCC method), as [Figure 7](#). So the AZKN9125P has more ability to communicate with low Bit-Error-Rate (BER) under the high noise environment.

**High Protection for All Pins**

● **±8kV System-level ESD for CANH and CANL**

AZKN9125P is embedded high voltage ±42V TVS on the pins of CANH and CANL to achieve IEC 61000-4-2 contact ±8kV of the system-level ESD protection. In the evaluation of system-level ESD, both CANH and CANL of AZKN9125P are zapped by ESD gun referred to GND on the evaluation board.

● **HBM 5kV, MM 400V and 800V CDM for all pins**

To achieve the high reliability and high assembly yield rate, AZKN9125P have high ESD specification of the component-level for both HBM and MM. With the high robust whole-chip ESD protection, AZKN9125P can still sustain no matter the ESD pulse comes from power pin or the I/O pins. For the IC self-discharge issue, the CDM protection level of AZKN9125P is up to ±800V.

Table 1. Operating modes

STB Pin		Low	High
Mode		Normal	Standby
Bus pins (CANH, CANL)		Dominant / Recessive	Bias to GND <sup>[1]</sup>
RXD	High	Recessive	No Wake-up
	Low	Dominant	Wake-up <sup>[1]</sup>

[1] In standby mode, the standby RX is active to wake-up MCU.



Preliminary

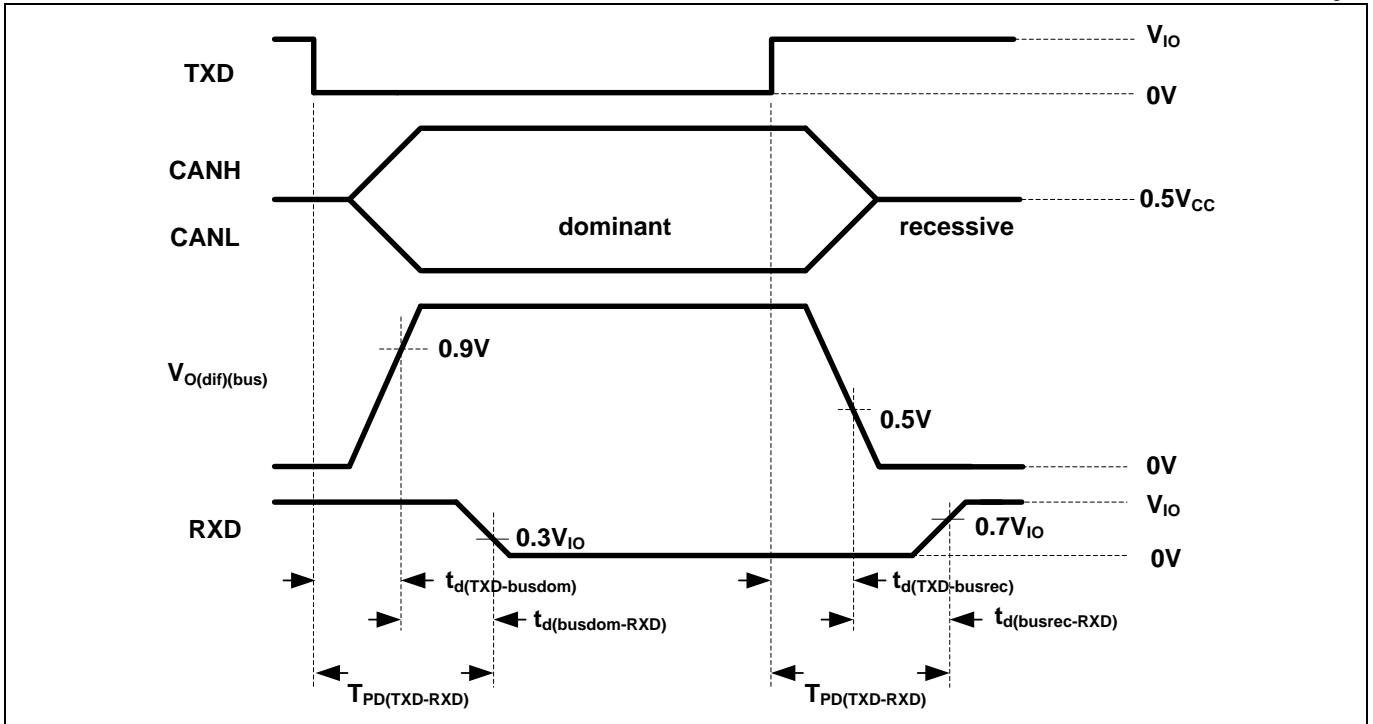


Figure 1. Timing diagram of the CAN transceiver.

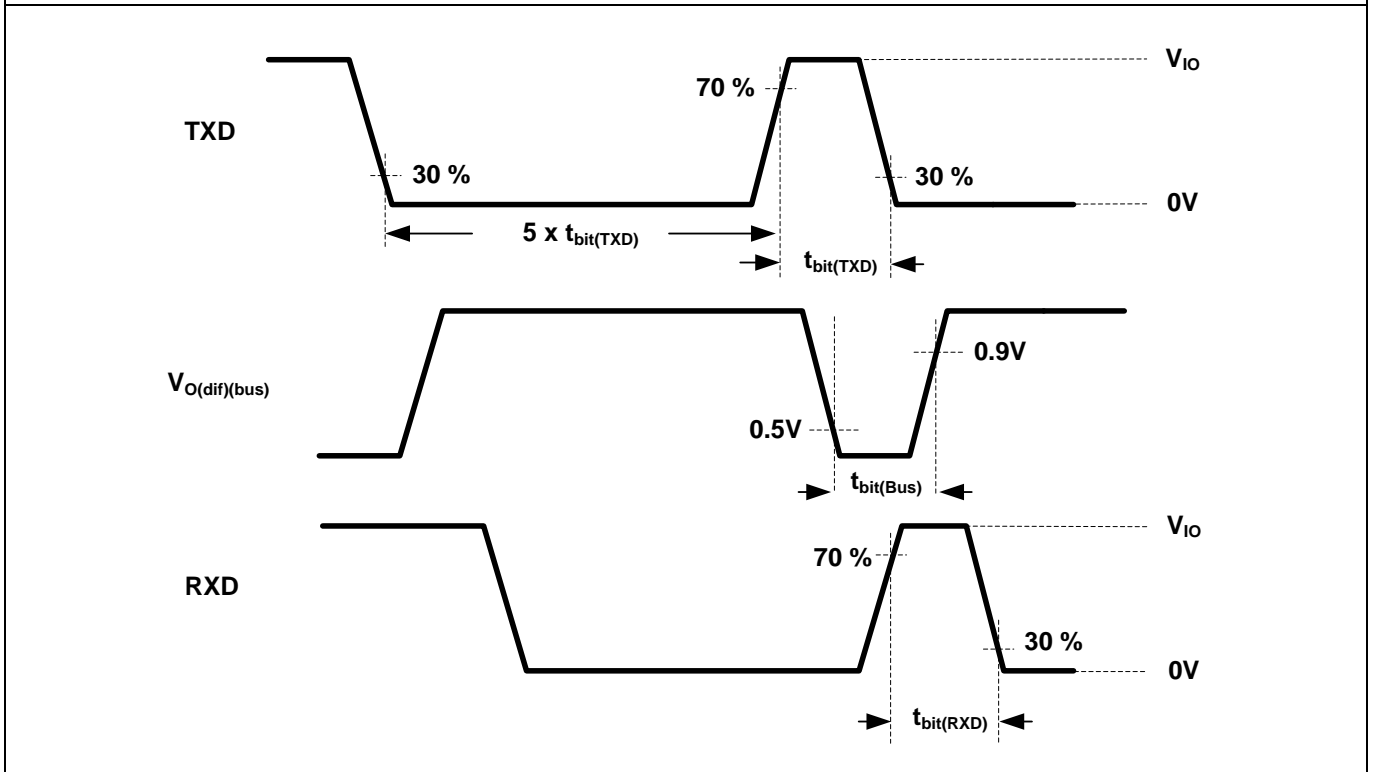


Figure 2. Timing diagram for loop delay symmetry.



Preliminary

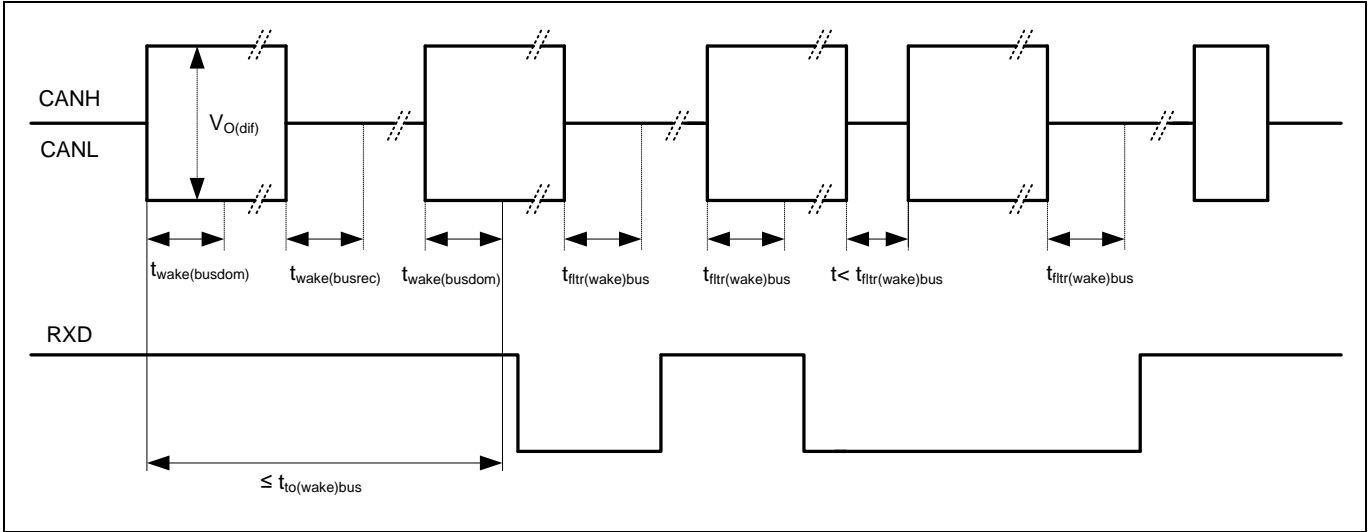


Figure 3. Timing diagram for wake-up pattern

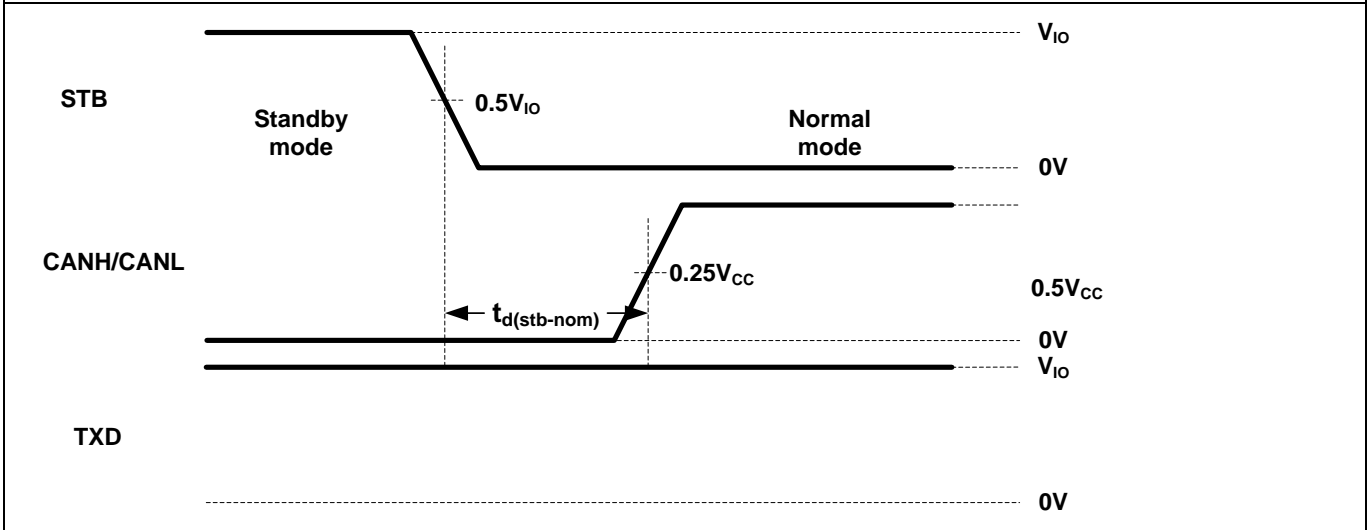


Figure 4. Timing diagram for the delay of the standby to normal mode.

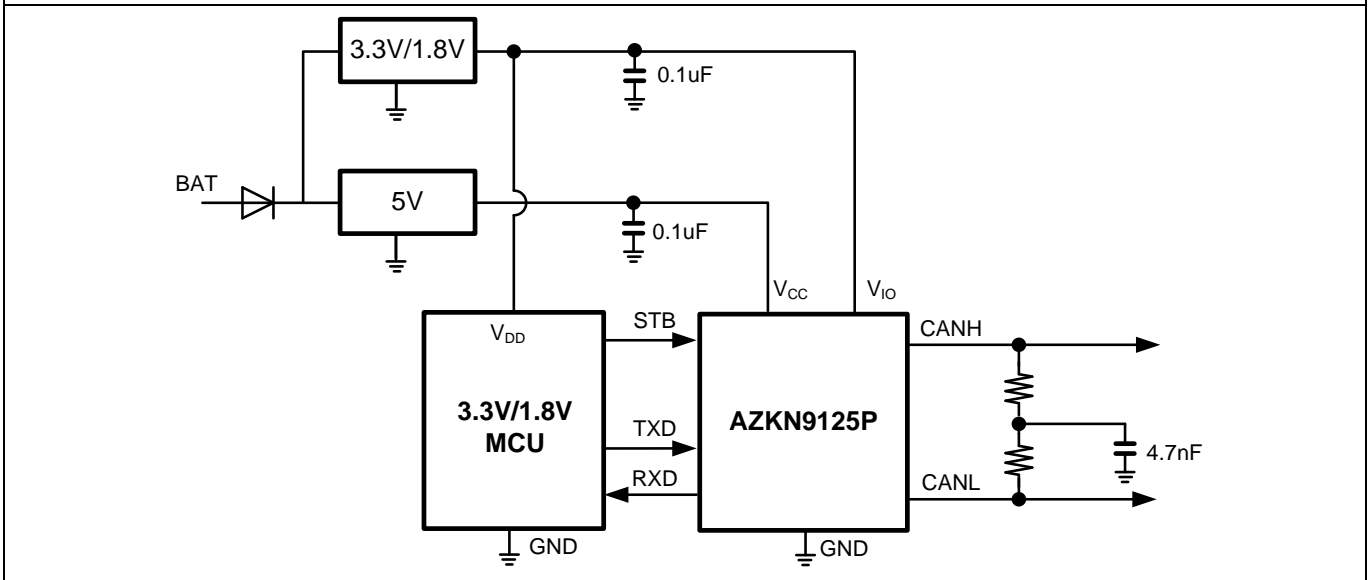


Figure 5. Typical application circuit for AZKN9125P with 3.3V or 1.8V MCU.



Preliminary

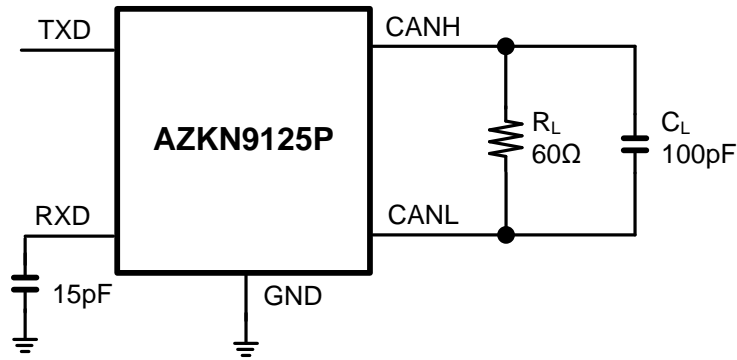


Figure 6. CAN transceiver timing test circuit.

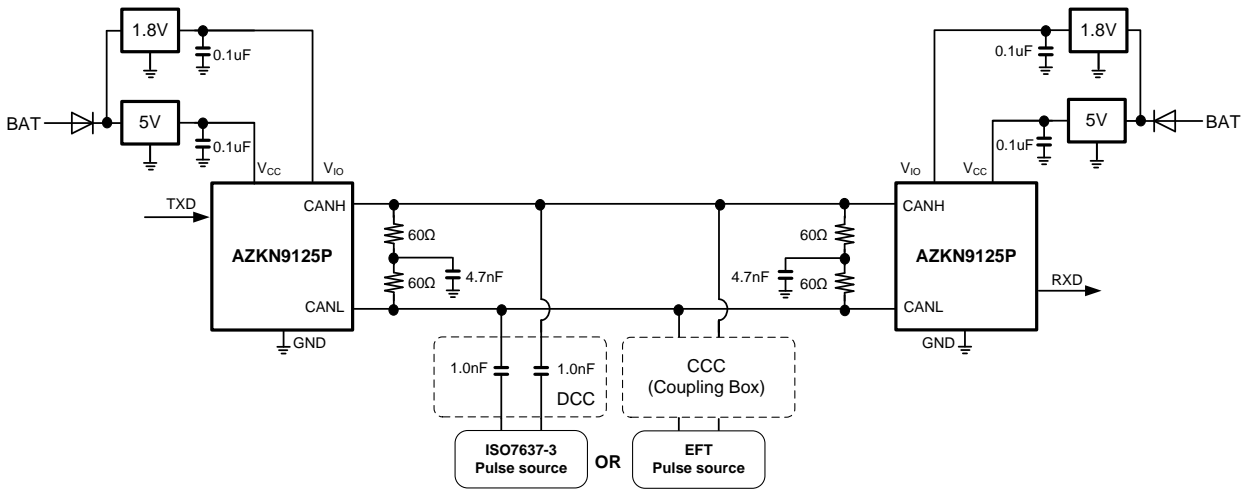


Figure 7. EFT coupling test circuit for AZKN9125P.

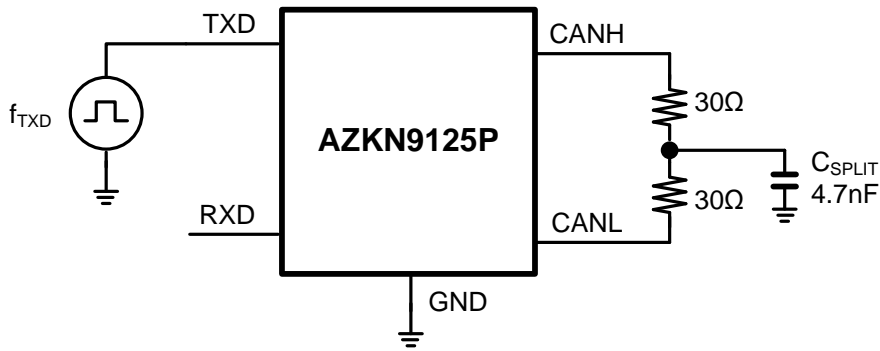
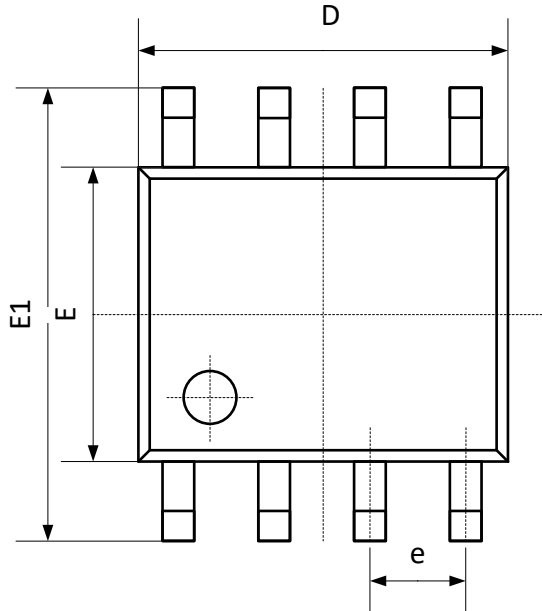


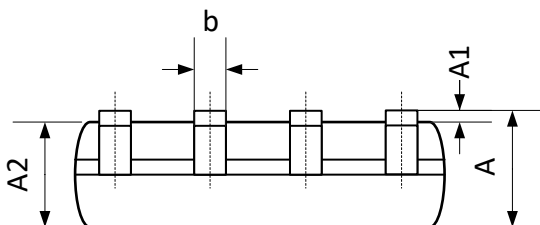
Figure 8. Test circuit for measuring transmitter driver symmetry.

## Mechanical Details

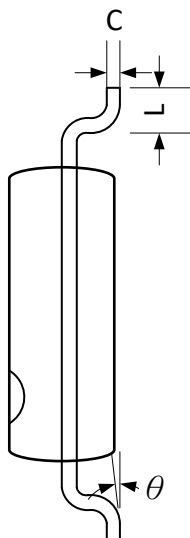
**PACKAGE DIAGRAMS**  
**TOP VIEW**



**SIDE VIEW**



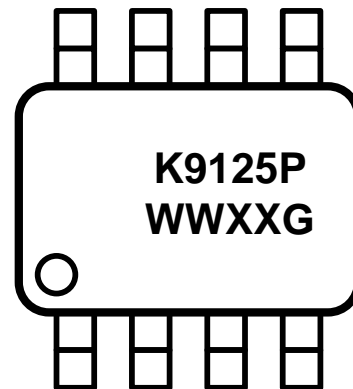
**END VIEW**



**PACKAGE DIMENSIONS**

Symbol	Millimeters		Inches	
	min	Max	min	max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.55	0.049	0.061
b	0.33	0.51	0.013	0.020
C	0.17	0.26	0.007	0.010
D	4.70	5.10	0.185	0.201
E	3.70	4.10	0.146	0.161
E1	5.80	6.20	0.228	0.244
e	1.27 BSC		0.05BSC	
L	0.40	1.27	0.016	0.050
Θ	0	8	0	8

## MARKING CODE



K9125P = Device Code

WW = Date Code ; XX = Control Code

G = Green Part Indication

Part Number	Marking Code
AZKN9125P.RDG	K9125P WWXXG



*Preliminary*

### Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZKN9125P.RDG	Green	T/R	13 inch	2,500/reel	1 reel=2,500/box	5 boxes =12,500/carton

### Revision History

Revision Date	Modification Description
2023/01/11	Preliminary version Release