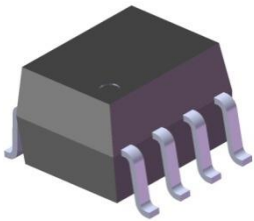


8 PIN SOP 3.3V HIGH SPEED - 15MBit/s LOGIC GATE PHOTOCOUPLER EL071L



Features

- Compliance Halogen Free
(Br < 900 ppm, Cl < 900 ppm, Br+Cl < 1500 ppm)
- 3.3 and 5 V CMOS compatibility
- High speed 15Mbit/s
- 10kV/μs min. common mode transient immunity
- Guaranteed performance from -40 to 110°C
- Logic gate output, Fan out 10
- High isolation voltage between input and output (Viso=3750 V rms)

Description

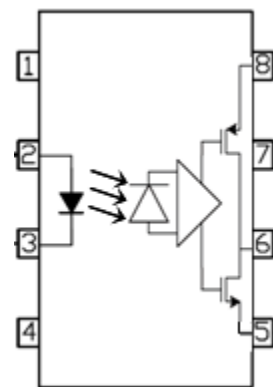
The EL071L consists of an infrared emitting diode optically coupled to a CMOS detector ICs. It is packaged in a 8-pin SOP package and is suitable for surface mounting technology.

Applications

- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer peripheral interface
- High speed logic ground isolation

Preliminary

Schematic



Pin Configuration

- 1, No Connection
- 2, Anode
- 3, Cathode
- 4, No Connection
- 5, Gnd
- 6, Vout
- 7, No Connection
- 8, VCC

Truth Table (Positive Logic)

Input	Output
H	L
L	H
H	H
L	H
H	L
L	H

Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$)

	Parameter	Symbol	Rating	Unit
Input	Forward current	I_F	50	mA
	Reverse voltage	V_R	5	V
	Power dissipation	P_D	45	mW
Output	Power dissipation	P_C	85	mW
	Output current	I_O	20	mA
	Output voltage	V_O	$V_{CC}+0.5$	V
	Supply voltage	V_{CC}	5.5	V
	Output Power Dissipation	P_O	85	mW
	Isolation voltage ^{*2}	V_{ISO}	3750	V rms
	Operating temperature	T_{OPR}	-40 ~ +110	$^{\circ}\text{C}$
	Storage temperature	T_{STG}	-55 ~ +125	$^{\circ}\text{C}$
	Soldering temperature ^{*3}	T_{SOL}	260	$^{\circ}\text{C}$

Notes:

*1 The V_{CC} supply must be bypassed by a 0.1 μF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and GND pins

*2 AC for 1 minute, R.H.= 40 ~ 60% R.H. In this test, pins 1, 2, 3 & 4 are shorted together, and pins 5, 6, 7 & 8 are shorted together.

*3 For 10 seconds

Electrical Characteristics (T_A=-40 to 110°C unless specified otherwise)

Input

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Forward voltage	V _F	-	1.4	1.8	V	I _F = 14mA
Reverse voltage	V _R	5.0	-	-	V	I _R = 10μA
Temperature coefficient of forward voltage	ΔV _F /ΔT _A	-	-1.8	-	mV/°C	I _F =10mA
Input capacitance	C _{IN}	-	60	-	pF	V _F =0, f=1MHz

Output

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
High level supply current	I _{CCH}	-	1	6	mA	I _F =0mA
Low level supply current	I _{CCL}	-	1	6	mA	I _F =14mA
High level output voltage	V _{OH}	V _{CC} -1	V _{CC} -0.3	-	V	V _{CC} =3.3V, I _F =0mA, I _O =-4mA
		V _{CC} -1	V _{CC} -0.2	-	V	V _{CC} =5V, I _F =0mA, I _O =-4mA
Low level output voltage	V _{OL}	-	0.21	0.8	V	V _{CC} = 3.3V, I _F =14mA, I _O =4mA
			0.17	0.8	V	V _{CC} = 5.0V, I _F =14mA, I _O =4mA
Input threshold current	I _{FT}	-	2	5	mA	I _{OL} =20uA

Switching Characteristics ($T_A = -40$ to 110°C , $V_{CC} = 3.3\text{V}$, $I_F = 14\text{mA}$ unless specified otherwise)

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
Propagation delay time to output high level (Fig.8)	t_{PHL}	-	29	40	ns	$I_F = 14\text{mA}$, $C_L = 15\text{pF}$, $V_{CC} = 3.3\text{V}$ CMOS Signal Levels
		-	27	50	ns	$I_F = 14\text{mA}$, $C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$ CMOS Signal Levels
Propagation delay time to output low level (Fig.8)	t_{PLH}	-	40	50	ns	$I_F = 14\text{mA}$, $C_L = 15\text{pF}$, $V_{CC} = 3.3\text{V}$ CMOS Signal Levels
		-	35	50	ns	$I_F = 14\text{mA}$, $C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$ CMOS Signal Levels
Pulse width distortion	$ t_{PHL} - t_{PLH} $	0	11	25	ns	$I_F = 14\text{mA}$, $C_L = 15\text{pF}$, $V_{CC} = 3.3\text{V}$ CMOS Signal Levels
		0	8	30	ns	$I_F = 14\text{mA}$, $C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$ CMOS Signal Levels
Output rise time (Fig.8)	t_r	-	9	-	ns	$I_F = 14\text{mA}$, $C_L = 15\text{pF}$, $V_{CC} = 3.3\text{V}$ CMOS Signal Levels
Output fall time (Fig.8)	t_f	-	11	-	ns	$I_F = 14\text{mA}$, $C_L = 15\text{pF}$, $V_{CC} = 3.3\text{V}$ CMOS Signal Levels
Common mode transient Immunity at logic high* ⁴ (Fig.9)	$ CM_H $	10,000	-	-	V/ μS	$I_F = 0\text{mA}$, $T_A = 25^\circ\text{C}$ $V_{CM} = 1000\text{Vp-p}$ (Fig.14)
Common mode transient immunity at logic low* ⁵ (Fig.9)	$ CM_L $	10,000	-	-	V/ μS	$I_F = 14\text{mA}$, $T_A = 25^\circ\text{C}$ $V_{CM} = 1000\text{Vp-p}$ (Fig.)

Typical Electro-Optical Characteristics Curves

Figure 1. Forward Current vs. Forward Voltage

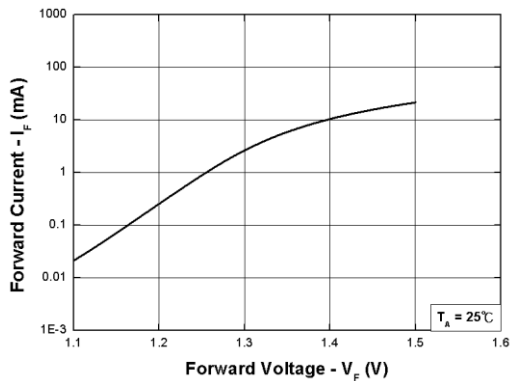


Figure 2. Input Threshold Current vs. Ambient Temperature

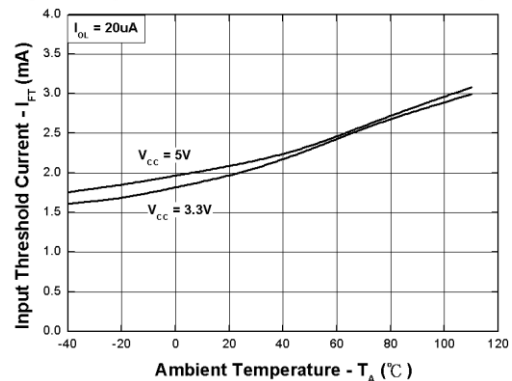


Figure 3. High Level Supply Current vs. Ambient Temperature

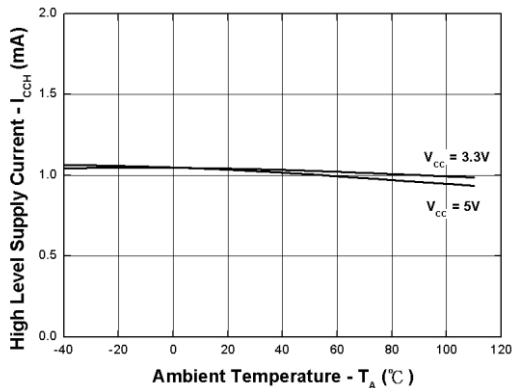


Figure 4. Low Level Supply Current vs. Ambient Temperature

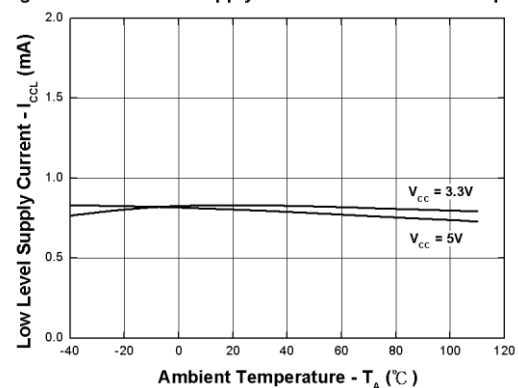


Figure 5. Switching Time vs. Forward Current

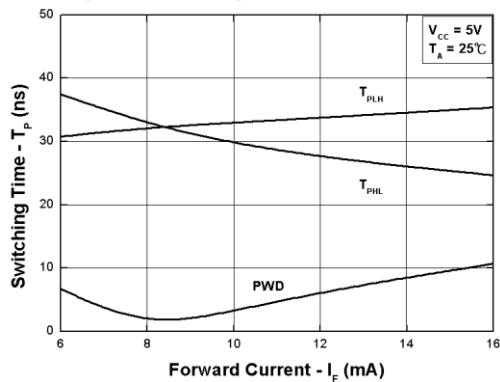


Figure 6. Switching Time vs. Forward Current

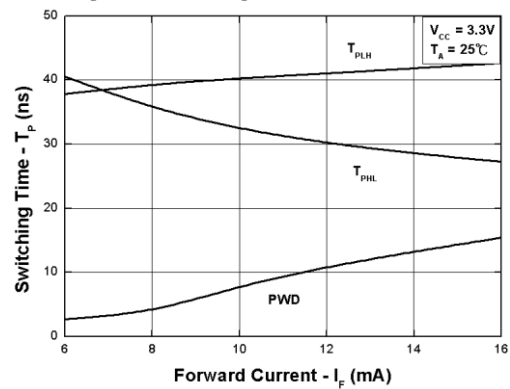


Figure 7. Forward voltage vs. Ambient Temperature

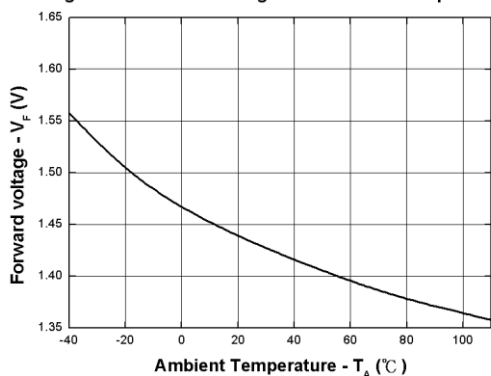


Fig. 8 Test circuit and waveforms for t_{PHL} , t_{PLH} , t_r , and t_f

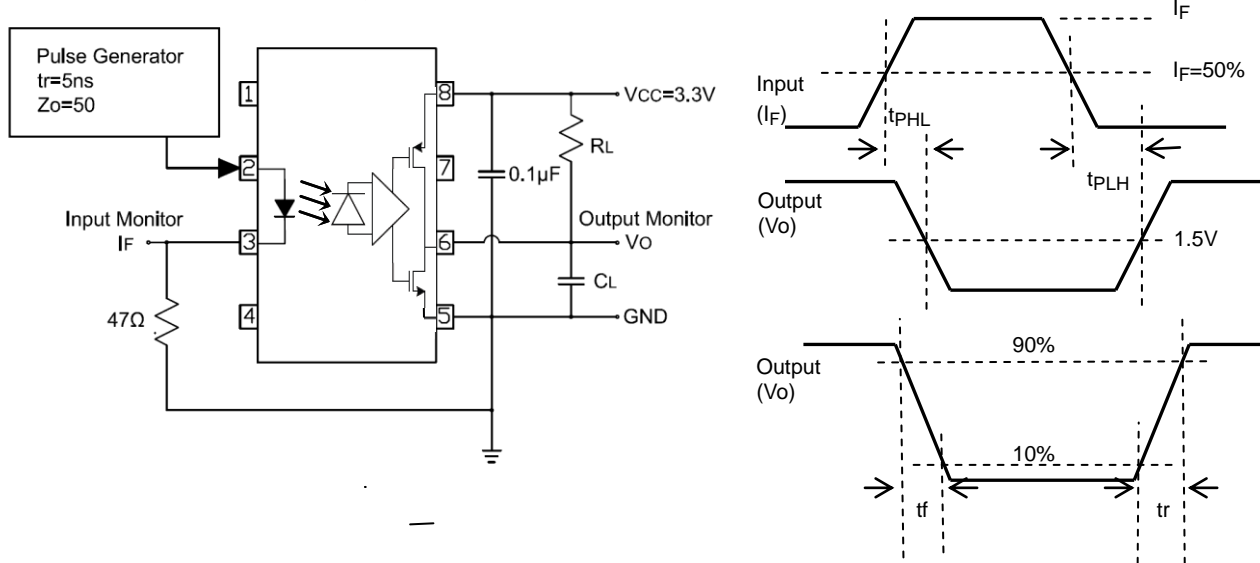
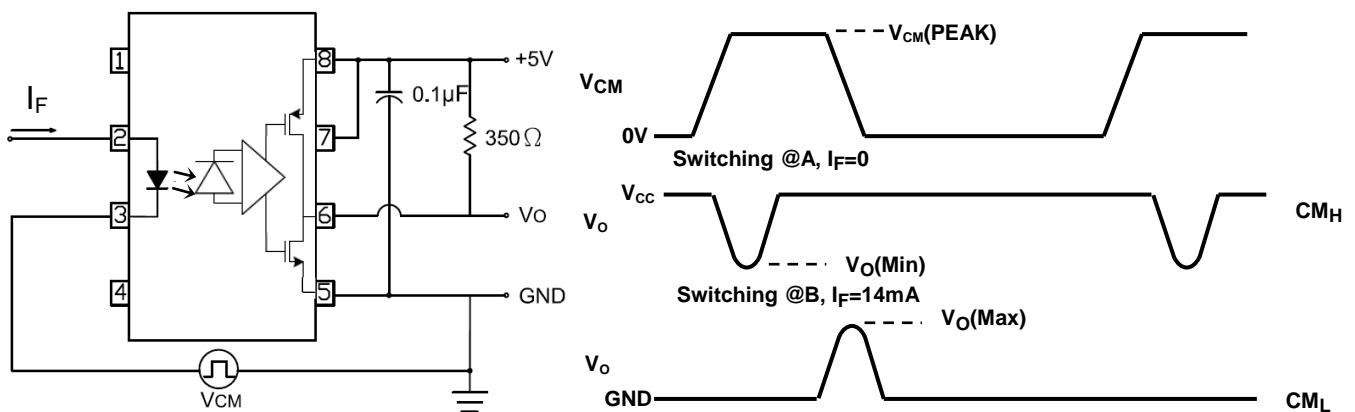


Fig. 9 Test circuit Common mode Transient Immunity



Note

*4. CM_H — The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the HIGH state (i.e., $V_{OUT} > 2.0\text{V}$).

*5. CM_L — The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the LOW output state (i.e., $V_{OUT} < 0.8\text{V}$).

Order Information

Part Number

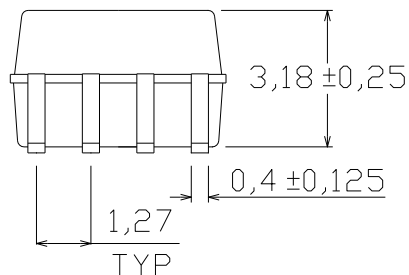
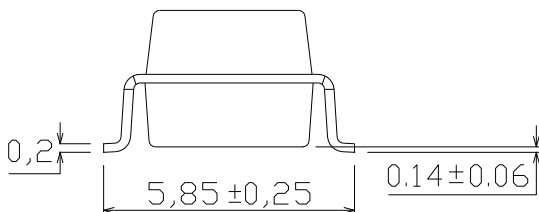
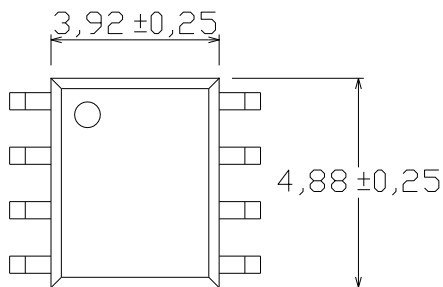
EL071L(Z)-V

Note

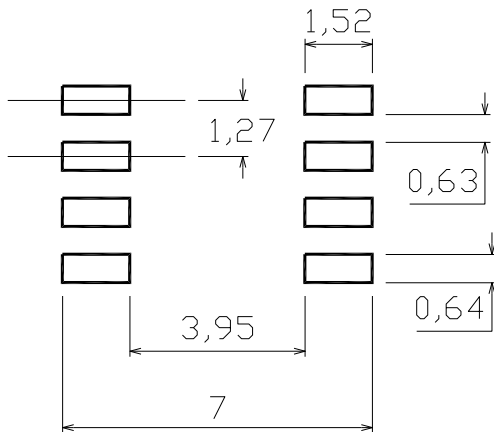
Z = Tape and reel option (TA, TB or none).
V = VDE (optional)

Option	Description	Packing quantity
None	Standard	100 units per tube
-V	Standard + VDE	100 units per tube
(TA)	TA tape & reel option	2000 units per reel
(TB)	TB tape & reel option	2000 units per reel
(TA)-V	TA tape & reel option + VDE	2000 units per reel
(TB)-V	TB tape & reel option + VDE	2000 units per reel

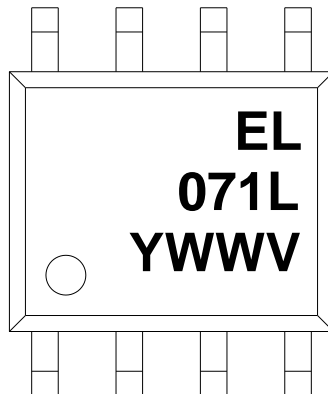
Package Dimension (Dimensions in mm)



Recommended pad layout for surface mount leadform



Device Marking

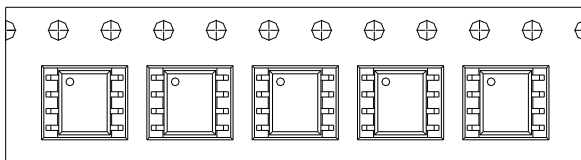


Notes

EL	denotes EVERLIGHT
060L	denotes Device Number
Y	denotes 1 digit Year code
WW	denotes 2 digit Week code
V	denotes VDE (optional)

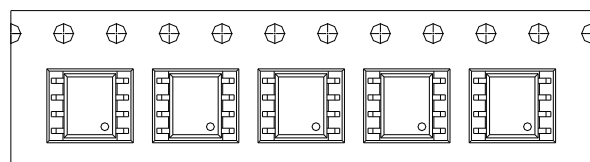
Tape & Reel Packing Specifications

Option TA



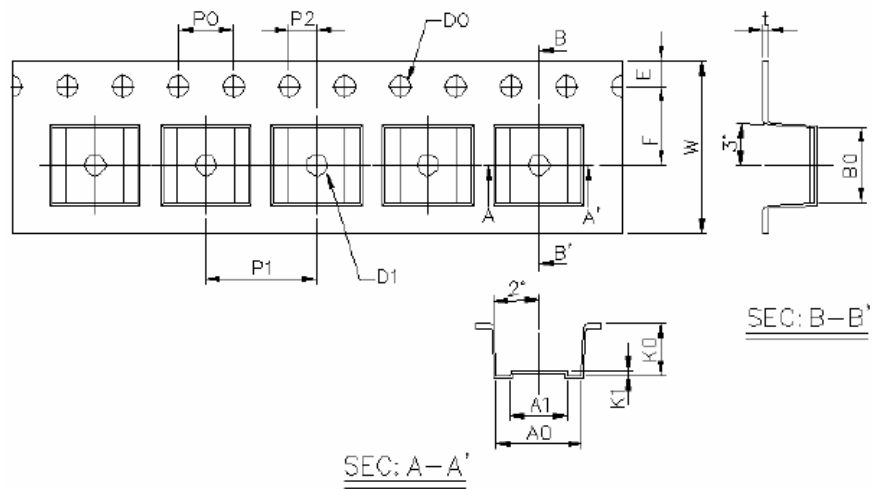
Direction of feed from reel

Option TB



Direction of feed from reel

Tape dimension

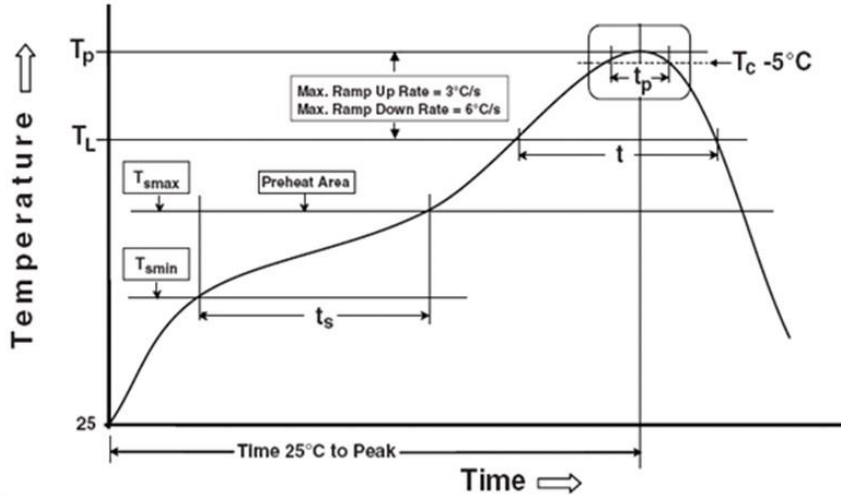


Dimension No.	A0	A1	B0	D0	D1	E	F
Dimension(mm)	6.2±0.1	4.1±0.1	5.28±0.1	1.5±0.1	1.5±0.3	1.75±0.1	5.5±0.1
Dimension No.	Po	P1	P2	t	W	K0	K1
Dimension(mm)	4.0±0.1	8.0±0.1	2.0±0.1	0.4±0.1	12.0+0.3/ -0.1	3.7±0.1	0.3±0.1

Precautions for Use

1. Soldering Condition

1.1 (A) Maximum Body Case Temperature Profile for evaluation of Reflow Profile



Note:

Reference: IPC/JEDEC J-STD-020D

Preheat

Temperature min (T_{smin})	150 °C
Temperature max (T_{smax})	200°C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max

Other

Liquidus Temperature (T_L)	217 °C
Time above Liquidus Temperature (t_L)	60-100 sec
Peak Temperature (T_p)	260°C
Time within 5 °C of Actual Peak Temperature: $T_p - 5^\circ\text{C}$	30 s
Ramp- Down Rate from Peak Temperature	6°C /second max.
Time 25°C to peak temperature	8 minutes max.
Reflow times	3 times

Disclaimer

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2. When using this product, please observe the absolute maximum ratings and the instructions for using outlined in these specification sheets. EVERLIGHT assumes no responsibility for any damage resulting from use of the product which does not comply with the absolute maximum ratings and the instructions included in these specification sheets.
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