

## **BMD-345**

# Stand-alone Bluetooth 5 low energy and IEEE 802.15.4 module with PA / LNA

Data sheet



#### **Abstract**

This technical data sheet describes the BMD-345 stand-alone Bluetooth® low energy and IEEE 802.15.4 module with a power amplifier and low noise amplifier. The OEMs can embed their own application on top of the integrated Bluetooth low energy stack using Nordic Semiconductor SDK integrated development environment (IDE).





## **Document information**

Title	BMD-345	
Subtitle	Stand-alone Bluetooth 5 low ener	gy and IEEE 802.15.4 module with PA /
Document type	Data sheet	
Document number	UBX-19039908	
Revision and date	R08	12-Oct-2020
Disclosure restriction	C1-Public	

Product status	Corresponding content status				
Functional sample	Draft For functional testing. Revised and supplementary data will be published later.				
In development / Prototype	Objective specification	Target values. Revised and supplementary data will be published later.			
Engineering sample	Advance information	Data based on early testing. Revised and supplementary data will be published later.			
Initial production	Early production information	Data from product verification. Revised and supplementary data may be published later.			
Mass production / End of life	Production information	Document contains the final product specification.			

#### This document applies to the following products:

Product name	Type number	Firmware version	PCN reference	Product status
BMD-345	BMD-345-A-R-10	N/A	N/A	Initial production

u-blox or third parties may hold intellectual property rights in the products, names, logos and designs included in this document. Copying, reproduction, modification or disclosure to third parties of this document or any part thereof is only permitted with the express written permission of u-blox.

The information contained herein is provided "as is" and u-blox assumes no liability for its use. No warranty, either express or implied, is given, including but not limited to, with respect to the accuracy, correctness, reliability and fitness for a particular purpose of the information. This document may be revised by u-blox at any time without notice. For the most recent documents, visit www.u-blox.com.

Copyright © u-blox AG.



## Contents

Document information	2
Contents	3
1 Functional description	5
1.1 Features	5
1.2 Applications	6
1.3 Block diagram	6
1.4 Product specifications	7
2 Pin definition	9
2.1 Pin assignment	g
2.2 Peripheral pins	11
2.2.1 BMD-301 to BMD-345 pad differences	12
3 Electrical specifications	13
3.1 Absolute maximum ratings	13
3.2 Operating conditions	13
3.3 Power configuration	13
3.3.1 USB power	14
3.4 General purpose I/O	14
3.5 Module reset	14
3.6 Debug and programming	14
3.7 Clocks	15
3.7.1 32.768 kHz crystal (LFXO)	15
3.7.2 32.768 kHz clock source comparison	15
4 Firmware	16
4.1 Factory image	16
4.2 SoftDevices	16
4.2.1 S140	16
4.2.2 S340	16
4.2.3 IEEE 802.15.4 (Thread and Zigbee)	16
4.3 Bluetooth device address	17
5 RF front end – PA / LNA	18
5.1 Hardware	18
5.1.1 PA / LNA modes	18
5.1.2 PA/LNA control	18
5.1.3 Power limitations	18
5.2 Software enablement	19
5.2.1 Dynamic method	19
5.2.2 Static method	22
6 Mechanical specifications	23
6.1 Dimensions	23
6.2 Recommended PCB land pads	23



	6.3	Mod	dule marking	24
7	R	F De	sign notes	25
	7.1	Rec	ommended RF layout and ground plane	25
	7.2	Med	chanical enclosure	25
	7.3	App	roved external antennas	25
	7.	.3.1	Canada (ISED) Antenna Statement	25
	7.	.3.2	Antenna list	25
8	В	MD-	345 evaluation development kit	26
9	Q	ualif	ication and approvals	27
	9.1	Unit	red States (FCC)	.27
	9.	.1.1	Labeling and user information requirements	27
	9.	.1.2	RF exposure	27
	9.2	Can	ada (ISED)	28
	9.	.2.1	Labeling and user information requirements	28
	9.	.2.2	RF exposure / Déclaration d'exposition aux radiofréquences	28
	9.1	Eur	opean Union regulatory compliance	29
	9.	.1.1	Radio Equipment Directive (RED) 2014/53/EU	29
	9.2	Aus	tralia / New Zealand (RCM)	29
	9.3	Blue	etooth qualification	29
1(	0 E	nviro	onmental	30
	10.	1 RoF	IS	.30
	10.2	2REA	NCH	.30
	10.3	3 Cali	fornia proposition 65 (P65)	30
1	1 P	rodu	ct handling	31
	11.	1 Pac	kaging	31
	1	1.1.1	Reel packaging	31
	1	1.1.2	Carrier tape dimensions	31
	11.2	2 Moi	sture sensitivity level	32
	11.3	3 Refl	ow soldering	32
	11.4	4ESE	precautions	32
12	2 0	rder	ing information	33
	12.	1 Ord	ering information	33
1;	3 S	uppo	ort and other high-risk use warning	34
			ocuments	
			nistory	
			,	36



## 1 Functional description

The BMD-345 is an advanced, highly flexible, low power multiprotocol System on Module (SoM) that enables Bluetooth 5 low energy low energy and IEEE 802.15.4 (Thread and Zigbee) connectivity for portable, low power embedded systems. With an Arm® Cortex®-M4 with FPU processor, integrated 2.4 GHz transceiver, RF power and low noise amplifiers (PA / LNA), and U.FL connector, the BMD-345 provides a full RF solution allowing faster time to market with reduced development costs. Providing full use of the Nordic Semiconductor nRF52840's capabilities and peripherals, the BMD-345 can power the most demanding applications, all while simplifying designs and reducing BOM costs. The BMD-345 is an ideal solution for designs that require maximum range and Bluetooth 5 features or 802.15.4 based networking for Thread and Zigbee. Increased integration with built in USB and DC/DC supply reduces design complexity and BOM cost, while expanding possible applications. BMD-345 designs are footprint compatible with the BMD-301, providing low-cost flexibility for tiered product lineups.

#### 1.1 Features

- Based on the Nordic Semiconductor nRF52840 SoC
- Bluetooth 5 PHYs: LE 1M, LE 2M, and LE Coded (long range)
- Bluetooth 5 features: Advertising Extensions, Channel Selection Algorithm #2
- Bluetooth mesh
- IEEE 802.15.4 with Thread and Zigbee support
- Extended range with PA + LNA
- Complete RF solution with U.FL connector for an external antenna
- Arm® Cortex®-M4 with FPU 32-bit processor
- Arm® TrustZone® Cryptocell 310 security
- 128-bit AES HW encryption
- True Random Number Generator
- Serial Wire Debug (SWD)
- Nordic Semiconductor SoftDevice ready
- 1 MB embedded flash memory
- 256 kB RAM
- 44 General Purpose I/O Pins
- -40 °C to +85 °C temperature range12-bit/200 KSPS ADC
- 12-bit/200 KSPS ADC
- One Full-Speed USB (12 Mbps)
- Four SPI master / three slave (8 Mbps)
- Quad SPI with Execute in Place (XIP)
- PWM 4 blocks x 4-channels each
- General Purpose and Low power comparators
- Temperature sensor
- Two 2-wire Master/Slave (I2C compatible)
- I2S audio interface
- Two UARTs (w/ CTS/RTS and DMA)
- 20-channel CPU independent Programmable Peripheral Interconnect (PPI)
- Quadrature Demodulator (QDEC)
- 5 x 32 bit timer/counters
- 3 x 24 bit Real Timer Counters (RTC)
- NFC-A tag interface for OOB pairing
- Dimensions: 15.0 x 10.2 x 2.0 mm



## 1.2 Applications

- Climate control
- Lighting products
- Safety and security
- Home appliances
- Access control
- Internet of Things
- Home Health Care
- Advanced Remote Controls
- Smart Energy Management
- Low-Power Sensor Networks
- Interactive Entertainment Devices
- Environmental Monitoring
- Hotel Automation
- Office Automation

## 1.3 Block diagram

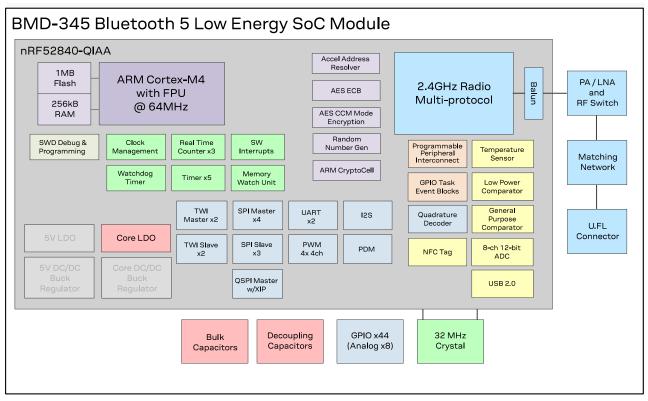


Figure 1: Block diagram of BMD-345



## 1.4 Product specifications

Detail	Description
Bluetooth	
Bluetooth version	Bluetooth 5 Low Energy, Concurrent Central & Peripheral (S140), LE Codec PHY (Long Range), LE 2M PHY, LE 1M PHY, Advertising Extensions, CSA #2, Bluetooth mesh
Security	AES-128, Arm® Cryptocell accelerated
LE connections	Concurrent central, observer, peripheral, and broadcaster roles with up to twenty concurrent connections along with one Observer and one Broadcaster (S140)
IEEE 802.15.4	
Thread stack	OpenThread, Thread 1.1
Thread security	AES-128, Arm® Cryptocell accelerated
Zigbee stack	Zigbee Compliant Platform
Radio	
Frequency	2.360 GHz to 2.500 GHz
Modulations	GFSK at 1 Mbps and 2 Mbps, QPSK at 250 Kbps
Transmit power (EIRP)	+18 dBm maximum (see section 5.1.3 for regional limits)
Receiver sensitivity	-98 dBm (2Mbps), -102 dBm (1Mbps), -107 dBm (125 kbps BLE), -105 dBm (IEEE 802.15.4)
Antenna	External through U.FL connector
Current consumption	
TX only @ +18 dBm, PA enabled	51 mA
RX only @ 1 Mbps, LNA enabled	20 mA
CPU @ 64 MHz from flash, from RAM, PA / LNA shutdown mode	6.3 mA, running from flash 5.2 mA, running from RAM
System off, on, no RAM retention, PA/LNA shutdown mode	0.7 $\mu$ A, system off 1.27 $\mu$ A, system on
Dimensions	
BMD-345	Length: 15.0 mm ± 0.3 mm
	Width: 10.2 mm ± 0.3 mm
	Height: 2.0 mm ± 0.1 mm
Hardware	
Interfaces	SPI Master/Slave x 4 Quad SPI x 1 UART x 2
	I2C Master/Slave x 2 GPIO x 44 I2S x1
	PWM x 16 (4 blocks x 4-channels each) PDM x 1 USB 2.0 x 1
Power supply	Analog input x 8  VDD: 2.0 V to 3.6 V  VBUS: 4.35 V to 5.5 V (For USB operation)
Temperature range	-40 °C to +85 °C
Certifications	
USA (FCC)	FCC part 15.247 modular certification FCC ID: XPYBMD345
Canada (ISED)	Innovation, Science and Economic Development Canada RSS-247 modular certification IC: 8595A-BMD345



Detail	Description
Europe (CE)	EN 62369-1:2014 + A11:2017
	EN 301 489-1 V2.2.3 & EN 301 489-17 V3.2.2
	EN 300 328 V2.2.2
Australia / New Zealand (RCM)	AS/NZS 4268:2017
Bluetooth	BMD-345 RF-PHY Component (Tested) – DID: D040774; QDID: 114712
Radio chip	
Nordic Semiconductor nRF52840	Additional details: nRF52840 Product Specification
	Software Development Kit

Table 1: Product specifications



## 2 Pin definition

## 2.1 Pin assignment

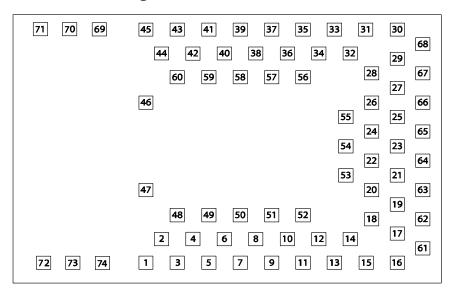


Figure 2: BMD-345 Pin assignment (Top view)

No.	Name	1/0	Description	nRF52 pin	Remarks
1	GND	Power	Electrical Ground		
2	GND	Power	Electrical Ground		
3	GND	Power	Electrical Ground		
4	GND	Power	Electrical Ground		
5	GND	Power	Electrical Ground		
6	P0.25	I/O	GPIO	P0.25	
7	P0.26	I/O	GPIO	P0.26	
8	P0.27	I/O	GPIO	P0.27	
9	P0.28	I/O	GPIO/AIN4	P0.28	Standard drive, low frequency I/O only (<10 kHz)
10	P0.29	I/O	GPIO/AIN5	P0.29	Standard drive, low frequency I/O only (<10 kHz)
11	P0.30	I/O	GPIO/AIN6	P0.30	Standard drive, low frequency I/O only (<10 kHz)
12	P0.31	I/O	GPIO/AIN7	P0.31	Standard drive, low frequency I/O only (<10 kHz)
13	P0.00	I/O	GPIO/XTAL1 (32.768 kHz)	P0.00	
14	P0.01	I/O	GPIO/XTAL2 (32.768 kHz)	P0.01	
15	P0.02	I/O	GPIO/AIN0	P0.02	Standard drive, low frequency I/O only (<10 kHz)
16	GND	Power	Electrical Ground		
17	VCC	Power I/O	Connect to 2.0V to 3.6V DC supply	VDD and VDDH	An internal 4.7 µF bulk capacitor is included on the module. However, it is good design practice to add additional bulk capacitance as required for your application, i.e. those with heavy GPIO usage and/or current draw.
18	GND	Power	Electrical Ground		
19	P0.03	I/O	GPIO/AIN1	P0.03	Standard drive, low frequency I/O only (<10 kHz)
20	P0.04	I/O	GPIO/AIN2	P0.04	
21	P0.05	I/O	GPIO/AIN3	P0.05	
22	P0.06	I/O	GPIO	P0.06	
23	P0.07	I/O	GPIO/TRACECLK	P0.07	



26         P0.10         I/O         GPIO/NFC2         P0.10         Standard drive, low from from from from from from from from	equency I/O only (<10 kHz) equency I/O only (<10 kHz)
26         P0.10         I/O         GPIO/NFC2         P0.10         Standard drive, low from the policy of the poli	
27         P0.11         I/O         GPIO/TRACEDATA[2]         P0.11           28         P0.12         I/O         GPIO/TRACEDATA[1]         P0.12           29         GND         Power         Electrical Ground           30         GND         Power         Electrical Ground           31         P0.13         I/O         GPIO         P0.13           32         P0.14         I/O         GPIO         P0.14           33         P0.15         I/O         GPIO         P0.15           34         P0.16         I/O         GPIO         P0.16           35         P0.17         I/O         GPIO         P0.17           36         P0.21         I/O         GPIO         P0.21           37         P0.19         I/O         GPIO         P0.19           38         P0.20         I/O         GPIO         P0.20           39         P0.18         I/O         GPIO/RESET         P0.18           40         P0.22         I/O         GPIO         P0.22           41         P0.23         I/O         GPIO         P0.23           42         P0.24         I/O         GPIO         SWDLK	equency I/O only (<10 kHz)
28 P0.12    I/O	
Power   Electrical Ground   Power   Electrical Ground	
30 GND	
31 P0.13 I/O GPIO P0.13 32 P0.14 I/O GPIO P0.14 33 P0.15 I/O GPIO P0.15 34 P0.16 I/O GPIO P0.16 35 P0.17 I/O GPIO P0.17 36 P0.21 I/O GPIO P0.19 38 P0.20 I/O GPIO P0.19 38 P0.20 I/O GPIO P0.20 39 P0.18 I/O GPIO P0.20 39 P0.18 I/O GPIO P0.22 41 P0.23 I/O GPIO P0.23 42 P0.24 I/O GPIO P0.24 43 SWCLK I SWD Clock SWCLK 44 SWDIO I/O SWD IO SWDIO 45 GND Power Electrical Ground 46 GND Power Electrical Ground 47 GND Power Electrical Ground 48 TX_EN O PA TX Enable P1.06 Internally connected to p1.07 I/O GPIO P1.07 Standard drive, low from for p1.08 I/O fine from from from from from from from from	
32 P0.14    I/O	
33   P0.15   I/O   GPIO   P0.15     34   P0.16   I/O   GPIO   P0.16     35   P0.17   I/O   GPIO   P0.17     36   P0.21   I/O   GPIO   P0.21     37   P0.19   I/O   GPIO   P0.19     38   P0.20   I/O   GPIO   P0.20     39   P0.18   I/O   GPIO   P0.20     39   P0.18   I/O   GPIO   P0.22     41   P0.22   I/O   GPIO   P0.22     41   P0.23   I/O   GPIO   P0.23     42   P0.24   I/O   GPIO   P0.24     43   SWCLK   I   SWD Clock   SWCLK     44   SWDIO   I/O   SWD IO   SWDIO     45   GND   Power   Electrical Ground     46   GND   Power   Electrical Ground     47   GND   Power   Electrical Ground     48   TX_EN   O   PA TX Enable   P1.05   Internally connected to the standard drive, low from the standard drive is the standard dr	
34   P0.16   I/O   GPIO   P0.16   35   P0.17   I/O   GPIO   P0.17   36   P0.21   I/O   GPIO   P0.21   37   P0.19   I/O   GPIO   P0.20   38   P0.20   I/O   GPIO   P0.20   39   P0.18   I/O   GPIO/RESET   P0.18   40   P0.22   I/O   GPIO   P0.22   41   P0.23   I/O   GPIO   P0.23   42   P0.24   I/O   GPIO   P0.24   43   SWCLK   I   SWD Clock   SWCLK   SWDIO	
35         P0.17         I/O         GPIO         P0.17           36         P0.21         I/O         GPIO         P0.21           37         P0.19         I/O         GPIO         P0.19           38         P0.20         I/O         GPIO         P0.20           39         P0.18         I/O         GPIO         P0.21           40         P0.22         I/O         GPIO         P0.22           41         P0.23         I/O         GPIO         P0.23           42         P0.24         I/O         GPIO         P0.24           43         SWCLK         I         SWD Clock         SWCLK           44         SWDIO         I/O         SWDIO         SWDIO           45         GND         Power         Electrical Ground           46         GND         Power         Electrical Ground           47         GND         Power         Electrical Ground           48         TX_EN         O         PA TX Enable         P1.05         Internally connected to the proper content of the	
36         P0.21         I/O         GPIO         P0.21           37         P0.19         I/O         GPIO         P0.19           38         P0.20         I/O         GPIO         P0.20           39         P0.18         I/O         GPIO/RESET         P0.18           40         P0.22         I/O         GPIO         P0.22           41         P0.23         I/O         GPIO         P0.23           42         P0.24         I/O         GPIO         P0.24           43         SWCLK         I         SWD Clock         SWCLK           44         SWDIO         I/O         SWDIO           45         GND         Power         Electrical Ground           46         GND         Power         Electrical Ground           47         GND         Power         Electrical Ground           48         TX_EN         O         PA TX Enable         P1.05         Internally connected to the property of the pro	
37         P0.19         I/O         GPIO         P0.19           38         P0.20         I/O         GPIO         P0.20           39         P0.18         I/O         GPIO/RESET         P0.18           40         P0.22         I/O         GPIO         P0.22           41         P0.23         I/O         GPIO         P0.23           42         P0.24         I/O         GPIO         P0.24           43         SWCLK         I         SWD Clock         SWCLK           44         SWDIO         I/O         SWDIO           45         GND         Power         Electrical Ground           46         GND         Power         Electrical Ground           47         GND         Power         Electrical Ground           48         TX_EN         O         PA TX Enable         P1.05         Internally connected to Internally connected to Internally connected to P1.06           50         P1.07         I/O         GPIO         P1.07         Standard drive, low from the property of the pro	
38         P0.20         I/O         GPIO         P0.20           39         P0.18         I/O         GPIO/RESET         P0.18           40         P0.22         I/O         GPIO         P0.22           41         P0.23         I/O         GPIO         P0.23           42         P0.24         I/O         GPIO         P0.24           43         SWCLK         I         SWD Clock         SWCLK           44         SWDIO         I/O         SWDIO           45         GND         Power         Electrical Ground           46         GND         Power         Electrical Ground           47         GND         Power         Electrical Ground           48         TX_EN         O         PA TX Enable         P1.05         Internally connected to Internally connected to Internally connected to P1.06           50         P1.07         I/O         GPIO         P1.07         Standard drive, low from Standard drive, low fro	
39         P0.18         I/O         GPIO/RESET         P0.18           40         P0.22         I/O         GPIO         P0.22           41         P0.23         I/O         GPIO         P0.23           42         P0.24         I/O         GPIO         P0.24           43         SWCLK         I         SWD Clock         SWCLK           44         SWDIO         I/O         SWDIO           45         GND         Power         Electrical Ground           46         GND         Power         Electrical Ground           47         GND         Power         Electrical Ground           48         TX_EN         O         PA TX Enable         P1.05         Internally connected to Internally connected to P1.06           49         RX_EN         O         PA RX Enable         P1.06         Internally connected to P1.07           50         P1.07         I/O         GPIO         P1.07         Standard drive, low from P1.08	
40 P0.22 I/O GPIO P0.22  41 P0.23 I/O GPIO P0.23  42 P0.24 I/O GPIO P0.24  43 SWCLK I SWD Clock SWCLK  44 SWDIO I/O SWD IO SWDIO  45 GND Power Electrical Ground  46 GND Power Electrical Ground  47 GND Power Electrical Ground  48 TX_EN O PA TX Enable P1.05 Internally connected to the sum of the su	
41 P0.23 I/O GPIO P0.23  42 P0.24 I/O GPIO P0.24  43 SWCLK I SWD Clock SWCLK  44 SWDIO I/O SWD IO SWDIO  45 GND Power Electrical Ground  46 GND Power Electrical Ground  47 GND Power Electrical Ground  48 TX_EN O PA TX Enable P1.05 Internally connected to the second se	
42         P0.24         I/O         GPIO         P0.24           43         SWCLK         I         SWD Clock         SWCLK           44         SWDIO         I/O         SWDIO           45         GND         Power         Electrical Ground           46         GND         Power         Electrical Ground           47         GND         Power         Electrical Ground           48         TX_EN         O         PA TX Enable         P1.05         Internally connected to the property of the property	
43 SWCLK I SWD Clock SWCLK  44 SWDIO I/O SWD IO SWDIO  45 GND Power Electrical Ground  46 GND Power Electrical Ground  47 GND Power Electrical Ground  48 TX_EN O PA TX Enable P1.05 Internally connected to the second second price of the second second second price of the second price of	
43 SWCLK I SWD Clock SWCLK  44 SWDIO I/O SWD IO SWDIO  45 GND Power Electrical Ground  46 GND Power Electrical Ground  47 GND Power Electrical Ground  48 TX_EN O PA TX Enable P1.05 Internally connected to the second second price of the second second second price of the second price of	
45 GND Power Electrical Ground 46 GND Power Electrical Ground 47 GND Power Electrical Ground 48 TX_EN O PA TX Enable P1.05 Internally connected t 49 RX_EN O PA RX Enable P1.06 Internally connected t 50 P1.07 I/O GPIO P1.07 Standard drive, low fro 51 P1.08 I/O GPIO P1.08	
46 GND Power Electrical Ground 47 GND Power Electrical Ground 48 TX_EN O PA TX Enable P1.05 Internally connected to the second second price of the second second price of the second price	
47         GND         Power         Electrical Ground           48         TX_EN         O         PA TX Enable         P1.05         Internally connected to the connected t	
48         TX_EN         O         PA TX Enable         P1.05         Internally connected to the price of	
49         RX_EN         O         PA RX Enable         P1.06         Internally connected to the connected	
50 P1.07 I/O GPIO P1.07 Standard drive, low from 51 P1.08 I/O GPIO P1.08	o PA / LNA TX_EN pin
51 P1.08 I/O GPIO P1.08	o PA / LNA RX_EN pin
	equency I/O only (<10 kHz)
52 D1 00 I/O CDIO/TDACEDATA[2] D1 00	
52 P1.09 I/O GPIO/TRACEDATA[3] P1.09	
53 P1.10 I/O GPIO P1.10 Standard drive, low fro	equency I/O only (<10 kHz)
54 P1.11 I/O GPIO P1.11 Standard drive, low fro	equency I/O only (<10 kHz)
55 GND Power Electrical Ground	
56 P1.00 I/O GPIO/TRACEDATA[0]/SWO P1.00	
57 P1.01 I/O GPIO P1.01 Standard drive, low fro	equency I/O only (<10 kHz)
58 PA_SW O PA Switch P1.02 Internally connected t	o PA / LNA RF Switch pin
59 P1.03 I/O GPIO P1.03 Standard drive, low fro	equency I/O only (<10 kHz)
60 PA_MODE O GPIO P1.04 Internally connected t	o PA / LNA Mode pin
61 P1.12 I/O GPIO P1.12 Standard drive, low fro	equency I/O only (<10 kHz)
62 P1.13 I/O GPIO P1.13 Standard drive, low fro	equency I/O only (<10 kHz)
63 P1.14 I/O GPIO P1.14 Standard drive, low fro	equency I/O only (<10 kHz)
64 P1.15 I/O GPIO P1.15 Standard drive, low fro	
65 VCC Power I/O Connect to 2.0 V to 3.6 V DC VDD/VDDH An internal 4.7 µF bull supply the module. However, to add additional bulk for your application, i. usage and/or current of the supplement of the supplementation of the suppl	equency I/O only (<10 kHz)



No.	Name	1/0	Description	nRF52 pin	Remarks
66	VBUS	Power	USB PHY supply: 4.35 V to 5.5 V in Connect to USB Host device 5 V supply	VBUS	
67	USB-D-	I/O	USB Data-	D-	
68	USB-D+	I/O	USB Data+	D+	
69	GND	Power	Electrical Ground		
70	GND	Power	Electrical Ground		
71	GND	Power	Electrical Ground		
72	GND	Power	Electrical Ground		
73	RESERVED	RESERVED	RESERVED		Reserved for future use. Leave floating.
74	GND	Power	Electrical Ground		

Table 2: BMD-345 pin-out

## 2.2 Peripheral pins

The BMD-345 features a pin multiplexing system that allows most internal peripherals, such as UART and SPI, to be used on any GPIO pin. This freedom in pin choice enables better optimization of designs and PCB layout.



Only one peripheral signal can be multiplexed to a GPIO pin at a time. Some functions are restricted to certain pins due to additional internal circuitry required by the interface. These include: Trace signals, analog inputs, XTAL signals, USB signals, SWD interface, and reset. See Table 3.

Peripheral	Signal	Pin options
UARTO, UART1, I2CO, I2C1, SPIO, SPI1, SPI2, SPI3, I2SO, QSPIO, PDMO, PWMO, PWM1, PWM2, PWM3	All	P0.00-P0.31, P1.01, P1.03, P1.07-P1.15
ADC, COMP, LPCOMP	All	P0.02-P0.05, P0.28-P0.31 (AIN0-AIN7)
NFC	NFC1 NFC2	P0.09 P0.10
Reset	RESET	P0.18
Trace	TRACECLK SWO/TRACEDATA[0] TRACEDATA[1] TRACEDATA[2] TRACEDATA[3]	P0.07 P1.00 P0.12 P0.11 P1.09
SWD	SWD Clock SWD IO	SWCLK SWDIO
32.768 kHz Crystal	XTAL1 XTAL2	P0.00 P0.01
USB	USB Data + USB Data -	USB-D+ USB-D-

Table 3: Peripheral pin options



Some peripherals on the BMD-345 share the same memory location for their registers. This means that only one of these peripherals can be used at a time. It is possible to switch between peripherals that share the same register location by clearing and reinitializing the associated configuration registers. See Nordic Semiconductor nRF52840 Product Specification for details.



Peripheral ID	Base address	Shared peripherals	
3	0x40003000	SPI0	12C0
4	0x40004000	SPI1	I2C1

Table 4: Peripherals with shared registers

### 2.2.1 BMD-301 to BMD-345 pad differences

Due to differences in the nRF52840 SoC used by the BMD-345, not all functions (such as SWO/TRACE signals) are found on the same pins as on the BMD-301 (nRF52832). Particularly of note is the reset pin function which on the BMD-345 is now available on P0.18 instead of P0.21 as on the BMD-301. To maintain pin for pin compatibility of the reset signal, P0.18 and P0.21 have swapped pad locations on the BMD-345 footprint. These differences are detailed in Table 5 below:

Pin	BMD-301 name	BMD-301 function	BMD-345 name	BMD-345 function
39	P0.21	GPIO/RESET	P0.18	GPIO/RESET
38	P0.20	GPIO/TRACECLK	P0.20	GPIO
36	P0.18	GPIO/TRACEDATA[0]/SWO	P0.21	GPIO
34	P0.16	GPIO/TRACEDATA[1]	P0.16	GPIO
33	P0.15	GPIO/TRACEDATA[2]	P0.15	GPIO
32	P0.14	GPIO/TRACEDATA[3]	P0.14	GPIO
23	P0.07	GPIO	P0.07	GPIO/TRACECLK
56	N/A	N/A	P1.00	GPIO/TRACEDATA[0]/SWO
28	P0.12	GPIO	P0.12	GPIO/TRACEDATA[1]
27	P0.11	GPIO	P0.11	GPIO/TRACEDATA[2]
52	N/A	N/A	P1.09	GPIO/TRACEDATA[3]

Table 5: BMD-301 to BMD-345 pad differences



## 3 Electrical specifications

Stressing the device above one or more of the ratings listed in the Absolute maximum rating section may cause permanent damage. These are stress ratings only. Operating the module at these or at any conditions other than those specified in the Operating conditions section of this document should be avoided. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating condition ranges define those limits within which the functionality of the device is guaranteed. Where application information is given, it is advisory only and does not form part of the specification.

## 3.1 Absolute maximum ratings

Symbol	Description	Min	Max	Unit
V <sub>CC_MAX</sub>	Voltage on VCC supply pin	-0.3	3.9	V
V <sub>BUS_MAX</sub>	Voltage on VBUS supply pin	-0.3	5.8	V
V <sub>IO_MAX</sub>	Voltage on GPIO pins (V <sub>CC</sub> > 3.6V)	-0.3	3.9	V
V <sub>IO_MAX</sub>	Voltage on GPIO pins (V <sub>CC</sub> ≤ 3.6V)	-0.3	V <sub>cc</sub> + 0.3 V	V
Ts	Storage Temperature Range	-40	125	°C

Table 6: Absolute maximum ratings

⚠

The product is not protected against overvoltage or reversed voltages. If necessary, voltage spikes exceeding the power supply voltage specification, given in table above, must be limited to values within the specified boundaries by using appropriate protection devices.

## 3.2 Operating conditions

Unless otherwise specified, all operating condition specifications are at an ambient temperature of 25 °C and a supply voltage of 3.3 V.

Operation beyond the specified operating conditions is not recommended and extended exposure beyond them may affect device reliability.

Symbol	Parameter	Min	Тур.	Max	Unit
V <sub>CC_IN</sub>	VCC operating supply voltage in	2.0	3.0	3.6	V
V <sub>BUS_IN</sub>	VBUS operating supply voltage in	4.35	5.0	5.5	V
T <sub>R_VCC</sub>	VCC Supply rise time (0 V to 1.7 V)	-	-	60	ms
T <sub>A</sub>	Operating Ambient Temperature Range	-40	25	85	°C

**Table 7: Operating conditions** 

\_

The BMD-345 is based on the nRF52840, revision 2 or newer IC.

## 3.3 Power configuration

The nRF52840 IC within the BMD-345 module has two internal regulator stages, REG0 and REG1, that each contain an LDO and DCDC regulator. Only the LDO regulator REG1 is utilized in the BMD-345. Pins 17 and 65 are connected within the module, which bypasses REG0. Both pins 17 and 65 should be connected on the host board. REG1 supplies power to the module core and can accept an input source voltage of 2.0 V to 3.6 V, placing the module in Normal mode. The voltage present on the VCC pins are always the GPIO high logic level voltage.



Mode	Pin	Name	Connection
Normal	17	VCC	2.0 V to 3.6 V DC
	65	VCC	

Table 8: Power mode pin connections

### 3.3.1 USB power

The USB interface on the BMD-345 can be used when the module is in Normal mode. The BMD-345 USB PHY is powered by a dedicated, internal LDO regulator that is fed by VBUS, pin 66.

⚠

Applying power to only the VBUS pin will not power the rest of the module. In order for the USB PHY to operate, VBUS must be externally powered.

## 3.4 General purpose I/O

The general purpose I/O is organized as two ports enabling access and control of the 44 available GPIO pins (4 GPIO are reserved for PA / LNA control). The first port allows access to P0.00 to P0.31, similar to the first port on the BMD-300/301. The second port, new to the BMD-345, allows access to P1.00 to P1.15. Each GPIO can be accessed individually with the following user configurable features:

- Input/output direction
- · Output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high- or low-level triggers on all pins
- Trigger interrupt on all pins
- All pins can be used by the PPI task/event system; the maximum number of pins that can be interfaced through the PPI at the same time is limited by the number of GPIOTE channels
- All pins can be individually configured to carry serial interface or quadrature demodulator signals
- Pins P1.02, P1.04, P1.05, and P1.06 are reserved for PA / LNA control.

Symbol	Parameter	Min.	Тур.	Max.	Unit
V <sub>IH</sub>	Input High Voltage	0.7 x VCC	-	VCC	V
V <sub>IL</sub>	Input Low Voltage	GND	-	0.3 x VCC	V
V <sub>OH</sub>	Output High Voltage	VCC - 0.4	-	VCC	V
V <sub>OL</sub>	Output Low Voltage	GND	-	GND + 0.4	V
R <sub>PU</sub>	Pull-up Resistance	11	13	16	kΩ
R <sub>PD</sub>	Pull-down Resistance	11	13	16	kΩ

Table 9: GPIO electrical specifications

#### 3.5 Module reset

GPIO pin P0.18 may be used for a hardware reset. In order to utilize P0.18 as a hardware reset, the UICR registers PSELRESET[0] and PSELRESET[1] must be set alike, to the value of 0x7FFFFD2. When P0.18 is programmed as RESET, the internal pull-up is automatically enabled. Nordic Semiconductor example applications and development kits program P0.18 as RESET\_N.

## 3.6 Debug and programming

The BMD-345 supports the two pin Serial Wire Debug (SWD) interface and offers flexible and powerful mechanism for non-intrusive debugging of program code. Breakpoints, single stepping, and instruction trace capture of code execution flow are part of this support.



The BMD-345 also supports ETM and ITM trace. The trace data from the ETM and the ITM is sent to an external debugger via a 4-bit wide parallel trace port. In addition to parallel trace, the TPIU supports serial trace via the Serial Wire Output (SWO) trace protocol.

### 3.7 Clocks

The BMD-345 requires two clocks, a high frequency clock and a low frequency clock. The high frequency clock is provided on-module by a high-accuracy 32 MHz crystal as required by the nRF52840 for radio operation.

The low frequency clock can be provided internally by an RC oscillator or synthesized from the fast clock, or externally by a 32.768 kHz crystal. An external crystal provides the lowest power consumption and greatest accuracy. Using the internal RC oscillator with calibration provides acceptable performance for Bluetooth low energy applications at a reduced cost and slight increase in power consumption.

### 3.7.1 32.768 kHz crystal (LFXO)

Symbol Parameter		Тур.	Max.	Unit	
F <sub>NOM_LFXO</sub>	Crystal frequency	32.768	-	kHz	
F <sub>TOL_LFXO_BLE</sub> Frequency tolerance, Bluetooth low energy applications <sup>1</sup>		-	±500	ppm	
f <sub>TOL_LFXO_ANT</sub>	Frequency Tolerance, ANT applications <sup>2</sup>	-	±50	ppm	
$C_{L\_LFXO}$	Load Capacitance	-	12.5	pF	
$C_{0\_LFXO}$	Shunt Capacitance	-	2	pF	
R <sub>S_LFXO</sub>	Equivalent series resistance	-	100	kΩ	
C <sub>pin</sub>	Input Capacitance on XL1 & XL2 pads	4	-	pF	

Table 10: 32.768 kHz crystal (LFXO)

### 3.7.2 32.768 kHz clock source comparison

Symbol	Parameter	Min.	Тур.	Max.	Unit
I <sub>LFXO</sub>	Current for 32.768 kHz Crystal Oscillator	-	0.23	-	μΑ
I <sub>LFRC</sub>	Current for 32.768 kHz RC Oscillator	-	0.7	1	μΑ
I <sub>LFSYNT</sub>	Current for 32.768 kHz Synthesized Oscillator	-	100	-	μΑ
f <sub>TOL_LFXO_BLE</sub>	Frequency Tolerance, 32.768 kHz Crystal Oscillator (Bluetooth low energy Stack) <sup>3</sup>	-	-	±500	ppm
f <sub>TOL_LFXO_ANT</sub>	Frequency Tolerance, 32.768 kHz Crystal Oscillator (ANT Stack) <sup>4</sup>	-	-	±50	ppm
f <sub>TOL_LFRC</sub>	Frequency Tolerance, 32.768 kHz RC Oscillator	-	-	±5	%
f <sub>TOL_CAL_LFRC</sub>	Frequency tolerance, 32.768 kHz RC after calibration	-	-	±500	ppm
f <sub>TOL_LFSYNT</sub>	Frequency Tolerance, 32.768 kHz Synthesized Oscillator	-	-	±48	ppm

Table 11: 32.768 kHz clock source comparison

1

 $<sup>^{1}</sup>$   $f_{TOL\_LFXO\_BLE}$  and  $f_{TOL\_LFXO\_ANT}$  are the maximum allowed for Bluetooth low energy and ANT applications. Actual tolerance depends on the crystal used.

 $<sup>^{\</sup>rm 2}$  The ANT protocol requires the use of an external crystal.



## 4 Firmware

Projects for the BMD-345 should utilize the Nordic Semiconductor SDK and the nRF52840 tools for new development. This will allow access to the very latest Bluetooth support from Nordic Semiconductor and provide an ongoing path as new features are released.

## 4.1 Factory image

The BMD-345 module is not loaded with a factory firmware image. The unique, public IEEE Bluetooth device address is printed on the module label and is also programmed into the UICR.

#### 4.2 SoftDevices

Nordic Semiconductor protocol stacks for Bluetooth and ANT are known as SoftDevices. SoftDevices are pre-compiled, pre-linked binary files. SoftDevices can be programmed in nRF52 series SoCs and are downloadable from the Nordic Semiconductor website. The BMD-345 with the nRF52840 SoC supports the S140 (Bluetooth low energy Central & Peripheral) and S340 (ANT and Bluetooth low energy) SoftDevices.

### 4.2.1 S140

The SoftDevice S140 is a feature complete Bluetooth 5 qualified protocol stack for the nRF52840 SoC. It supports up to 20 concurrent links in all roles. It supports Bluetooth 5 features: 2 Mbps, Long Range, Advertising Extensions and channel selection algorithm #2(CSA #2). The number of connections and bandwidth per connection are configurable, offering memory and performance optimization.

It is a complete stack with GAP, GATT, ATT, SM, L2CAP, and Link Layer. Both GATT Server and Client are supported. The broad feature set also includes Privacy 1.2, LE Data Length Extension (DLE), configurable ATT MTU, L2CAP connection-oriented channels and LE Secure Connections.

SoftDevice S140 is available for download here.

#### 4.2.2 S340

SoftDevice S340 is a combined Bluetooth 5 and ANT™ protocol stack for the nRF52840 SoC, supporting concurrent operation of the two.

It is a Bluetooth 5 qualified protocol stack that offers up to 20 concurrent links in all roles. It supports all Bluetooth 5 features: 2 Mbps, Long Range, Advertising Extensions and channel selection algorithm #2 (CSA #2). The number of connections and bandwidth per connection is configurable, offering memory and performance optimization.

It is a complete Bluetooth LE stack with GAP, GATT, ATT, SM, L2CAP, and Link Layer. Both GATT Server and Client are supported. The broad feature set also includes Privacy 1.2, LE Data Length Extension (DLE), configurable ATT MTU, L2CAP connection-oriented channels and LE Secure Connections.

It supports all ANT features and offers a variety of network topologies, including peer-to-peer, star and tree. Up to 15 individual channels are available, with broadcast, acknowledged, or burst transfer communication.

SoftDevice S340 is available for download here.

### 4.2.3 IEEE 802.15.4 (Thread and Zigbee)

IEEE 802.15.4 based protocols, such as Thread and Zigbee, on the BMD-345 are not implemented using a SoftDevice. Nordic Semiconductor provides an IEEE 802.15.4 compliant MAC stack which



does not require a SoftDevice to be loaded to operate. Nordic Semiconductor also provides pre-compiled Thread and Zigbee stacks. See the Nordic Semiconductor SDK for more information on developing applications that utilize IEEE 802.15.4. Both allow for concurrent operation with Bluetooth low energy SoftDevices.

### 4.3 Bluetooth device address

The BMD-345 modules are preprogrammed from the factory with a unique public Bluetooth device address stored in the CUSTOMER[0] and CUSTOMER[1] registers of the User Information Configuration Registers (UICR). The Bluetooth device address consists of the IEEE Organizationally Unique Identifier (OUI) combined with the hexadecimal digits that are printed on a 2D barcode and in human-readable text on the module label, as described in section 6.3. The Bluetooth device address is stored in little endian format. The most significant bytes of the CUSTOMER[1] register are 0xFF to complete the 32-bit register.

UICR Register	Address	Description	Remarks
CUSTOMER[0]	0x10001080	0xFF = Bluetooth_addr [0]	Example - actual value printed on label
CUSTOMER[0]	0x10001081	0xEE = Bluetooth_addr [1]	Example - actual value printed on label
CUSTOMER[0]	0x10001082	0xDD = Bluetooth_addr [2]	Example - actual value printed on label
CUSTOMER[0]	0x10001083	0xCC = Bluetooth_addr [3]	IEEE OUI <sup>3,4</sup>
CUSTOMER[1]	0x10001084	0xBB = Bluetooth_addr [4]	IEEE OUI <sup>3,4</sup>
CUSTOMER[1]	0x10001085	0xAA = Bluetooth_addr [5]	IEEE OUI <sup>3,4</sup>
CUSTOMER[1]	0x10001086	0xFF	Unused
CUSTOMER[1]	0x10001087	0xFF	Unused

Table 12: Bluetooth device address

<sup>&</sup>lt;sup>3</sup> The IEEE OUI for type number BMD-345-A-R-00 is: 94:54:93

<sup>&</sup>lt;sup>4</sup> The IEEE OUI for type number BMD-345-A-R-10 is one of the following: D4:CA:6E, CC:F9:57, 60:09:C3, or 6C:1D:EB



## 5 RF front end – PA / LNA

The BMD-345 uses an RF front end that incorporates a power amplifier (PA) and low noise amplifier (LNA) to achieve superior RF performance. The Skyworks RFX2411 PA / LNA IC used to increase TX power and RX sensitivity, providing a significantly increased link budget for long range connections. This section covers how to configure the RFX2411 via GPIO for radio operation.

The RFX2411 must be configured by the application firmware to allow for radio operation

By default, if all nRF52840 GPIOs are left in their default state the RFX2411 will be in a shutdown mode. There are two options for configuring the IC:

- Static method
- Dynamic method

The static method only requires setting GPIO once but results in reduced performance. The dynamic method results in the best RF performance but requires more in-depth firmware implementation. This guide will cover implementing both methods. See section 7.3 for allowed antennas.

#### 5.1 Hardware

### 5.1.1 PA/LNA modes

The table below shows the available modes of the Skyworks RFX2411 PA / LNA IC.

Mode	Description
Shutdown	No RF signal can be received or transmitted
Bypass	All RF signals lose ~10 dB of signal strength compared to receive mode (LNA gain + insertion loss) and ~29dB compared to transmit mode (with same nRF52840 output power). Compensating for the nRF52840 transmit power, bypass vs transmit mode power difference is ~10dB.
Transmit	Transmit signal from nRF52840 is amplified by ~24dB. Max allowed transmit power setting for the nRF52840 is -8 dBm (power settings depend on region, modulation mode, and channel).
Receive	Received signals from the antenna are amplified by an effective 5dB for most conditions (+10dB over bypass mode).

Table 13: Skyworks RFX2411 PA / LNA modes

### 5.1.2 PA/LNA control

The table below shows the control signal names, pin names and the state they need to be in for each mode. Switching time between states is  $< 1 \,\mu S$ .

Signal	nRF82840 signal	Shutdown mode	Bypass mode	Transmit mode	Receive mode
TX_EN	P1.05	Low	Low	High	Low
RX_EN	P1.06	Low	Low	Low	High
MODE	P1.04	Low	High	Low	Low
A-SEL	P1.02	Low	Low	Low	Low

Table 14: PA / LNA control logic

#### 5.1.3 Power limitations

To comply with regulatory power output and band-edge requirements, the following table shows the maximum allowable power setting values that can be used in the NRF\_RADIO -> TXPOWER register of the nRF52840.



Agency	World region	Maximum nRF52840 transmit power setting	RFX2411 mode during transmit	
FCC	USA	-8 dBm (0x000000F8)	PA transmit enabled	When using 802.15.4 (O-QPSK) – Channel 26 (2480MHz): Max NRF52840 TX Power setting: +6dBm (0x00000006) RFX2411 Mode during transmit: Bypass Mode
ISED	Canada	-8 dBm (0x000000F8)	PA transmit enabled	When using 802.15.4 (O-QPSK) – Channel 26 (2480MHz): Max NRF52840 TX Power setting: +6dBm (0x00000006) RFX2411 Mode during transmit: Bypass Mode
CE-RED	Europe	-16 dBm (0x000000F0)	PA transmit enabled	

Table 15: Regulatory transmit power limits



u-blox recommends consulting with an accredited certification agency to obtain the transmit power limit information for all world regions.

### 5.2 Software enablement

There are two methods for implementing control of the PA / LNA: dynamic and static. Using the dynamic method, full control of the PA / LNA is possible. Using the static method, only shutdown and bypass modes are available.

### 5.2.1 Dynamic method

The dynamic method for enabling PA / LNA provides full RF performance but requires precise timing of the control signals. The PA must be turned on right before each transmission and then turned off after; same for the LNA. Some software stacks such as the Nordic Semiconductor SoftDevices support a PA / LNA with a simple configuration (SoftDevice S140 v6.1 / nRF5 SDK v15.2 or newer required). Zephyr can be configured as well but requires a bug fix (as of Zephyr 1.13.0). Support can be manually implemented as well, provided user code can be run between each transmit and receive context switch.

The typical implementation uses the nRF52840's Peripheral-Peripheral Interface (PPI) and GPIO Task Event (GPIOTE) to automatically toggle the PA/LNA control pins, TX\_EN and RX\_EN. In the sequence below, the highlighted events (EVENTS\_READY and EVENTS\_DISABLED) are used to trigger the GPIOTE peripheral tasks (TASK\_SET and TASK\_CLEAR, respectively). This requires two PPI channels (1 and 2 are used in the example), and one GPIOTE channel (0 is used in the example) that are reconfigured between when the radio needs to transmit and receive. This method enables the GPIO to be toggled automatically for every radio packet, however the GPIOTE needs to be reconfigured when switching between modes in order to toggle the correct pin for the required mode.



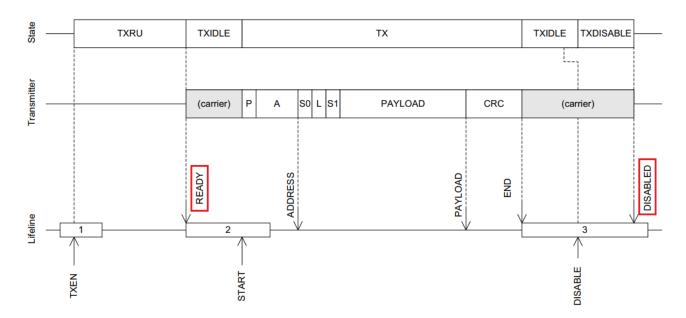


Figure 3: Radio packet event timing diagram

Code to enable full dynamic mode using the PPI and GPIOTE peripherals:

```
#define RX EN PIN
                       38 //P1.06
#define TX EN PIN
                       37 //P1.05
#define MODE PIN
                       36 //P1.04
#define A SEL PIN
                       34 //P1.02
typedef enum
    PA SHUTDOWN,
    PA TX,
    PA RX,
    PA BYPASS
} pa_modes_t;
void pa_lna_init(void)
    //configure PA / LNA pins as outputs
    nrf_gpio_cfg_output(RX_EN_PIN);
    nrf_gpio_cfg_output(TX_EN_PIN);
    nrf_gpio_cfg_output(MODE_PIN);
    nrf_gpio_cfg_output(A_SEL_PIN);
    //set PA \overline{\ } LNA pins for shutdown mode, U.FL antenna
    nrf gpio pin clear (RX EN PIN);
    nrf_gpio_pin_clear(TX_EN_PIN);
    nrf_gpio_pin clear(MODE PIN);
    nrf gpio pin clear (A SEL PIN);
    //Setup a PPI Channel for Radio Ready Event to enable PA / LNA
    NRF_PPI->CH[1].EEP = (uint32_t)&NRF_RADIO->EVENTS_READY;
    NRF_PPI->CH[1].TEP = (uint32_t)&NRF_GPIOTE->TASKS_SET[0];
    //{	ext{Setup}} PPI channel for Radio Disabled Event to disable PA / LNA
    NRF_PPI->CH[2].EEP = (uint32_t)&NRF_RADIO->EVENTS_DISABLED;
NRF_PPI->CH[2].TEP = (uint32_t)&NRF_GPIOTE->TASKS_CLR[0];
    //set radio power to max allowed (FCC)
    NRF RADIO->TXPOWER = RADIO TXPOWER TXPOWER Neg8dBm;
    //Note: FCC and ISED max power setting: -8 dBm
            CE (RED) max power setting: -16 dBm
void pa lna set mode (pa modes t mode)
  NRF_PPI->CHENCLR = 0x06;
                                        //disable PPI channels 1 and 2
```



```
NRF GPIOTE->TASKS CLR[0] = 1;
                                  //ensure current GPIOTE pin is low
if ( mode == PA SHUTDOWN )
 NRF GPIOTE->CONFIG[0] = 0;
                                   //reset GPIOTE config
else if( mode == PA TX )
 NRF_GPIOTE->CONFIG[0]= 0x32503; //TX - pin p1.05, task, toggle, init low
 \overline{NRF} PPI->CHENSET = 0x06;
                           //re-enable PPI channels 1 and 2
else if ( mode == PA RX )
 NRF GPIOTE->CONFIG[0] = 0x32603; //RX - pin p1.06, task, toggle, init low
 NRF PPI->CHENSET = 0 \times 06; //re-enable PPI channels 1 and 2
else if( mode == PA BYPASS )
 NRF GPIOTE->CONFIG[0]= 0x32403; //MODE - pin p1.04, task, toggle, init low
 NRF PPI->CHENSET = 0 \times 06;
                             //re-enable PPI channels 1 and 2
```

#### Code block 1: Full dynamic method using PPI and GPIOTE

The code above requires calling  $pa_lna_init()$  during initialization and then calling either  $pa_lna_set_mode(PA_TX)$  or  $pa_lna_set_mode(PA_RX)$  before using the radio to transmit or receive, respectively.

pa\_lna\_set\_mode() should also be called when switching the radio between transmit and receive usage, specifying the required mode. PA\_SHUTDOWN mode can be used to disable the PA / LNA, and PA\_BYPASS will enable the bypass mode during radio events (with reduced range and lower power consumption). Note: it is not necessary to call pa lna set mode() between packets.

Code to enable the PA / LNA with a Nordic Semiconductor SoftDevice:

```
static void pa lna assist(uint32 t gpio pa pin, uint32 t gpio lna pin)
   ret code t err code;
   static const uint32_t gpio_toggle_ch = 0;
   static const uint32_t ppi_set_ch = 0;
   static const uint32 t ppi clr ch = 1;
   // Configure SoftDevice PA / LNA assist
   ble opt t opt;
   memset(&opt, 0, sizeof(ble_opt_t));
    // Common PA / LNA config
   // GPIOTE channel
   opt.common opt.pa lna.gpiote ch id = gpio toggle ch;
    // PPI channel for pin learing
   opt.common_opt.pa_lna.ppi_ch_id_clr = ppi_clr_ch;
    // PPI channel for pin setting
   opt.common_opt.pa_lna.ppi_ch_id_set = ppi_set_ch;
    // PA config
    // Set the pin to be active high
    opt.common opt.pa lna.pa cfg.active high = 1;
    // Enable toggling
   opt.common_opt.pa_lna.pa_cfg.enable
    // The GPIO pin to toggle
   opt.common_opt.pa_lna.pa_cfg.gpio_pin = gpio_pa_pin;
    // LNA config
    // Set the pin to be active high
    opt.common opt.pa lna.lna cfg.active high = 1;
    // Enable toggling
   opt.common_opt.pa_lna.lna_cfg.enable
                                             = 1:
```



```
// The GPIO pin to toggle
opt.common opt.pa lna.lna cfg.gpio pin
                                       = gpio lna pin;
err code = sd ble opt set(BLE COMMON OPT PA LNA, &opt);
APP ERROR CHECK (err code);
//Insert the following code before calling scan start() or advertising start ()
/*-----/
//Set PA / LNA Mode Pin: Low for Normal operation
nrf_gpio_cfg_output(NRF_GPIO_PIN_MAP(1,4));
nrf_gpio_pin_clear(NRF_GPIO_PIN_MAP(1,4));
//Set PA / LNA Select Pin: low for u.FL
nrf_gpio_cfg_output(NRF_GPIO_PIN_MAP(1,2));
nrf_gpio_pin_clear(NRF_GPIO_PIN_MAP(1,2));
//Setup PA / LNA TX and RX control pins with the SoftDevice
pa lna assist(NRF GPIO PIN MAP(1,5), NRF GPIO PIN MAP(1,6));
//Set TX power for scan responses
sd_ble_gap_tx_power_set(BLE_GAP_TX POWER ROLE SCAN INIT, 0,
                      RADIO TXPOWER TXPOWER Neg8dBm);
//Set TX power for advertisements
sd_ble_gap_tx_power_set(BLE_GAP_TX POWER ROLE ADV, 0,
                     RADIO TXPOWER TXPOWER Neg8dBm);
//Tx power setting for connections inherit the scan or advertising power setting
```

Code block 2: Full dynamic method using Nordic Semiconductor SoftDevice

#### 5.2.2 Static method

The static method is a "simple set it and forget it" way to enable basic use of the PA / LNA, typically when using a radio stack that doesn't support a PA / LNA and there is no way to run application code when the radio switches between transmitting and receiving, such as the Wirepas® SDK. It only requires the ability to set GPIO once at startup. For full stack support, it only supports bypass mode. Importantly, the GPIO need for PA / LNA control are on Port 1 of the nRF52840.



If the radio will only transmit or receive (such as BLE broadcast or listener roles), the RFX2411 can be configured statically in transmit or receive modes, through long term performance in these modes is not tested.

#### Code to enable bypass mode:

Code block 3: Static method to set bypass mode



## 6 Mechanical specifications

## 6.1 Dimensions

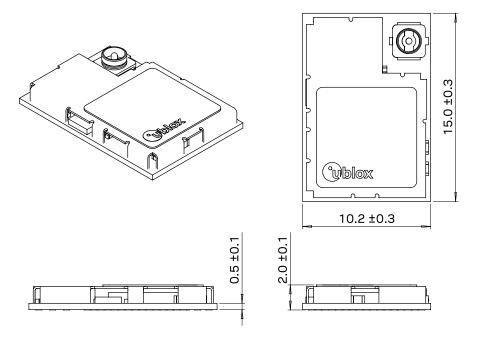


Figure 4: BMD-345 mechanical drawing (dimensions in mm)

## 6.2 Recommended PCB land pads

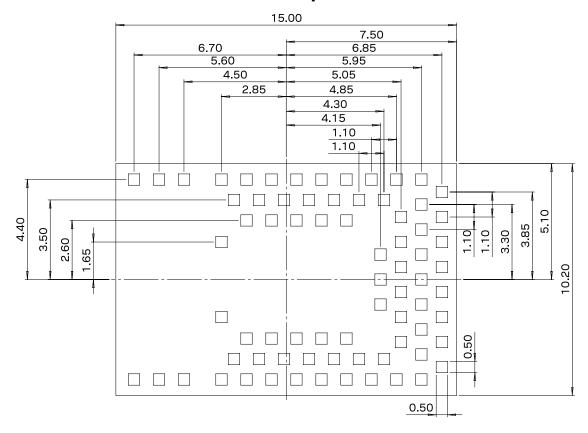


Figure 5: Recommended PCB land pads (dimensions in mm)



## 6.3 Module marking

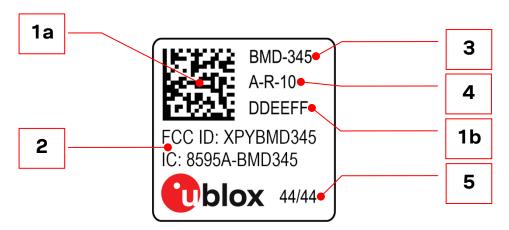


Figure 6: Module marking

Reference	Description
1a	Data Matrix with unique serial number of 19 alphanumeric symbols. The first 3 symbols represent module type number unique to each module variant, the next 12 symbols represent the unique hexadecimal Bluetooth device address of the module AABBCCDDEEFF, and the last 4 symbols represent the hardware and firmware version encoded HHFF. See section 4.3 for the IEEE OUI details (AABBCC in the Data Matrix).
1b	Second half of Bluetooth device address in human-readable format (DDEEFF above)
2	FCC and IC ID numbers
3	Product name (Model)
3 + 4	Product type number
5	Date of production encoded YY/WW (year / week)

Table 16: Module marking



## 7 RF Design notes

## 7.1 Recommended RF layout and ground plane

Using the BMD-345 with the U.FL connector relies on an external antenna, there are no ground plane requirements or keep-out area for the module itself. Refer to the external antenna datasheet for antenna placement and grounding recommendations.

### 7.2 Mechanical enclosure

When using the BMD-345 with the U.FL connector, refer to the external antenna datasheet for placement in or on a mechanical enclosure.

## 7.3 Approved external antennas

### 7.3.1 Canada (ISED) Antenna Statement

This radio transmitter [IC: 8595A-BMD345] has been approved by Innovation, Science and Economic Development Canada to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Cet émetteur radio [IC: 8595A-BMD345] a été approuvé par Innovation, Sciences et Développement économique Canada pour fonctionner avec les types d'antennes énumérés ci-dessous, avec le gain maximal admissible indiqué. Les types d'antennes non inclus dans cette liste qui ont un gain supérieur au gain maximum indiqué pour tout type répertorié sont strictement interdits pour une utilisation avec cet appareil.

#### 7.3.2 Antenna list

The antennas listed below were tested for use with BMD-345.

#	Mfg.	Part number	Max gain	Туре	Impedance	Size	Approvals
1	Pulse	W1030	2 dBi	1/4 Wave Dipole – Whip	50 Ω	Length: 108.3mm	FCC, ISED, CE, RCM
2	Taoglas	FXP73.07.0100A	2.5 dBi	1/4 Wave Dipole – Flex	50 Ω	7 mm x 47 mm x 0.1 mm	FCC, ISED, CE, RCM
3	Pulse	W1027	3.2 dBi	1/4 Wave Dipole – Whip	50 Ω	Length: 136.8mm	FCC, ISED, CE, RCM
4	Kinsun	6670113050-145	2.0 dBi	1/4 Wave Dipole – PCB	50 Ω	12 mm x 65 mm x 0.46 mm	FCC, ISED, CE, RCM

Table 17: BMD-345 Approved external antennas



## 8 BMD-345 evaluation development kit

u-blox has developed full featured evaluation boards that provide a complete I/O pin out to headers, on-board programming and debugging, 32.768 kHz crystal, power and virtual COM port over USB, BMD-345 USB connector, 64 Mb quad SPI Flash, four user LEDs, and four user buttons. The evaluation boards also provide the option to be powered from a CR2032 coin cell battery or a LiPo battery through a JST-PH connecter and have current sense resistors and headers to allow for convenient current measurements. Arduino Mega style headers are provided for easy prototyping of additional functions. The evaluation boards also support programming off-board u-blox modules based on Nordic Semiconductor nRF5 SoCs.



## 9 Qualification and approvals

## 9.1 United States (FCC)

(OEM) Integrator has to assure compliance of the entire end-product incl. the integrated RF Module. For 15 B (§15.107 and if applicable §15.109) compliance, the host manufacturer is required to show compliance with 15 while the module is installed and operating.

Furthermore, the module should be transmitting and the evaluation should confirm that the module's intentional emissions (15C) are compliant (fundamental / out-of-band). Finally, the integrator has to apply the appropriate equipment authorization (e.g. Verification) for the new host device per definition in §15.101.

The integrator is reminded to assure that these installation instructions will not be made available to the end-user of the final host device.

### 9.1.1 Labeling and user information requirements

#### The BMD-345 is assigned the FCC ID number: XPYBMD345

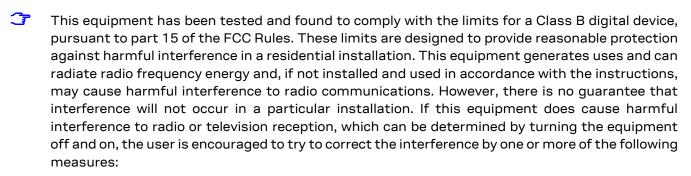
The final host device, into which this RF Module is integrated" has to be labeled with an auxiliary label stating the FCC ID of the RF Module, such as:

"Contains FCC ID: XPYBMD345

"This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions:

- 1. This device may not cause harmful interference, and
- 2. This device must accept any interference received, including interference that may cause undesired operation.

"Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment."



- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

### 9.1.2 RF exposure

⚠

The Integrator is responsible for satisfying SAR/ RF exposure requirements when the module is integrated into the host device.



All transmitters regulated by FCC must comply with RF exposure requirements. KDB 447498 General RF Exposure Guidance provides guidance in determining whether proposed or existing transmitting facilities, operations or devices comply with limits for human exposure to Radio Frequency (RF) fields adopted by the Federal Communications Commission (FCC).

This module is approved for installation into mobile host platforms and must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter guidelines. End users must be provided with transmitter operating conditions for satisfying RF Exposure compliance.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment.

This equipment shall be installed and operated with minimum distance 20cm between the radiator & body.

## 9.2 Canada (ISED)

The BMD-345 module is certified for use in Canada under Innovation, Science and Economic Development Canada (ISED) Radio Standards Specification (RSS) RSS-247 Issue 2 and RSSGen.

### 9.2.1 Labeling and user information requirements

#### The BMD-345 is assigned the IC ID number: 8595A-BMD345

The final host device, into which this RF Module is integrated has to be labeled with an auxiliary label stating the IC of the RF Module, such as:

"Contains transmitter module IC: 8595A-BMD345

"This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions:

- 1. This device may not cause interference, and
- 2. This device must accept any interference, including interference that may cause undesired operation of the device."

Le périphérique hôte final, dans lequel ce module RF est intégré "doit être étiqueté avec une étiquette auxiliaire indiquant le CI du module RF, tel que" Contient le module émetteur IC: 8595A-BMD345

"Le présent appareil est conforme aux CNR d'Industrie Canada applicables auxappareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

- 1. L'appareil ne doit pas produire de brouillage, et
- 2. L'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre lefonctionnement."

### 9.2.2 RF exposure / Déclaration d'exposition aux radiofréquences

The device has been evaluated to meet general RF exposure requirements. The device can be used in mobile exposure conditions. The min separation distance is 20cm.

L'appareil a été évalué pour répondre aux exigences générales en matière d'exposition aux RF. L'appareil peut être utilisé dans des conditions d'exposition mobiles. La distance de séparation minimale est de 20 cm.

All transmitters regulated by ISED must comply with RF exposure requirements listed in RSS-102 - Radio Frequency (RF) Exposure Compliance of Radiocommunication Apparatus (All Frequency Bands). This module is approved for installation into mobile host platforms and must not be colocated or operating in conjunction with any other antenna or transmitter except in accordance with



Industry Canada's multi-transmitter guidelines. A minimum of 20cm separation distance between any nearby person and the transmitter or antenna shall be maintained. End users must be provided with transmitter operating conditions for satisfying RF Exposure compliance.

## 9.1 European Union regulatory compliance

Information about regulatory compliance of the European Union for the BMD-345 module is available in the BMD-345 Declaration of Conformity.

### 9.1.1 Radio Equipment Directive (RED) 2014/53/EU

The BMD-345 module complies with the essential requirements and other relevant provisions of Radio Equipment Directive (RED) 2014/53/EU.

## 9.2 Australia / New Zealand (RCM)

The BMD-345 has been tested to comply with the AS/NZS 4268:2017, Radio equipment and systems – Short range devices – Limits and methods of measurement. The report may be obtained from your local FAE, and may be used as evidence in obtaining permission to use the Regulatory Compliance Mark (RCM).

Information on registration as a Responsible Party, license and labeling requirements may be found at the following websites:

Australia: http://www.acma.gov.au/theACMA/radiocommunications-short-range-devices-standard-2004

New Zealand: http://www.rsm.govt.nz/compliance

Only Australian-based and New Zealand-based companies who are registered may be granted permission to use the RCM. An Australian-based or New Zealand-based agent or importer may also register as a Responsible Party to use the RCM on behalf of a company not in Australia or New Zealand.

## 9.3 Bluetooth qualification

The Bluetooth SIG maintains the Bluetooth Specification, and ensures that products are properly tested and comply with the Bluetooth license agreements. Companies that list products with the Bluetooth SIG are required to be members of the SIG and submit the listed fees. Refer to this link for details: https://www.bluetooth.com/develop-with-bluetooth/qualification-listing

The BMD-345 Bluetooth low energy module based on Nordic Semiconductor SoCs is listed as a "Tested Component". This allows an end product based on a u-blox module to inherit the component listings without the need to run all of the tests again. The end product will often inherit several different listings, known as Qualified Design IDs (QDID), and are identified on a "Declaration of Compliance".

The list of qualified products is found here: https://launchstudio.bluetooth.com/Listings/Search

The BMD-345 primarily utilizes the S140 SoftDevice.



## 10 Environmental

### 10.1 RoHS

BMD-345 modules are in compliance with Directive 2011/65/EU, 2015/863/EU of the European Parliament and the Council on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

### **10.2 REACH**

BMD-345 modules do not contain the SVHC (Substance of Very High Concern), as defined by Directive EC/1907/2006 Article according to REACH Annex XVII.

## 10.3 California proposition 65 (P65)

This product can expose you to Nickel (metallic), which is known to the State of California to cause cancer. For more information go to www.P65Warnings.ca.gov.



Warnings are not required where the listed chemical is inaccessible to the average user of the end product.



## 11 Product handling

## 11.1 Packaging

### 11.1.1 Reel packaging

Modules are packaged on 330 mm reels loaded with 1000 modules. Each reel is placed in an antistatic bag with a desiccant pack and humidity card and placed in a 340 x 350 x 65 mm box. An antistatic warning and reel label are adhered to the outside of the bag.

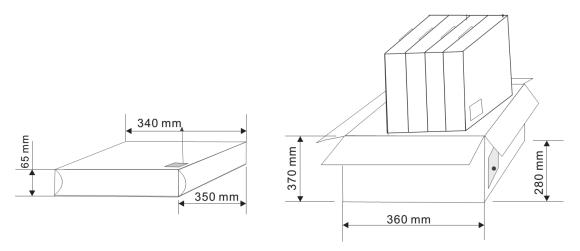


Figure 7: Reel cartons

### 11.1.2 Carrier tape dimensions

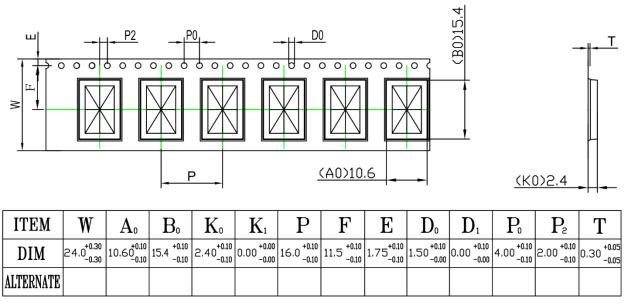


Figure 8: Carrier tape dimensions



## 11.2 Moisture sensitivity level

The BMD-345 is rated for MSL 3, 168-hour floor life after opening.

## 11.3 Reflow soldering

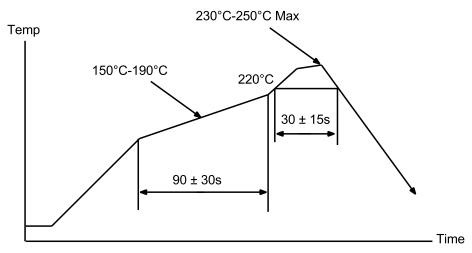


Figure 9: Reflow profile for lead free solder

## 11.4 ESD precautions

•

The BMD-345 module contains highly sensitive electronic circuitry and is an Electrostatic Sensitive Device (ESD). Handling the BMD-345 module without proper ESD protection may destroy or damage them permanently.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the BMD-345 module. Failure to observe these recommendations can result in severe damage to the device.



## 12 Ordering information

## 12.1 Ordering information

Ordering Code	Product
BMD-345-A-R	BMD-345 module, Rev A, nRF52840-QIAA, Tape & Reel, 1000 piece multiples
BMD-345-EVAL	BMD-345 Evaluation Kit w/ SEGGER J-Link-OB debug probe

Table 18: Product ordering codes



## 13 Support and other high-risk use warning

This product is neither designed nor intended for use in a life support device or system, nor for use in other fault-intolerant, hazardous or other environments requiring fail-safe performance, such as any application in which the failure or malfunction of the product could lead directly or indirectly to death, bodily injury, or physical or property damage (collectively, "high-risk environments").

⚠

u-blox expressly disclaims any express or implied warranty of fitness for use in high-risk environments.

The customer using this product in a high-risk environment agrees to indemnify and defend u-blox from and against any claims and damages arising out of such use.



## Related documents

- [1] u-blox Package Information Guide, UBX-14001652
- [2] Nordic Semiconductor, nRF52840 Product Specification
- [3] Nordic Semiconductor, nRF5 Software Development Kit
- [4] Skyworks, RFX2411 Data Sheet



For product change notifications and regular updates of u-blox documentation, register on our website, www.u-blox.com.

## **Revision history**

Revision	Date	Name	Comments	
0.5	11-Jul-2017	brec	Preliminary release for engineering samples	
1.0	12-Jun-2019	brec	Preliminary release	
R03	21-Oct-2019	brec, kgom	Document converted from Rigado to u-blox style data sheet	
R04	07-Feb-2020	brec	Product/document status changed to Engineering sample Added new section 5 for PA / LNA configuration; Added Figure 4: BMD-345 mechanical drawing; Added link to PA / LNA data sheet; Updated Figure 6: Module marking; Added ESD warning Edits for consistency with other BMD modules	
R05	31-Mar-2020	brec	Updated product photo	
R06	27-Apr-2020	brec, cnic	Updated receive sensitivity and current consumption values in Table 1.  Updated direction of RF front end control signals (TX_EN, RX_EN, PA_SW, and PA_MODE) in Table 2. Updated TX power setting in Table 15, Code block 1, and Code block 2. Noted TX output power and current consumption are expected values in Table 1. Clarified PWM feature. Corrected block diagram. Minor typographical corrections. Updated module thickness to 2.0 mm in Figure 4	
R07	09-Jun-2020	brec	Product/document status changed to Initial Production. Updated TX pow current draw, and CE test versions in Table 1. Updated FCC and ISED regulatory statements (section 9). Updated module marking (section 6.3) Removed "pending" notes for all certifications, as certifications are compl	
R08	12-Oct-2020	brec	Corrected power setting in section 5.1.1, corrected typo in sample code in section 5.2.1, added disclosure restriction	



## **Contact**

For complete contact information, visit us at www.u-blox.com.

#### u-blox Offices

#### North, Central and South America

#### u-blox America, Inc.

Phone: +1 703 483 3180 E-mail: info\_us@u-blox.com

#### **Regional Office West Coast:**

Phone: +1 408 573 3640 E-mail: info\_us@u-blox.com

#### **Technical Support:**

Phone: +1 703 483 3185 E-mail: support@u-blox.com

#### Headquarters Europe, Middle East, Africa

#### u-blox AG

Phone: +41 44 722 74 44

E-mail: info@u-blox.com

Support: support@u-blox.com

#### Asia, Australia, Pacific

#### u-blox Singapore Pte. Ltd.

Phone: +65 6734 3811
E-mail: info\_ap@u-blox.com
Support: support\_ap@u-blox.com

#### Regional Office Australia:

Phone: +61 2 8448 2016 E-mail: info\_anz@u-blox.com Support: support\_ap@u-blox.com

#### Regional Office China (Beijing):

Phone: +86 10 68 133 545
E-mail: info\_cn@u-blox.com
Support: support\_cn@u-blox.com

#### Regional Office China (Chongqing):

Phone: +86 23 6815 1588
E-mail: info\_cn@u-blox.com
Support: support\_cn@u-blox.com

#### Regional Office China (Shanghai):

Phone: +86 21 6090 4832 E-mail: info\_cn@u-blox.com Support: support\_cn@u-blox.com

#### Regional Office China (Shenzhen):

Phone: +86 755 8627 1083
E-mail: info\_cn@u-blox.com
Support: support\_cn@u-blox.com

#### Regional Office India:

Phone: +91 80 405 092 00
E-mail: info\_in@u-blox.com
Support: support\_in@u-blox.com

#### Regional Office Japan (Osaka):

Phone: +81 6 6941 3660
E-mail: info\_jp@u-blox.com
Support: support\_jp@u-blox.com

#### Regional Office Japan (Tokyo):

Phone: +81 3 5775 3850
E-mail: info\_jp@u-blox.com
Support: support\_jp@u-blox.com

#### Regional Office Korea:

Phone: +82 2 542 0861 E-mail: info\_kr@u-blox.com Support: support\_kr@u-blox.com

#### Regional Office Taiwan:

Phone: +886 2 2657 1090
E-mail: info\_tw@u-blox.com
Support: support\_tw@u-blox.com