OLED DISPLAY SPECIFICATION

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SPECIFICATION

Model No:

REX025664D

General Specification

The Features is described as follow:

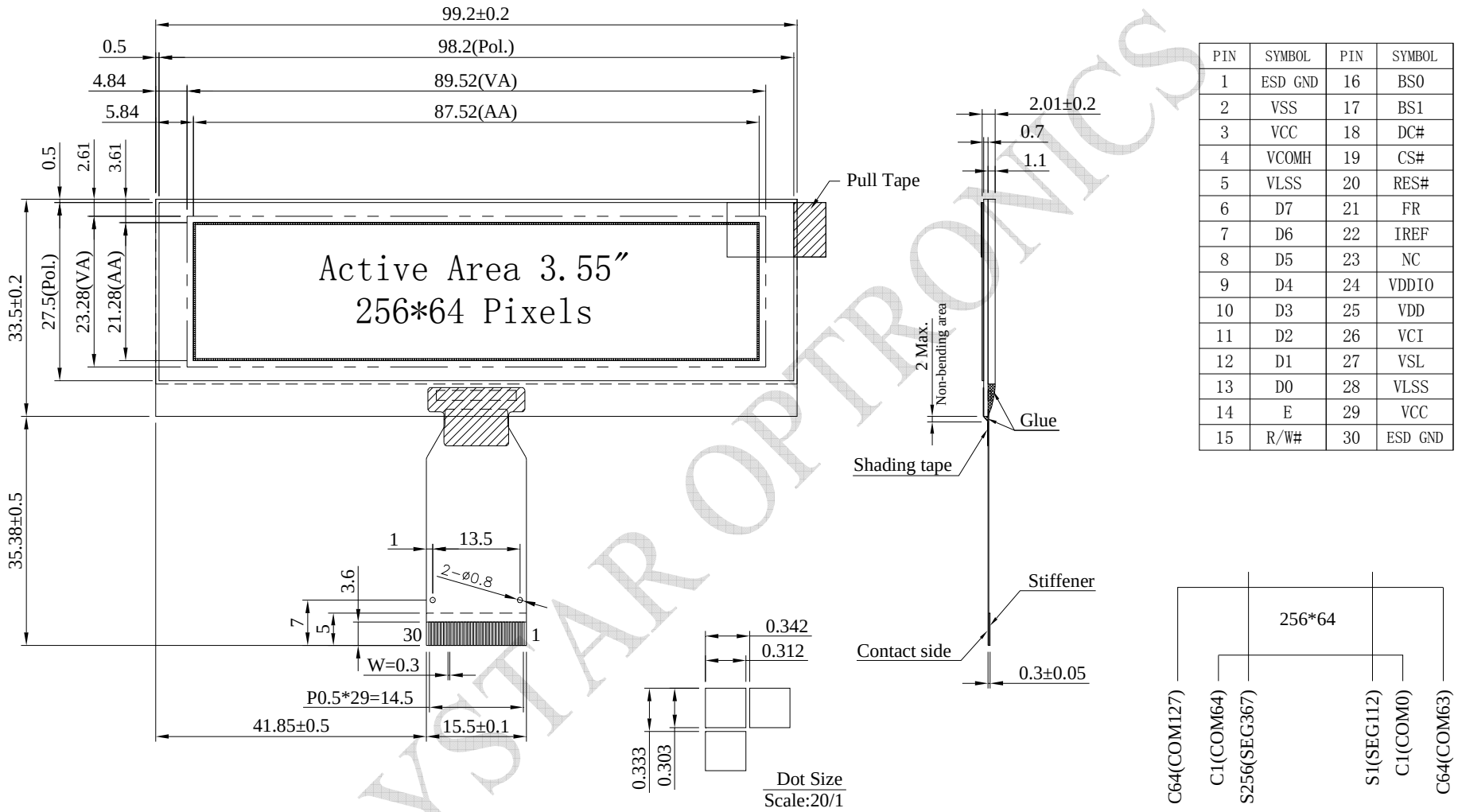
- Module dimension: 99.20 x 33.50 x 2.01 mm
- Active area: 87.52 x 21.28 mm
- Dot Matrix: 256 x 64 Dots
- Pixel Size: 0.312 x 0.303 mm
- Pixel Pitch: 0.342 x 0.333 mm
- Display Mode: Passive Matrix
- Duty: 1/64 Duty
- Gray Scale: 4 bits
- Display Color: Monochrome
- IC: SSD1322
- Interface: 6800,8080,SPI
- Size: 3.55 inch

Interface Pin Function

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>1</td><td>ESD_GND</td><td>P</td><td>Ground</td></tr>
<tr><td>2</td><td>VSS</td><td>P</td><td>Ground.</td></tr>
<tr><td>3</td><td>VCC</td><td>P</td><td>Power supply for panel driving voltage.
This is also the most positive power voltage supply pin.</td></tr>
<tr><td>4</td><td>VCOMH</td><td>P</td><td>COM signal deselected voltage level.
A capacitor should be connected between this pin and VSS.</td></tr>
<tr><td>5</td><td>VLSS</td><td>P</td><td>Analog system ground pin.</td></tr>
<tr><td>6~13</td><td>D7~D0</td><td>I/O</td><td>Host Data Input/Output Bus
These pins are 8-bit bi-directional data bus to be connected to the microprocessor’s data bus.
When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK.</td></tr>
<tr><td>14</td><td>E/RD#</td><td>I</td><td>Read/Write Enable or Read
This pin is MCU interface input.
When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low.
When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.
When serial mode is selected, this pin must be connected to VSS.</td></tr>
<tr><td>15</td><td>R/W#</td><td>I</td><td>Read/Write Select or Write
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it to “Low” for write mode.
When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.
When serial mode is selected, this pin must be connected to VSS.</td></tr>
<tr><td>16</td><td>BS0</td><td rowspan="2">I</td><td rowspan="2">Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><th>BS[1:0]</th><th>Bus Interface Selection</th></tr>
<tr><td>00</td><td>4 line SPI</td></tr>
<tr><td>01</td><td>3 line SPI</td></tr>
<tr><td>10</td><td>8-bit 8080 parallel</td></tr>
<tr><td>11</td><td>8-bit 6800 parallel</td></tr>
</table>
Note
(1) 0 is connected to VSS
(2) 1 is connected to VDDIO</td></tr>
<tr><td>17</td><td>BS1</td></tr>
</table>

18	**D/C#**	I	***Data/Command Control*** This pin is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the content at D[7:0] will be interpreted as data. When the pin is pulled LOW, the content at D[7:0] will be interpreted as command.
19	**CS#**	I	***Data/Command Control*** This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.
20	**RES#**	I	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin pull HIGH during normal operation.
21	**FR**	O	This pin is No Connection pins. Nothing should be connected to this pin. This pin should be left open individually.
22	**IREF**	I	***Current Reference for Brightness Adjustment*** This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower than 10uA.
23	**N.C.**	-	***Reserved Pin*** The N.C. pin between function pins are reserved for compatible and flexible design.
24	**VDDIO**	P	***Power Supply for I/O Pin*** It should be matched with the MCU interface voltage level.
25	**VDD**	P	***Power Supply for Core Logic Circuit*** Power supply pin for core logic operation. A capacitor is required to connect between this pin and VSS
26	**VCI**	P	***Power Supply for Operation*** VCI must always be equal to or higher than VDD and VDDIO.
27	**VSL**	P	***Voltage Output Low Level for SEG Signal*** This is segment voltage reference pin. When external VSL is not used, this pin should be left open. When external VSL is used, this pin should connect with resistor and diode to ground.
28	**VLSS**	P	***Ground of Analog Circuit*** These are the analog ground pins. They should be connected to VSS externally.
29	**VCC**	P	***Power Supply for OLED Panel*** These are the most positive voltage supply pin of the chip. They must be connected to external source.
30	**ESD GND**	P	Ground

Contour Drawing & Block Diagram



PIN	SYMBOL	PIN	SYMBOL
1	ESD GND	16	BS0
2	VSS	17	BS1
3	VCC	18	DC#
4	VCOMH	19	CS#
5	VLSS	20	RES#
6	D7	21	FR
7	D6	22	IREF
8	D5	23	NC
9	D4	24	VDDIO
10	D3	25	VDD
11	D2	26	VCI
12	D1	27	VSL
13	D0	28	VLSS
14	E	29	VCC
15	R/W#	30	ESD GND

The non-specified tolerance of dimension is ± 0.3mm.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage for Logic	VDD	-0.5	2.75	V
Low voltage power supply	VCI	-0.3	4.0	V
Power supply for I/O pins	VDDIO	-0.5	VCI	V
Supply Voltage for Display	VCC	-0.5	20.0	V
Operating Temperature	TOP	-40	+80	°C
Storage Temperature	TSTG	-40	+85	°C

Electrical Characteristics

DC Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Low Voltage power supply	VCI	—	3.1	3.3	3.5	V
Supply Voltage for Display	VCC	—	15.5	16.0	16.5	V
Logic supply voltage	VDD	—	2.4	—	2.6	V
Power for I/O pins	VDDIO	—	1.65	—	VCI	V
High Level Input	VIH	—	0.8×VDDIO	—	VDDIO	V
Low Level Input	VIL	—	0	—	0.2×VDDIO	V
High Level Output	VOH	—	0.9×VDDIO	—	VDDIO	V
Low Level Output	VOL	—	0	—	0.1×VDDIO	V
50% Check Board operating Current		VCC =16V	—	35	55	mA