Features

- ESD/Surge protection for one line with uni-directional
- Provide transient protection for each line to
  IEC 61000-4-2 (ESD) ±30kV (air/contact)
  IEC 61000-4-4 (EFT) 80A (5/50ns)
  IEC 61000-4-5 (Lightning) 14A (8/20μs)
- Suitable for, **36V and below,** operating voltage applications
- Protect one I/O line or one power line
- Fast turn-on and low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green part***

Applications

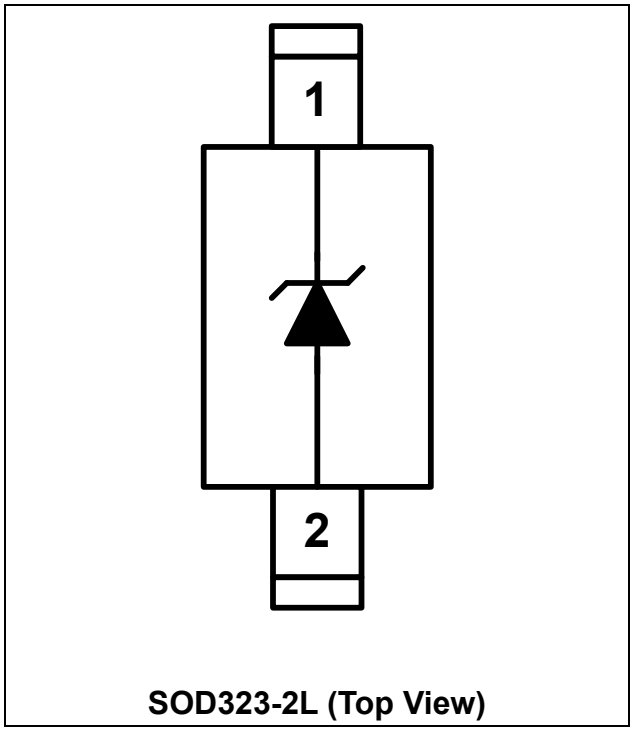
- Power supply protection
- USB VBUS protection
- Cellular handsets and accessories
- Small panel modules
- Handheld portable applications
- Low speed data or control line protection
- Peripherals
- Consumer electronics

Description

AZ4536-01L is a design which includes a uni-directional surge rated clamping cell to protect one power line, or one control line, or one low speed data line in an electronic system. The AZ4536-01L has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

AZ4536-01L is a unique design which includes proprietary clamping cell in a single package.
During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.
AZ4536-01L may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram / Pin Configuration



SOD323-2L (Top View)

Specifications

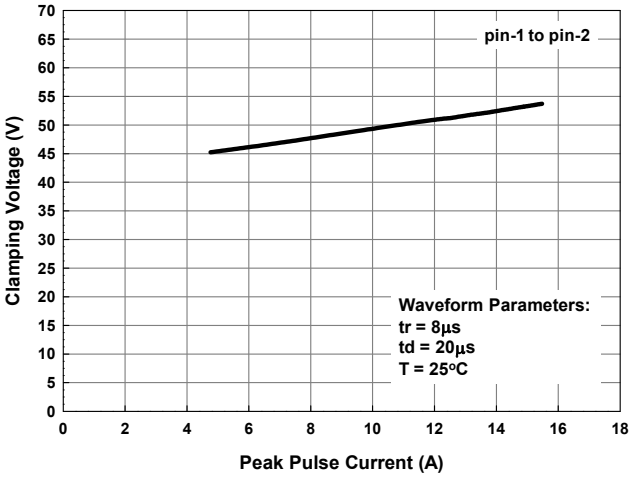
Absolute Maximum Ratings (T_A= 25°C, unless otherwise specified)			
Parameter	**Symbol**	**Rating**	**Unit**
Peak Pulse Current (t_p =8/20μs)	I_{PP}	14	A
Operating Voltage (pin-1 to pin-2)	V_{DC}	39.6	V
ESD per IEC 61000-4-2 (Air)	V_{ESD-1}	±30	kV
ESD per IEC 61000-4-2 (Contact)	V_{ESD-2}	±30	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +125	°C
Storage Temperature	T_{STO}	-55 to +150	°C

Electrical Characteristics						
Parameter	**Symbol**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Reverse Stand-Off Voltage	V_{RWM}	Pin-1 to pin-2, T=25 °C.			36	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = 36V, T=25 °C, pin-1 to pin-2.			0.5	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C, pin-1 to pin-2.	40		46	V
Forward Voltage	V_F	I_F = 15mA, T=25 °C, pin-2 to pin-1.	0.6		1.2	V
Surge Clamping Voltage	$V_{CL-surge}$	I_{PP}=5A, t_p=8/20μs, T=25 °C, pin-1 to pin-2.		45		V
		I_{PP}=14A, t_p=8/20μs, T=25 °C, pin-1 to pin-2.		52		V
ESD Clamping Voltage (Note 1)	V_{CL-ESD}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), T=25 °C, contact mode, pin-1 to pin-2.		45		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2 0~+8kV, T=25 °C, contact mode, pin-1 to pin-2.		0.19		Ω
Channel Input Capacitance	C_{IN}	V_R = 0V, f = 1MHz, T=25 °C, pin-1 to pin-2.		160		pF

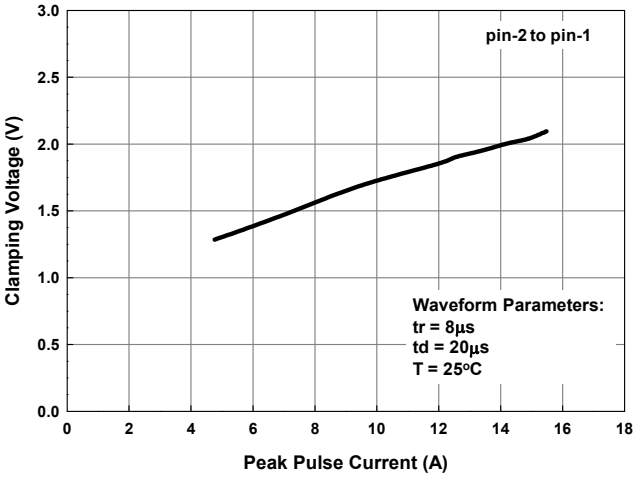
Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.
TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 1ns.

Typical Characteristics

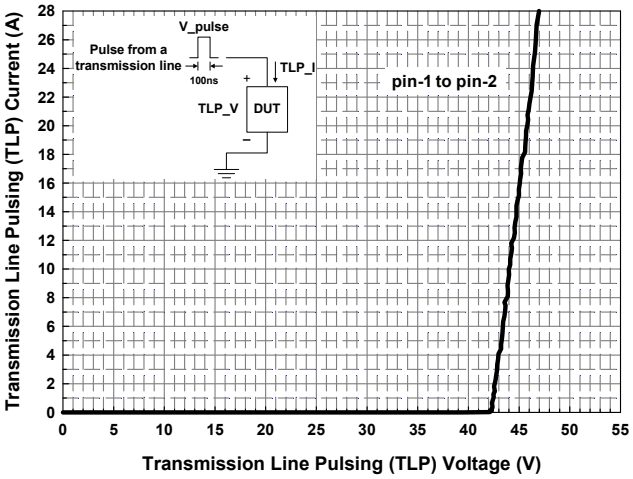
Reverse Clamping Voltage vs. Peak Pulse Current



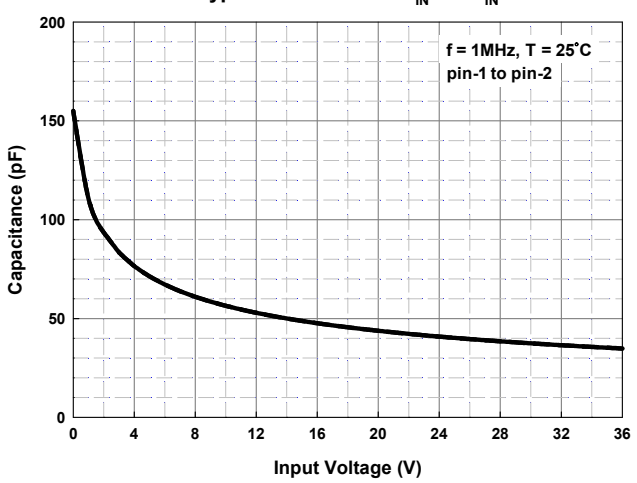
Forward Clamping Voltage vs. Peak Pulse Current



Transmission Line Pulsing (TLP) Measurement



Typical Variation of C_{IN} vs. V_{IN}



Applications Information

The AZ4536-01L is designed to protect one line against system ESD/EFT/Lightning pulses by clamping it to an acceptable reference.

The usage of the AZ4536-01L is shown in Fig. 1. Protected line, such as data line, control line, or power line, is connected at pin-1. The pin-2 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ4536-01L should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ4536-01L.
- Place the AZ4536-01L near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

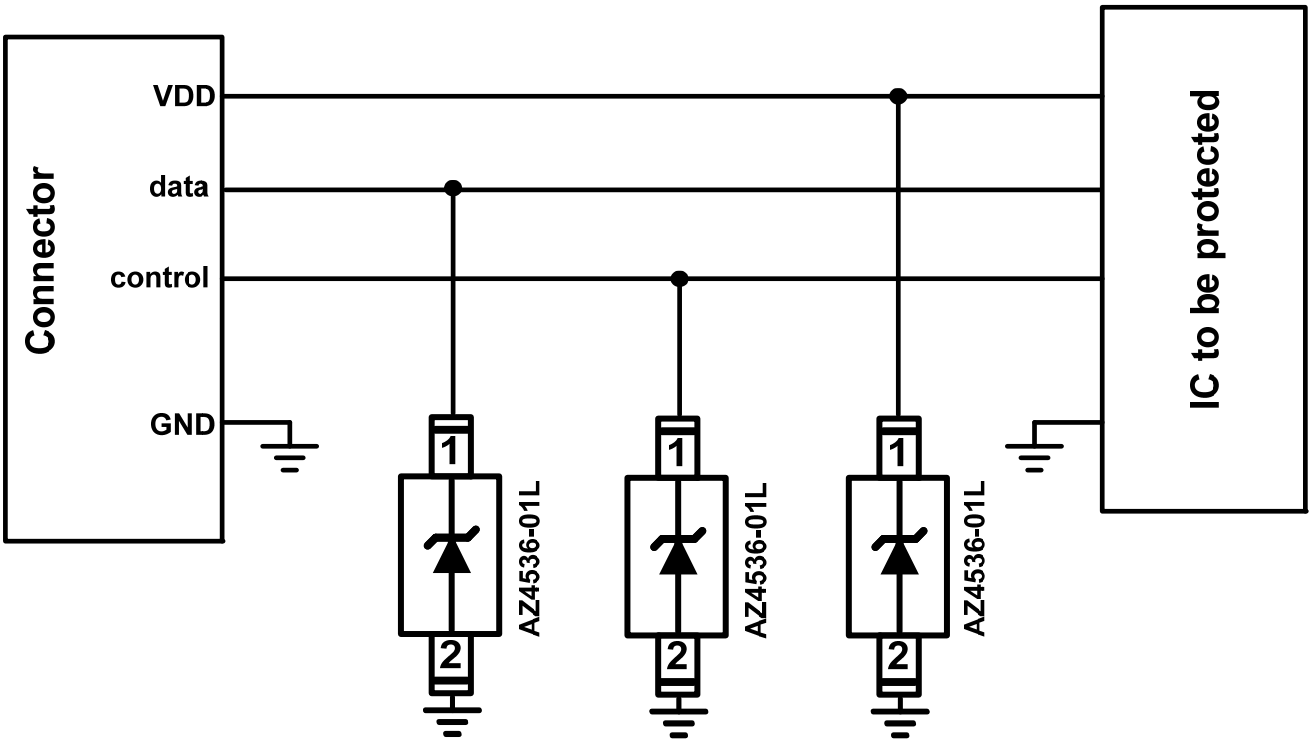


Fig. 1

Fig. 2 shows another simplified example of using AZ4536-01L to protect the control line, low speed data line, and power line from ESD transient stress.

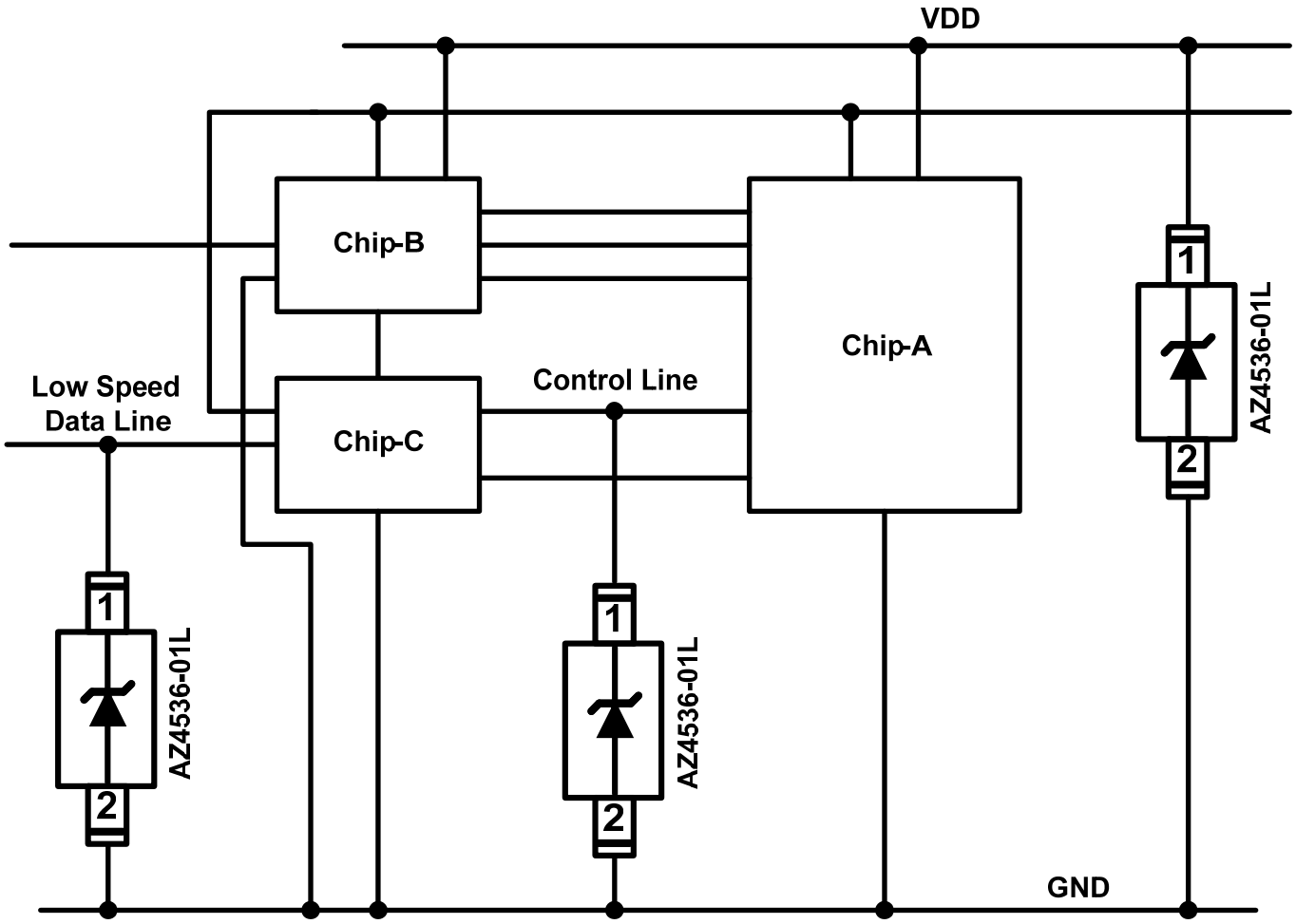


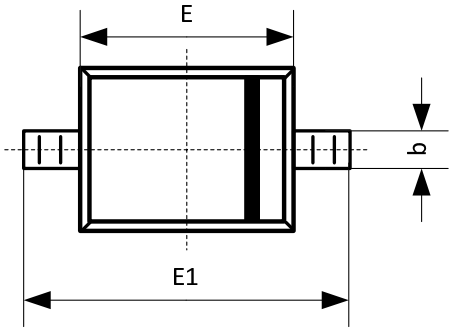
Fig. 2

Mechanical Details

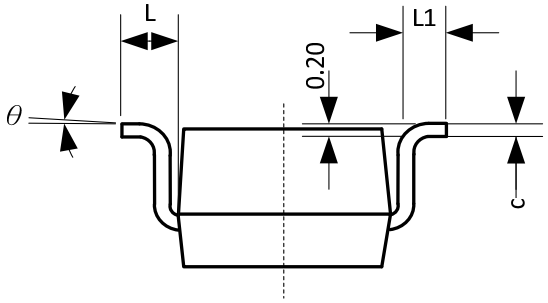
SOD323-2L

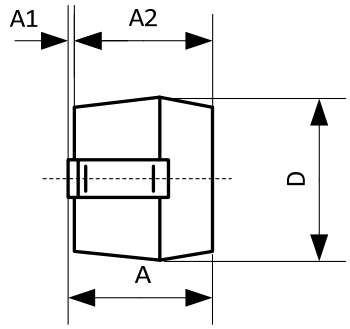
Package Diagrams

TOP VIEW



SIDE VIEW

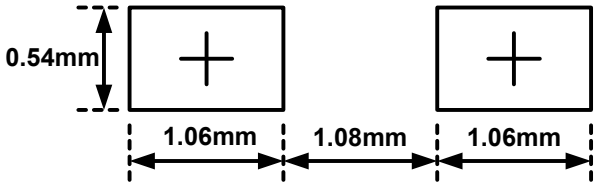




Package Dimensions

Symbol	Millimeters	
	MIN.	MAX.
A	0.80	1.00
A1	0.00	0.10
A2	0.80	0.90
b	0.25	0.35
c	0.08	0.15
D	1.20	1.40
E	1.60	1.80
E1	2.50	2.70
L	0.475REF	
L1	0.25	0.40
θ	0	8

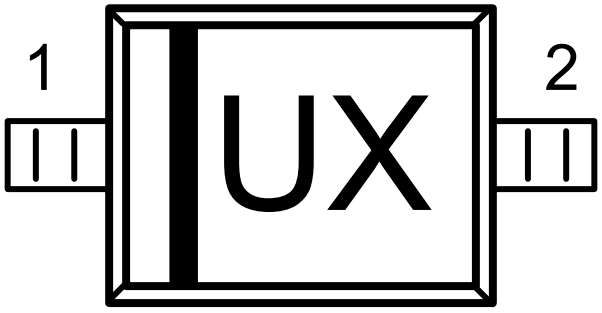
Land Layout



Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

Marking Code



U = Device Code
X = Date Code

Part Number	Marking Code
AZ4536-01L.R7G (Green Part)	UX

Note. Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ4536-01L.R7G	Green	T/R	7 inch	3,000/reel	4 reels=12,000/box	6 boxes=72,000/carton

Revision History

Revision	Modification Description
Revision 2022/11/18	Formal Release.