1ch Video Amplifier & 2Vrms Ground Referenced Stereo Line Amplifier

■ GENERAL DESCRIPTION

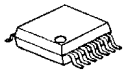
The **NJW1230** is an audio line Amplifier with 1ch video amplifiier.

Audio line amplifier can swing 2Vrms (5.6V peak-to-peak) signal at 3.3V operating voltage.

Ground-referenced outputs eliminate output coupling capacitor. The pop noise suppression circuit removes a pop noise at the power-on and power-off.

Video amplifier contained LPF circuit. Internal 75Ω driver is easy to connect TV monitor directly.

■ PACKAGE OUTLINE



NJW1230V

■ APPLICATION

- Blu-ray/DVD player
- Home theater/Set top box
- AV receiver

■ FEATURES

- Operating Voltage 2.7 to 3.6V
- Power Save circuit
- Package Outline SSOP16

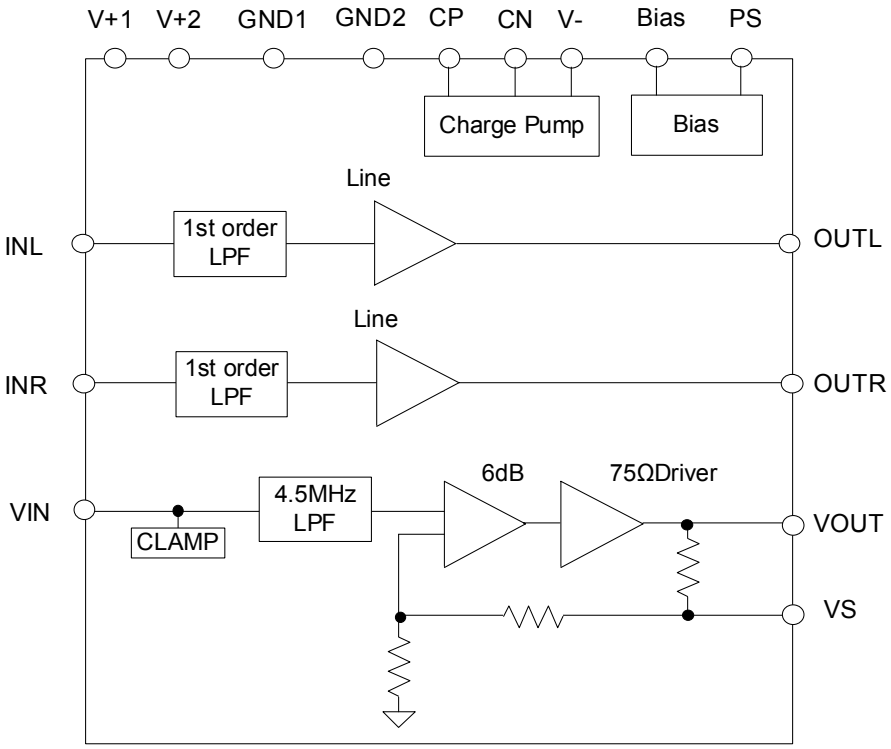
Audio block

- Output Coupling Capacitor-less
- Pop Noise Suppression Circuit

Video block

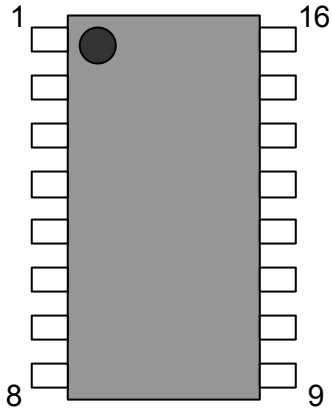
- LPF 4.5MHz
- 6dB Amplifier
- 75Ω Driver (2-system drive)

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

SSOP16



No.	Symbol	Function
1	V+1	V+ Power Supply for Audio
2	CP	Flying Capacitor Positive Terminal for Audio
3	CN	Flying Capacitor Negative Terminal for Audio
4	V-	V- Power Supply for Audio
5	MUTE	Mute / Pop Noise Suppression for Audio
6	GND1	Ground for Audio
7	VIN	Video Input
8	VS	Sag Correction
9	VOUT	Video Output
10	PS	Powe save for Video
11	GND2	Ground for Video
12	V+2	V+ Power Supply for Video
13	OUTR	Rch Output
14	INR	Rch Input
15	INL	Lch Input
16	OUTL	Lch Output

■ **ABSOLUTE MAXIMUM RATING** (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V^+	4	V
Power Dissipation	P_D	430(Note1)	mW
Maximum Input Voltage	V_{IN}	-0.3 to V^+ +0.3	V
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-40 to +125	°C

(Note1) EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 2layer, FR-4) mounting

■ **RECOMMENDED OPERATING CONDITIONS**(Ta=25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating voltage	V^{+1}	1pin	2.7	3.3	3.6	V
	V^{+2}	12pin	2.7	3.3	3.6	

■ **ELECTRICAL CHARACTERISTICS**

♦**AUDIO CHARACTERISTICS**

(Ta=25°C, V^+=3.3V, f=1kHz, Vin=1Vrms, Mute=OFF, R_L=47kΩ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{DD}	No signal	-	5	10	mA
Output Gain	G_V		5.2	6.2	7.2	dB
Output Gain Error	ΔG_V		-0.5	0	0.5	dB
Maximum Output Voltage Level	V_{OMAX}	THD=1%	-	2.2	-	Vrms
Mute Level	V_{MUTE}	Rg=0Ω, MUTE=ON	-	-110	-	dB
Equivalent Input Noise Voltage	V_{NO}	Rg=0Ω, BW:400Hz-22kHz	-	-106	-	dB
Total Harmonic Distortion	THD	BW:400Hz-22kHz	-	0.003	-	%
Channel Separation	CS	Rg=600Ω	80	-	-	dB
Cut-off Frequency	f_C	2^{nd} LPF	100	150	200	kHz
Output Offset Voltage	Vos	Rg=0Ω	-	1	5	mV
Power Supply Rejection Ratio	PSRR	Vripple=1kHz / 100mVrms	-	45	-	dB
MUTE High Level	MuteH	Mute=OFF	$0.8V^+$	-	V^+	V
MUTE Low Level	MuteL	Mute=ON	0	-	$0.2V^+$	V

♦ **CONTROL CHARACTERISTICS**

PARAMETER	STATUS	NOTE
MUTE	H	OFF(Active)
	L	ON (Mute)

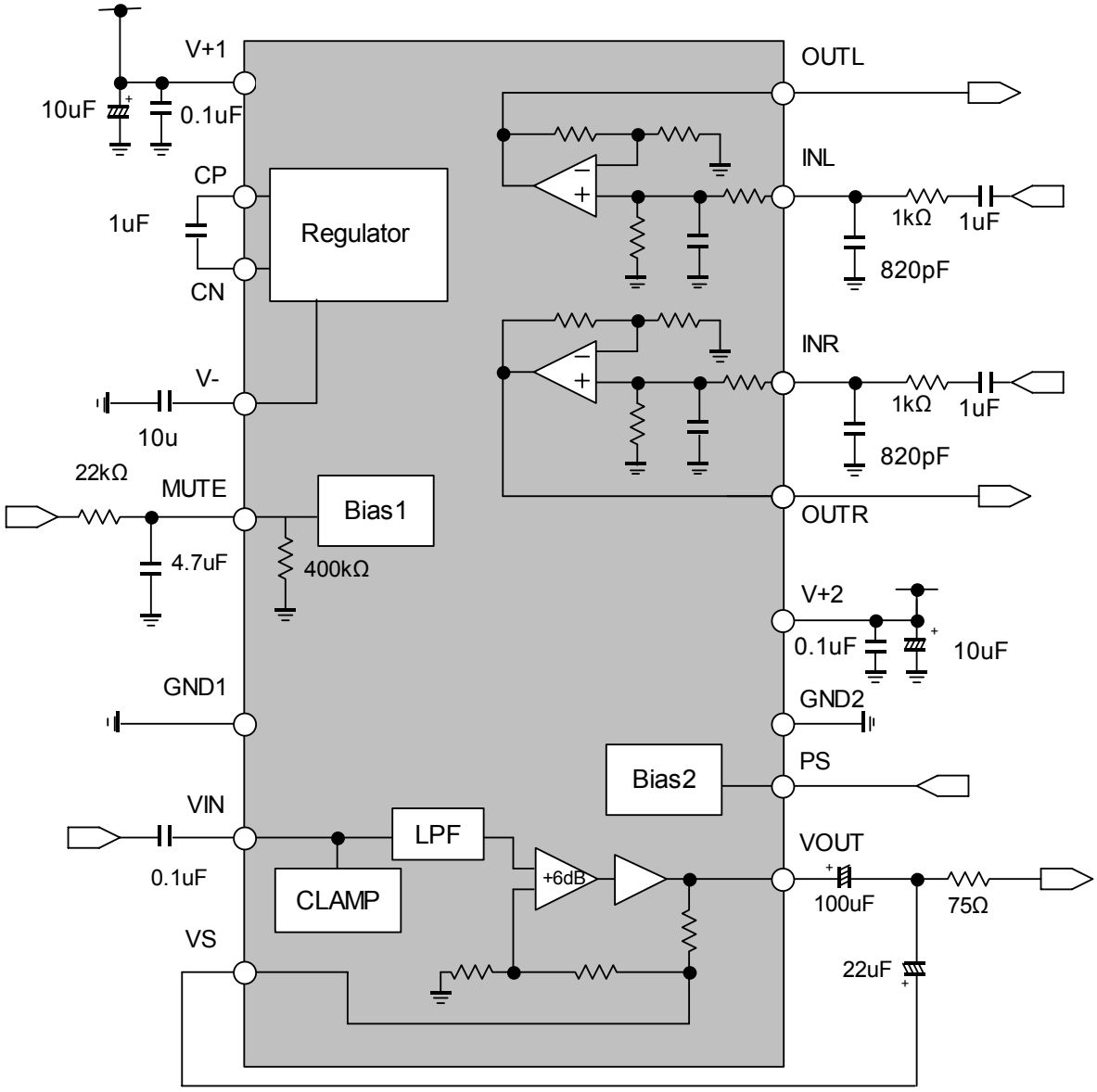
♦**VIDEO CHARACTERISTICS** (Ta=25°C, V^+=3.3V, R_L=150Ω, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}	No Signal	-	8.0	12.0	mA
Operating Current at Power Save	Isave	No Signal, Power Save Mode	-	30	50	μA
Maximum Output Voltage Swing	Vom	f=100kHz,THD=1%	2.2	2.5	-	Vp-p
Voltage Gain	Gv	Vin=100kHz, 1.0Vp-p,Input Sine Signal	5.6	6.0	6.4	dB
Low Pass Filter Characteristic	Gfy4.5M	Vin=4.5MHz/100kHz, 1.0Vp-p	-0.6	-0.1	0.4	dB
	Gfy19M	Vin=19MHz/100kHz, 1.0Vp-p	-	-33	-23	
Differential Gain	DG	Vin=1.0Vp-p, 10step Video Signal	-	0.5	-	%
Differential Phase	DP	Vin=1.0Vp-p, 10step Video Signal	-	0.5	-	deg
S/N Ratio	SNv	Vin=1.0Vp-p, R_L=75Ω 100% White Video Signal, 100KHz to 6MHz	-	65	-	dB
Power save High Level	VthH	Active	1.8	-	V^+	V
Power save Low Level	VthL	Non-active	0	-	0.3	

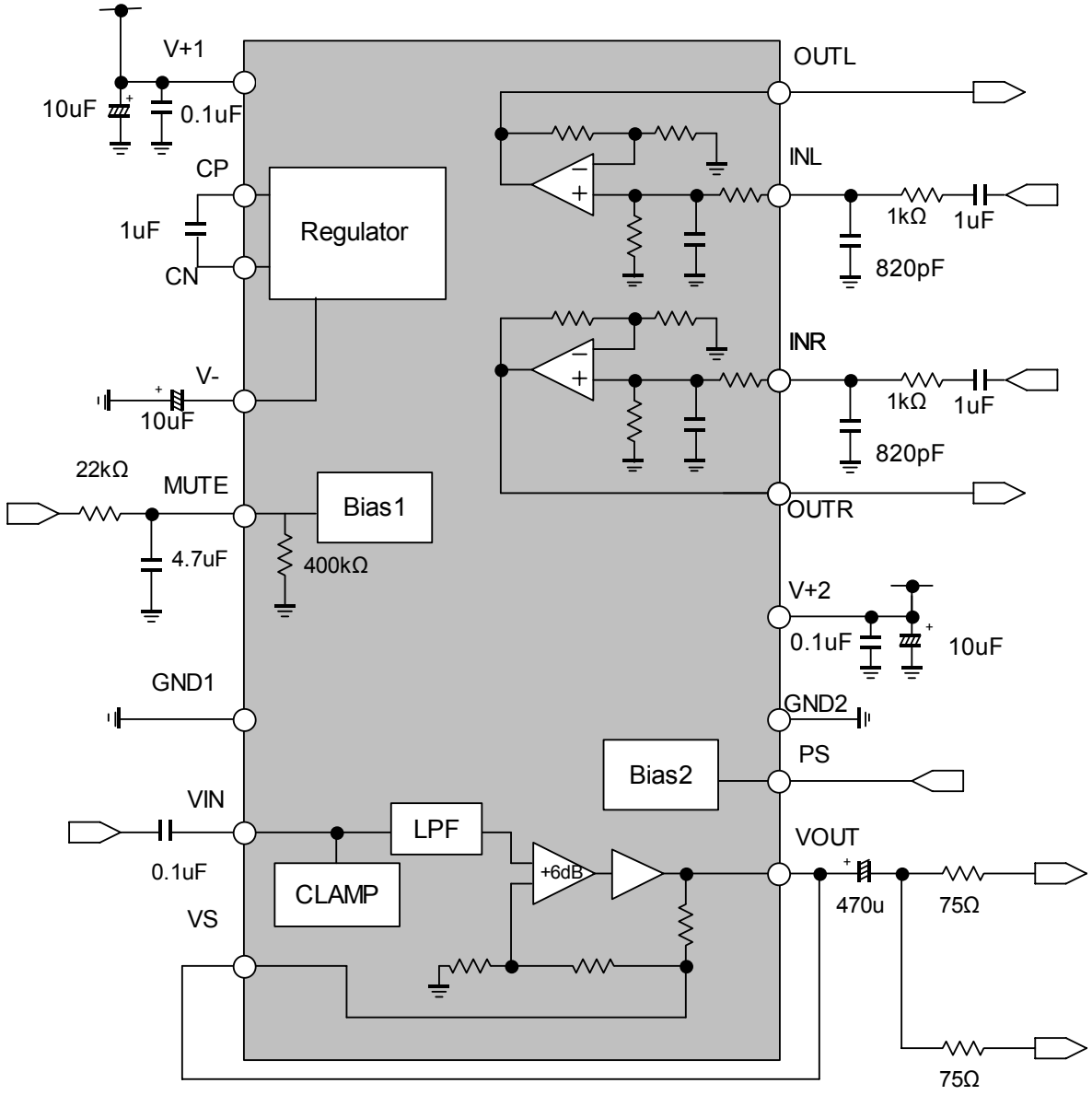
♦ **CONTROL CHARACTERISTICS**

PARAMETER	STATUS	NOTE
Power Save	H	Power Save: OFF(Active)
	L	Power Save: ON (Mute)

■ **APPLICATION CIRCUIT 1(Video output is AC coupling)**

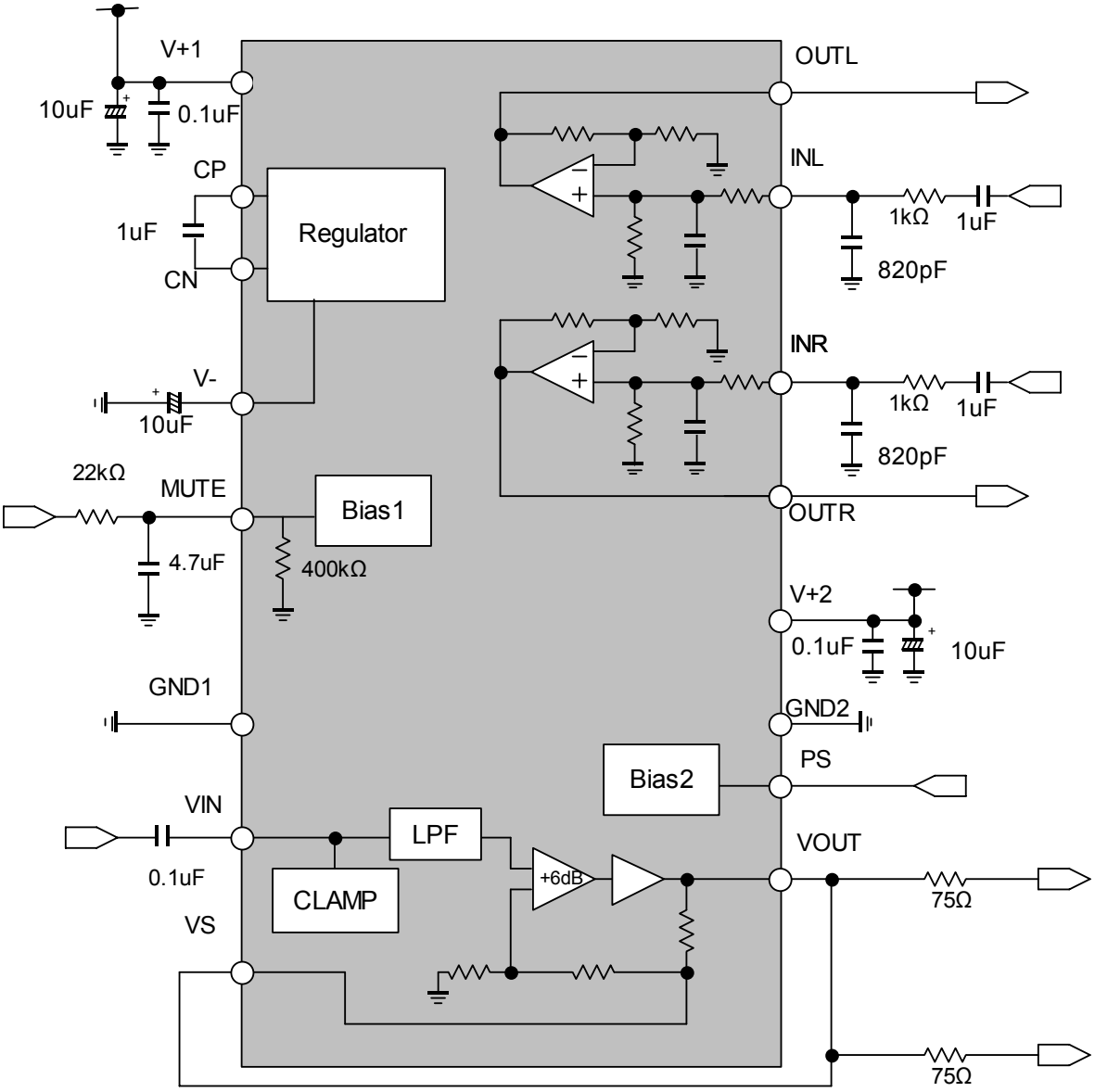


■ **APPLICATION CIRCUIT 2(Video output is AC coupling 2-Drive)**



Note)
When AC coupling and the video output connect two line of 150Ω ,connect the coupling capacitor after connecting the Vout pin and Vsag pin. The recommended value is 470μF or more.

■ **APPLICATION CIRCUIT 2(Video output is DC coupling)**



Note)
Vout outputs DC of 0.33V.

■ APPLICATION NOTE

NJW1230 built in stereo line amplifier. Stereo line amplifier is that eliminates the need for external dc-blocking output capacitors. Also built in pop suppression circuitry to eliminate disturbing pop noise during power-on, power-off and mute-control.

Video block is low voltage operate video amplifier with LPF. It direct coupling to TV monitor with built in 75Ω - driver. It is able to both AC – coupling and DC – coupling. Input signal is CVBS, also suitability low power application with built in power save circuit

1. Audio block's operating principle

Audio block of NJW1230 is stereo line amplifier. It has the built-in non-inverted input operational amplifiers, voltage inverter, and pop noise suppression circuitry (Fig.1).

The voltage inverter for stereo line amplifier eliminates the need for external dc-blocking output capacitors.

The pop suppression circuitry for stereo line amplifier eliminates the pop noise during power-on, power-off and mute-control.

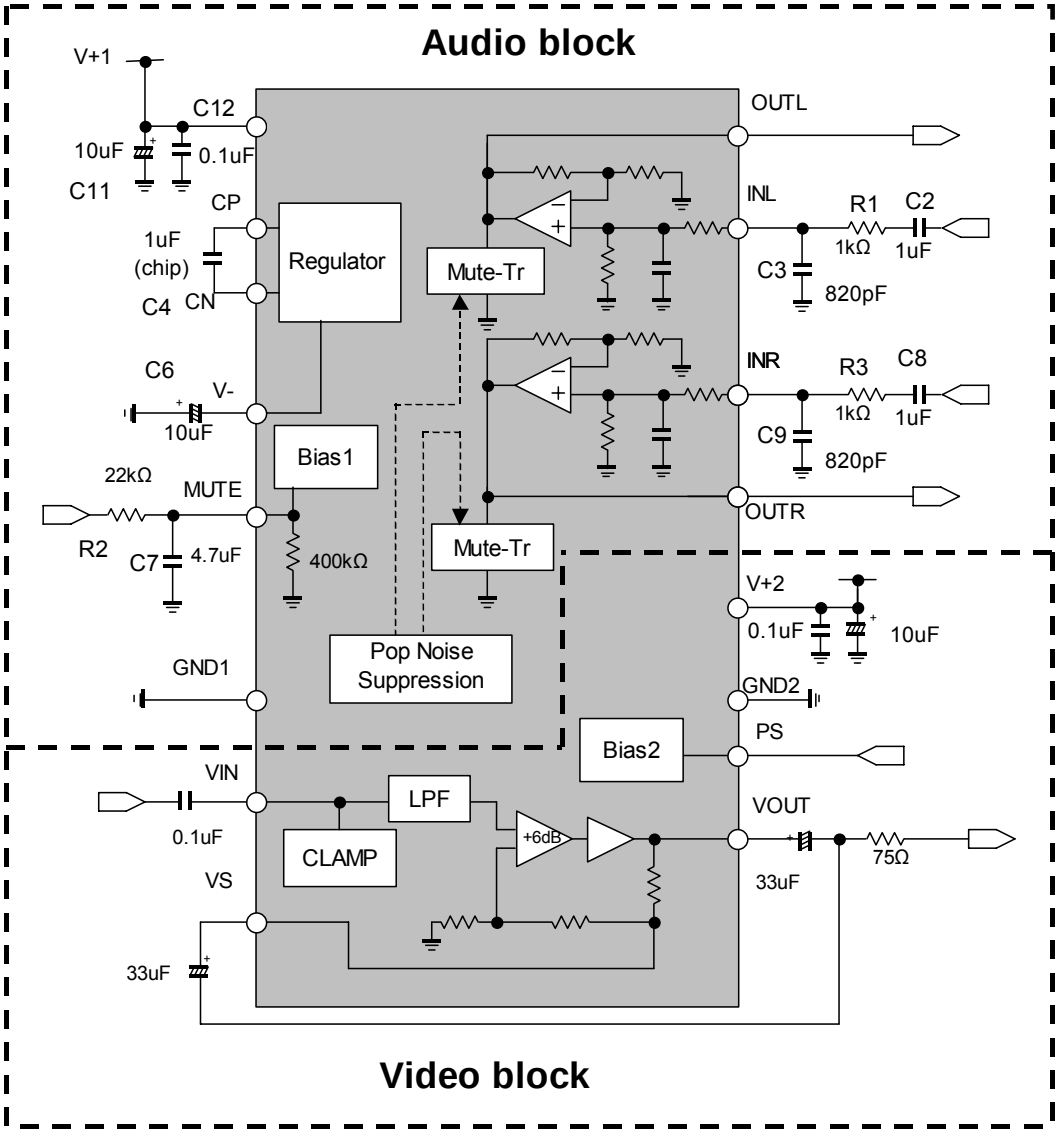


Fig.1 NJW1230 block diagram

1.1 External parts

1.1.1 Input coupling capacitors C_i (C2, C8)

The input coupling capacitor (C_i) and the total of the external resistance (R1, R3) and the input resistance (R_{in}=218kΩ typ.) for the non-inverted terminal form a high-pass filter with the corner frequency determined in [fc=1/(2π x (R1+218kΩ) x C_i)). It is necessary to adjust 1uF or more.

1.1.2 Flying capacitor (C4)

Use capacitors with a low-ESR (ex. ceramic capacitors) for optimum performance. Design to provide low impedance for the wiring between CP terminal (2pin), CN terminal (3pin), and the flying capacitor (C4).

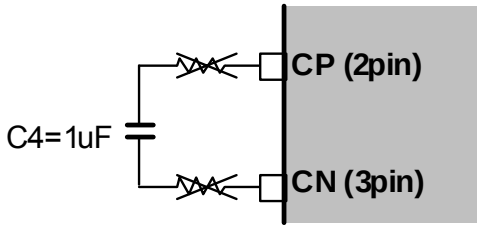


Fig.2 external circuit of 2pin, 3pin

1.1.3 Hold capacitor (C6)

Use capacitors with a low-ESR (ex. ceramic capacitors) for optimum performance. Design to provide low impedance for the wiring between the hold capacitor (C6), V- terminal (6pin) and the GND on the PCB.

Separate the GND pattern connecting to the hold capacitor (C6) from that connecting to the GND terminal (6pin), thus suppressing the influence of switching noise by removing the common impedance of the GND wiring.

Design no short-circuits of V- terminal (4pin) and V+ terminal (1pin) on the PCB pattern.

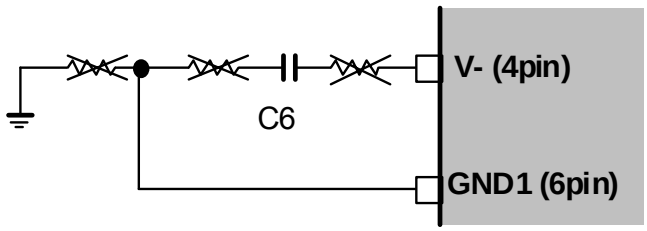


Fig.3 external circuit of 4pin, 6pin

1.1.4 Mute terminal pop noise countermeasures (R2, C7)

Mute terminal (5pin) needs time constant more than R2 x C7=0.1. It is necessary to adjust 22kΩ or less.

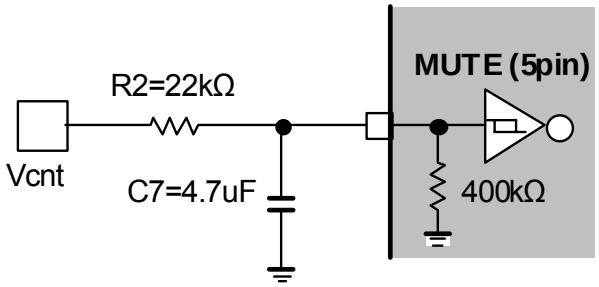


Fig.4 external circuit of 5pin

1.2 Control of V+ terminal and Mute terminal

1.2.2 Power-on procedure

1. Turn on the V+.
2. After 100msec from power on, change the control voltage of MUTE terminal (Vcnt) from "Low" to "High".

* It is necessary to stabilize an IC for 100msec.

By releasing the MUTE function, the output terminal output the signal.

1.2.3 Power-off procedure

1. Change the control voltage of MUTE terminal (Vcnt) from "High" to "Low".

By the MUTE function, the output signals are stopped from output terminal.

2. Turn off the V+ after “2RC” sec from MUTE.

* It is necessary to stabilize a MUTE condition for “2RC” sec.

Ex.) R2=22kΩ, C7=4.7uF -> 2R2 x C7=200msec

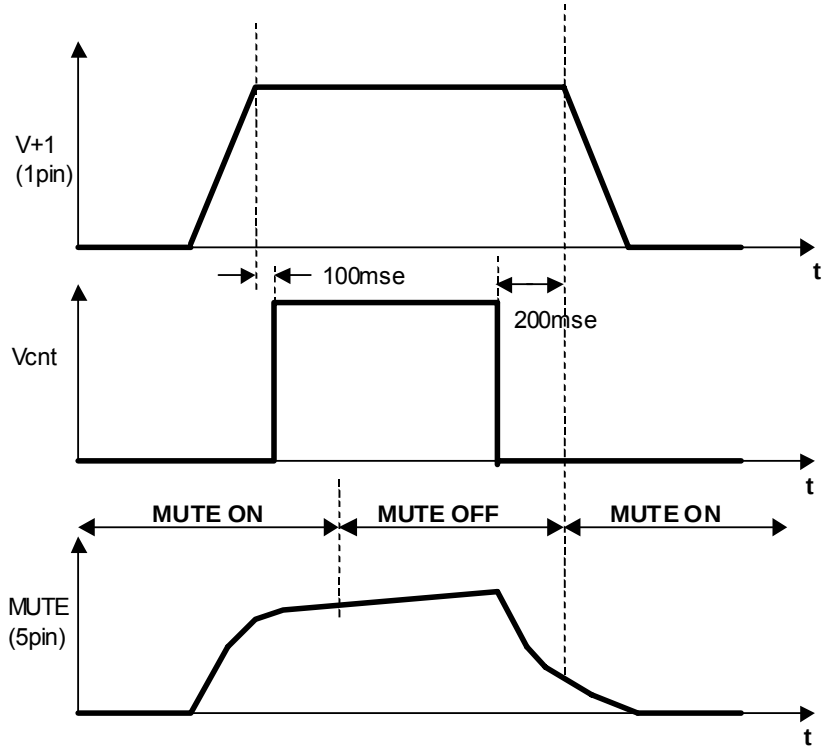


Fig.5 Power-on / Power-off timing chart

2. Video block's operating principle

Video block is low voltage video amplifier with LPF. It direct coupling to TV monitor with built in 75Ω - driver. It is able to both AC – coupling and DC – coupling. Input signal is CVBS, also suitability low power application with built in power save circuit

2.1 Typical application circuit (at use SAG collection circuit)

This application circuit is deal with the possibility of portable system that be bound by space. It can make output capacitor smaller by SAG collection circuit. However, this circuit has possibilities deterioration of SAG, and get out synchronization at rapid changes in brightness of input signal. Therefore we recommend measurement at comprehend low frequency of input signal (ex. WHITE – BLACK bounce signal).

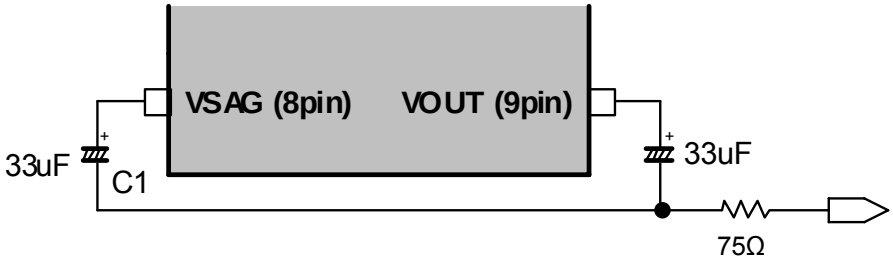


Fig.6 Typical application circuit

2.2 Unused SAG collection circuit

We recommend unused SAG collection circuit at be not bound by space. Connect with VOUT terminal and VSAG terminal. Then connect to output capacitor of over 470uF.

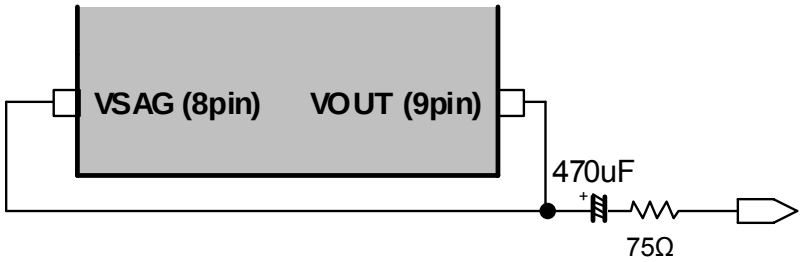


Fig.7 Unused SAG collection circuit

2.3 Two drive application circuit

This circuit can drive 150Ωx2. However get out synchronization at rapid changes in brightness of input signal. We recommend measurement at comprehend low frequency of input signal (ex. WHITE – BLACK bounce signal).

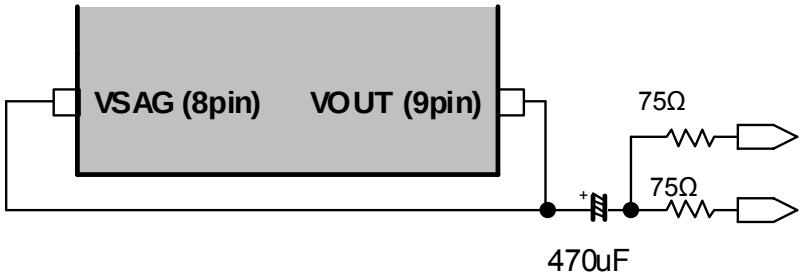


Fig.7 Two drive application circuit

2.4 DC – coupling application circuit

VOUT terminal output 0.33V all of the time.

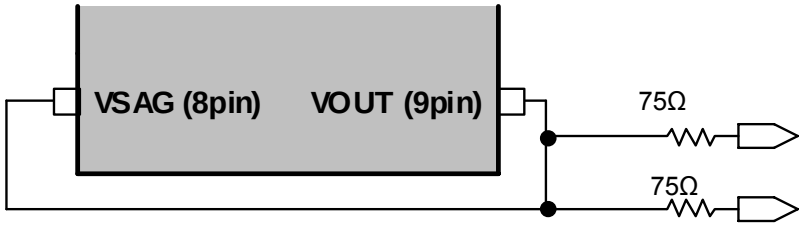


Fig.8 DC – coupling application circuit

3. How to trace V+1(1pin), V+2(12pin), GND1(6pin), GND2(11pin)

V+1 and GND1 for audio block. V+2 and GND2 for video block. Audio block built in charge pump circuit. As a result, clock noise of charge pump circuit on between V+1 and GND1. Video output is take a leaf from clock noise at clock noise on between V+2 and GND2. Each terminal make a separation trace. Cut down common impedance of between audio block and video block.

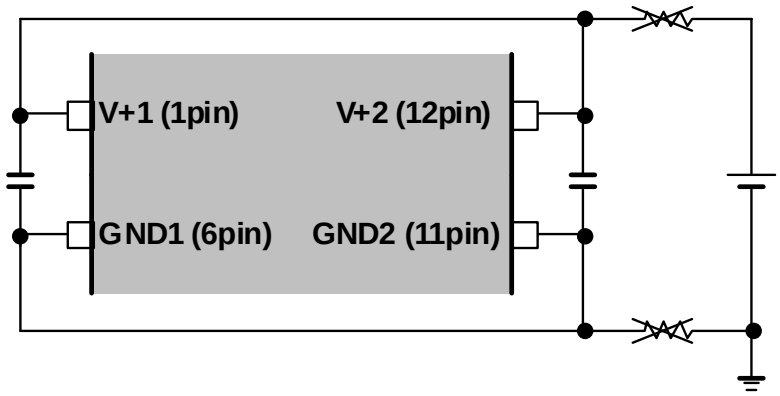


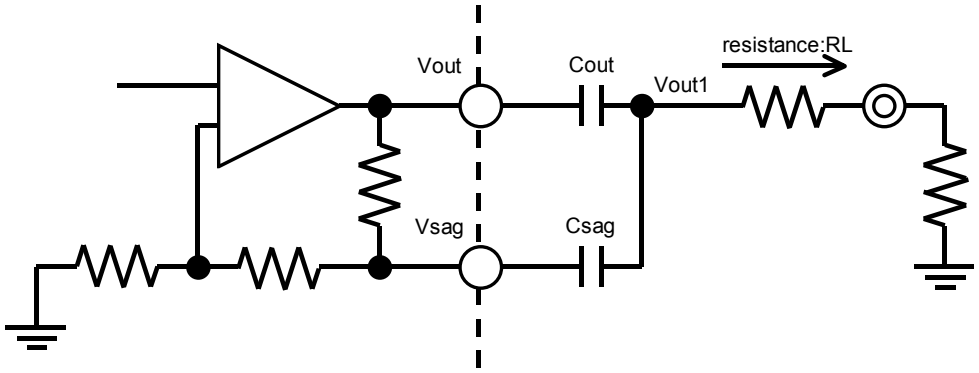
Fig.9 external circuit of 1pin, 6pin, 11pin, 12pin

♦ **SAG correction circuit**

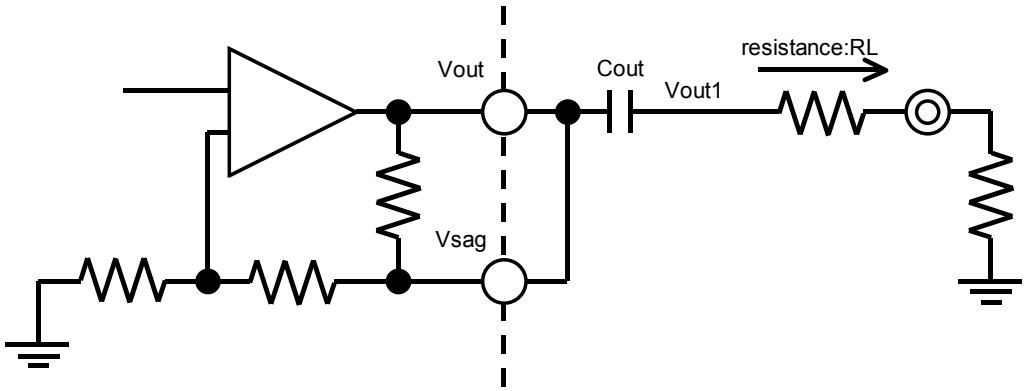
SAG correction circuit is a circuit to correct for low-frequency attenuation by high-pass filter consisting of the output coupling capacitance and load resistance. Low-frequency attenuation raises the sag in the vertical period of the video signal.

Capacitor for Vsag (Csag) is connected to the negative feedback of the amplifier. This Csag increase the low frequency gain to correct for the attenuation of low frequency gain.

Example SAG collection circuit

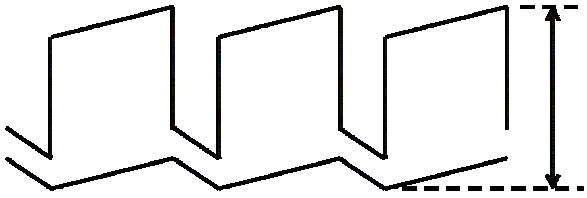


Example of not using sag compensation circuit

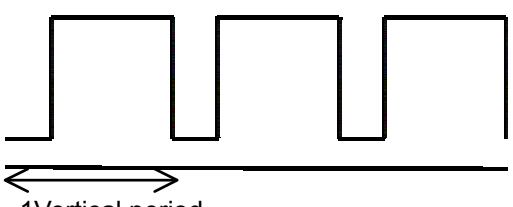


Waveform of Vout terminal and Vout1 terminal

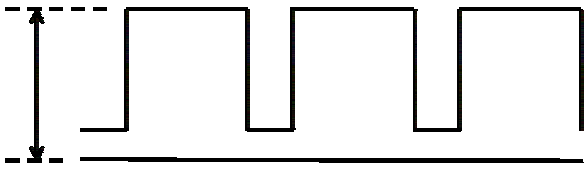
using SAG correction circuit
Waveform of Vout



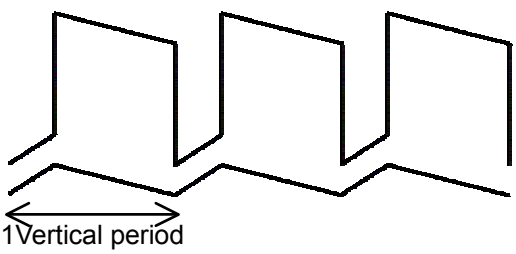
Waveform of Vout1



not using SAG correction circuit
Waveform of Vout

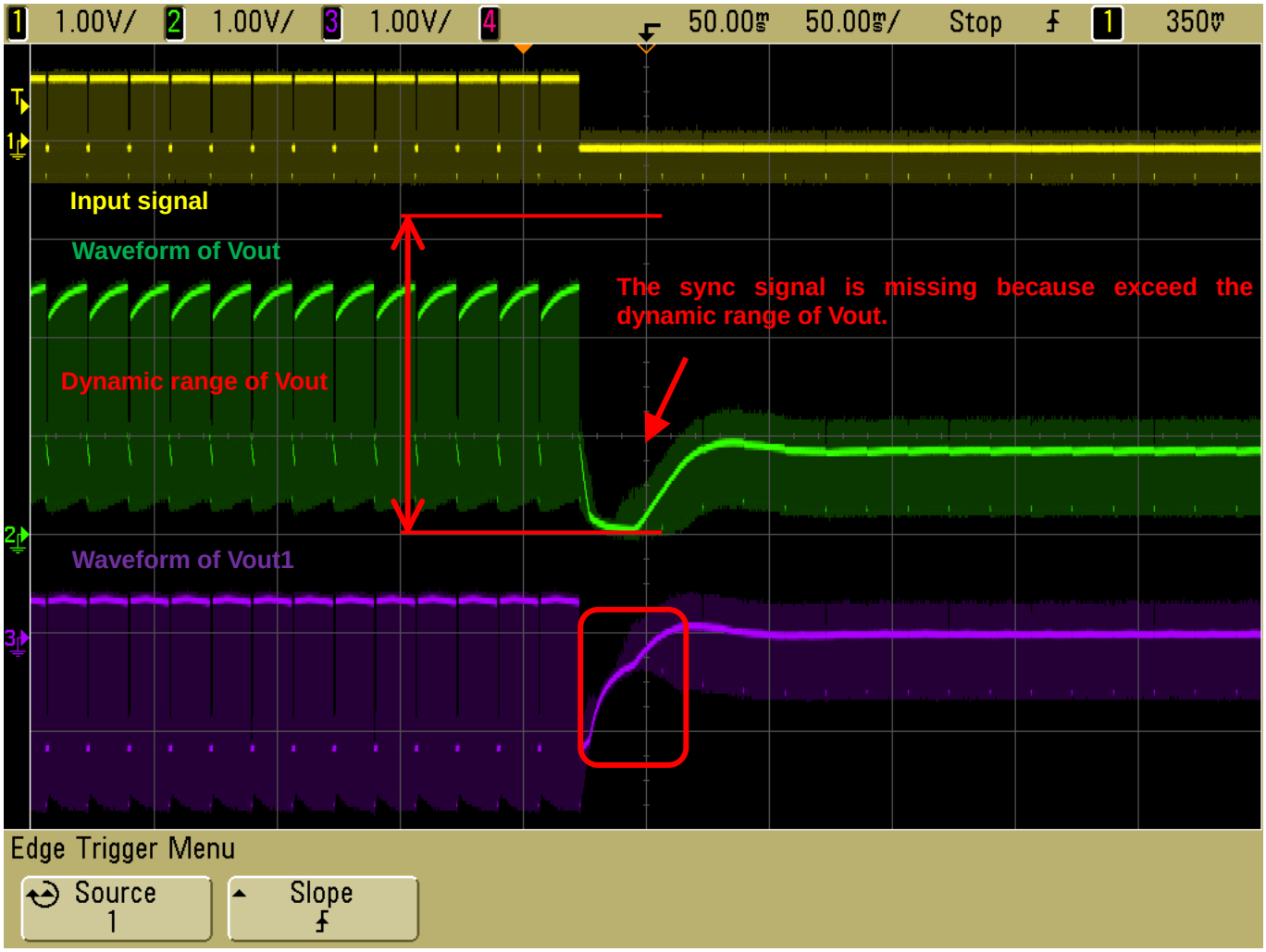


Waveform of Vout1



SAG correction circuit generates a low frequency component signal amplified to Vout terminal.
Changes of the luminance signal will be low-frequency components, if you want to output a large signal luminance changes. Therefore, generate correction signal of change of a luminance signal to Vout pin.
At this time, signal is over the dynamic range of Vout pin. This may cause a lack of sync signal, and waveform distortion.

Please see diagram below (green waveform), if you want to output large changes of a signal luminance, such as 100% white video signal and black signal. Thus, output signal exceed dynamic range of Vout pin and may be the signal lack.



< Countermeasure for waveform distortion >

1. Please using small value the Sag compensation capacitor (VSAG).

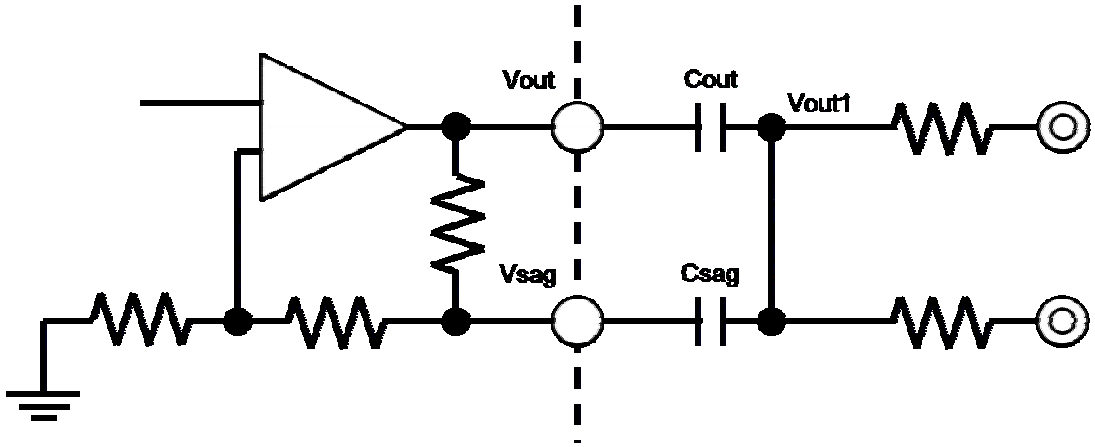
It can ensure the dynamic range by using small value the capacitor (VSAG). It because of low-frequency variation of Vout pin is smaller. However, the output (VOUT) must be use large capacitor for this reason sag characteristics become exacerbated.

2. Please do not use the sag correction circuit.

Signal can output within dynamic range for reason it does not change the DC level of the output terminal.
However, the output (VOUT) must be use large capacitor for this reason sag characteristics become exacerbated.

< Dual drive at using SAG correction circuit >

Using sag correction circuit at dual drive circuit is below. Dual drives are less load resistance. Thus, the cut-off frequency of HPF that is composed of the output capacitor and load resistance will be small. Therefore, the sag characteristics deteriorate.
Please size up to the output capacitor (Vout) for not to deteriorate the sag characteristics.

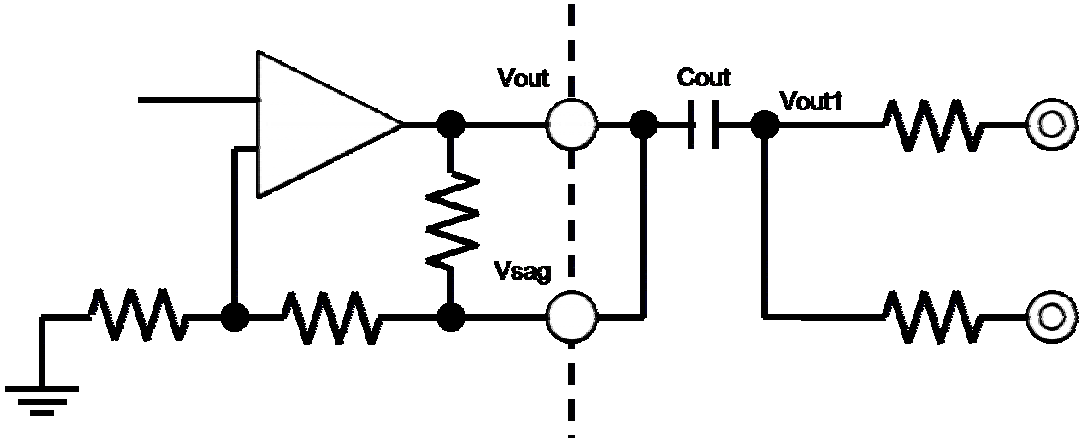


< Dual drive at not using SAG correction circuit >

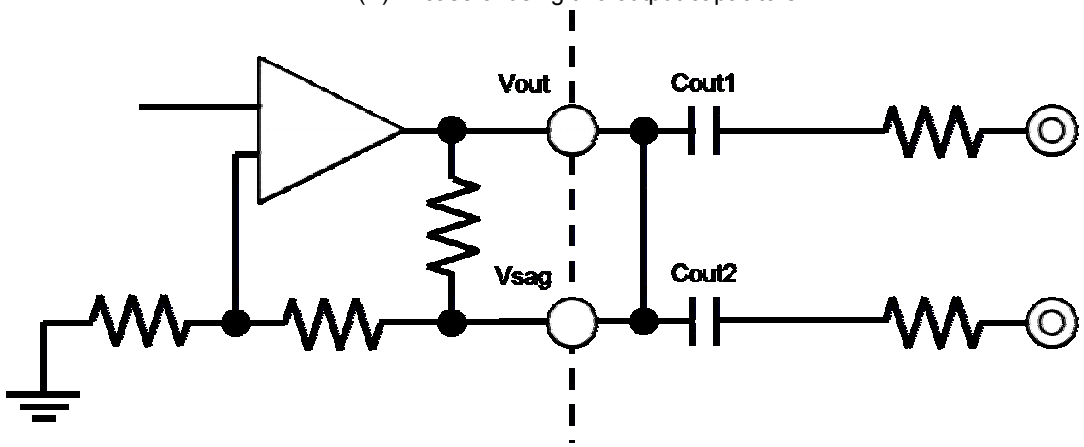
We recommended two-example dual drive circuit with not use sag correction circuit. Please change the configuration to be used according to the situation. Please configure to meet the following conditions. Then you can adjust the characteristics of each configuration.

$$Cout = Cout1 + Cout2$$
$$Cout1 = Cout2$$

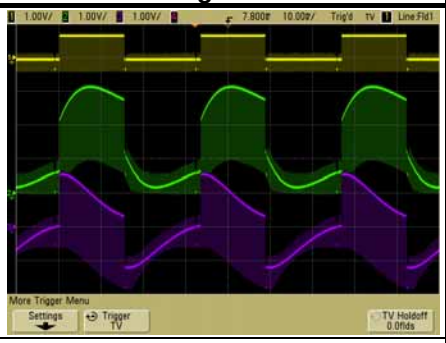
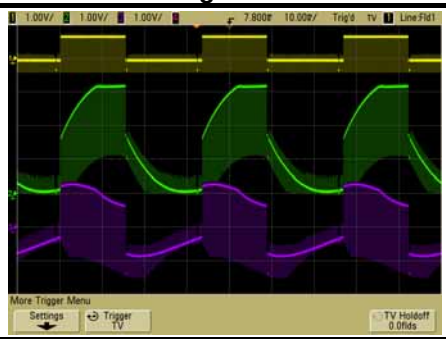
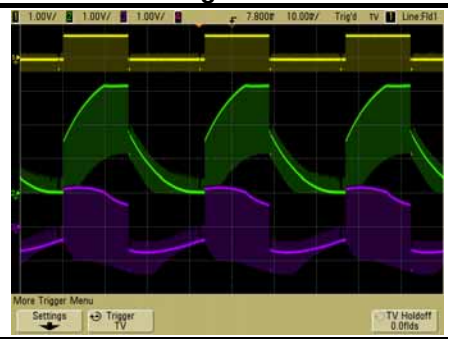
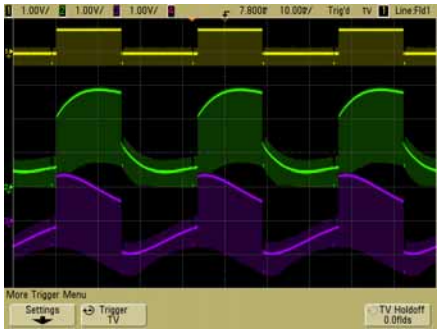
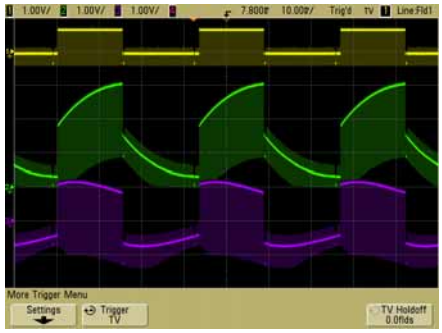
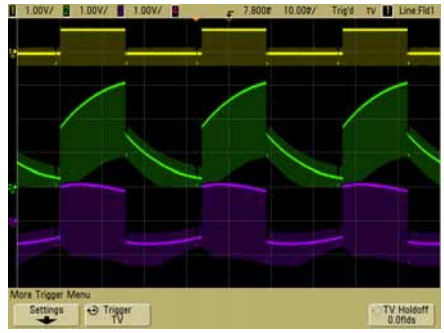
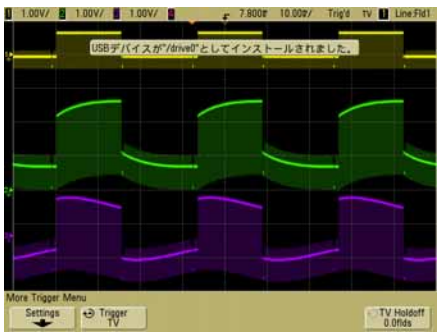
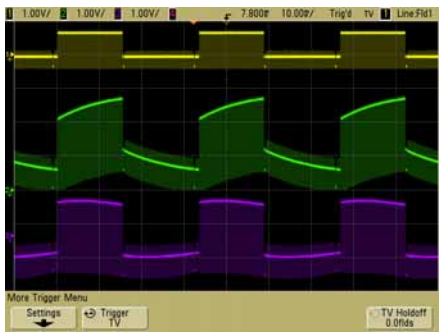
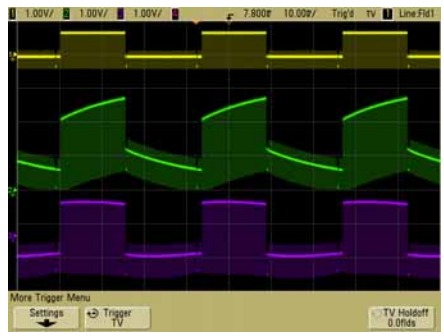
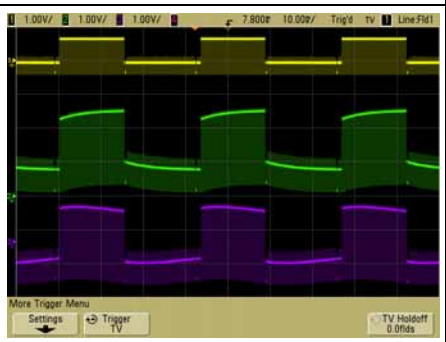
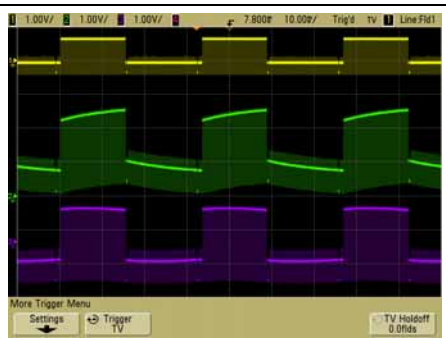
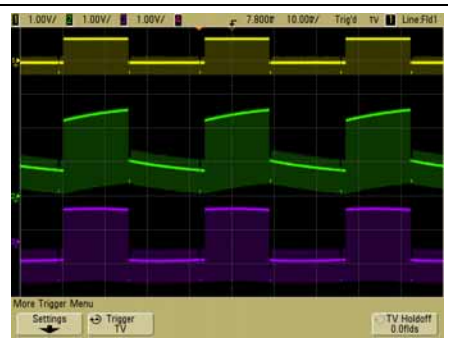
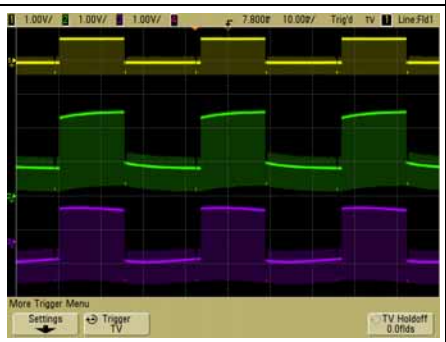
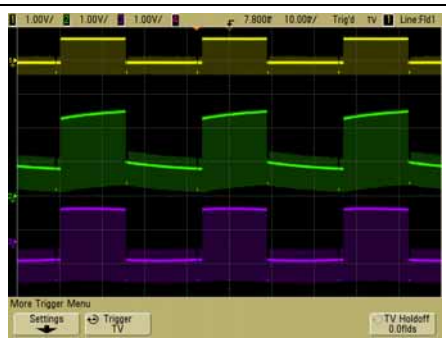
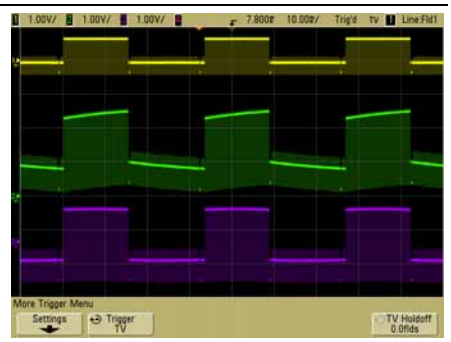
(A) In case of using one output capacitor



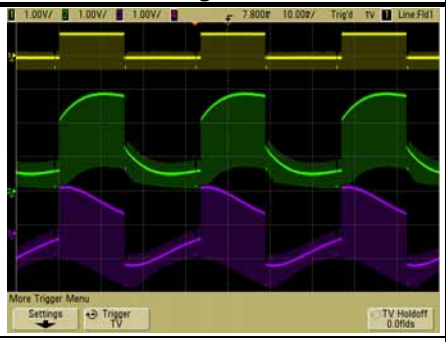
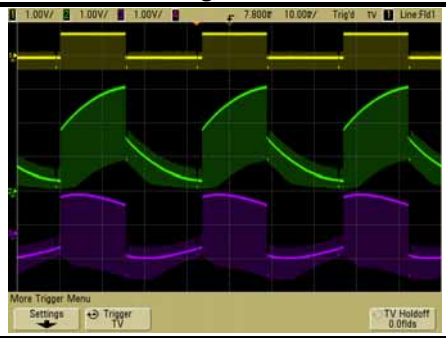
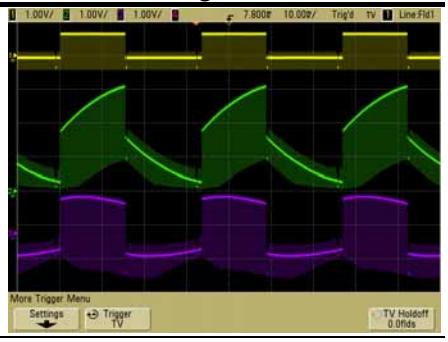
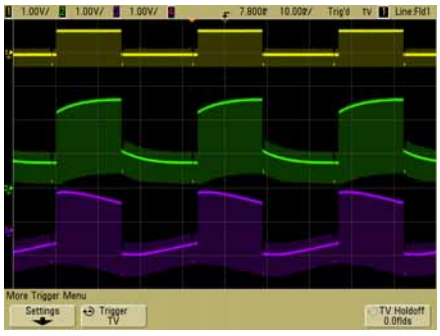
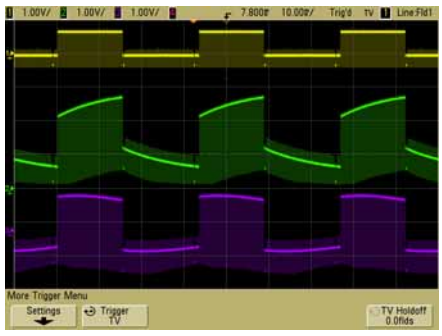
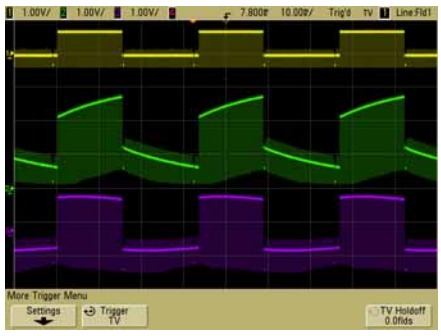
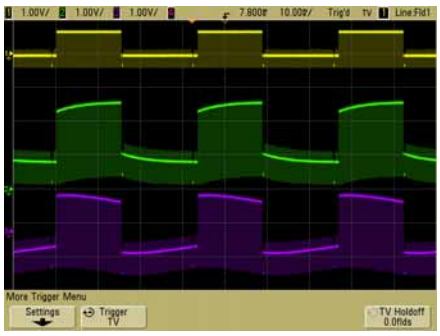
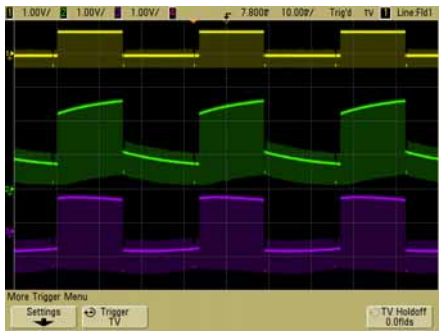
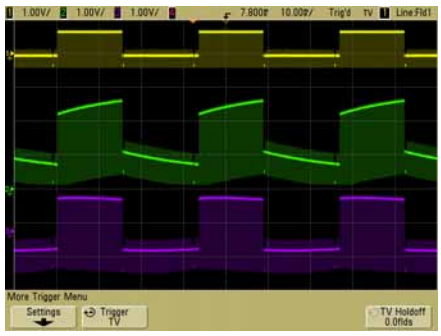
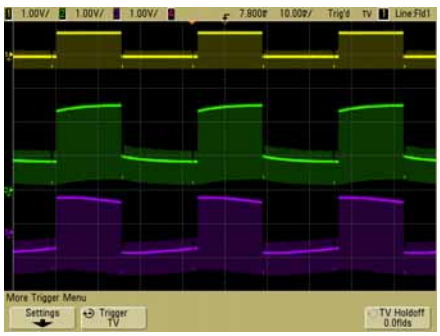
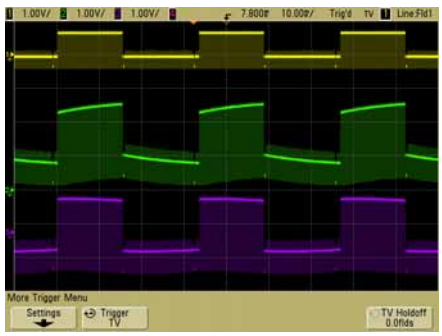
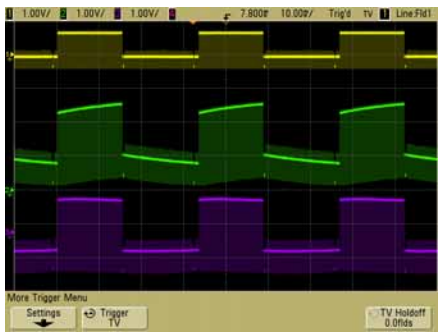
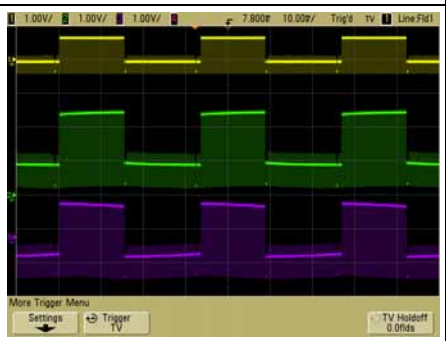
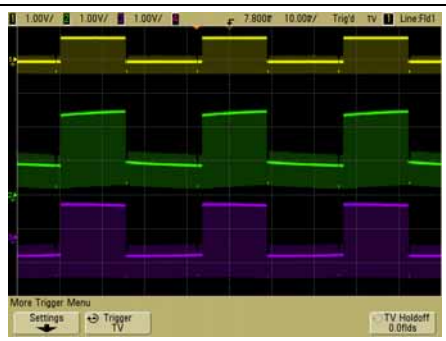
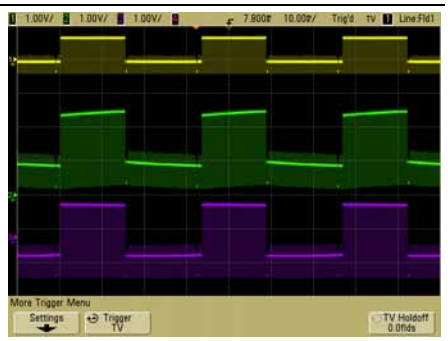
(B) In case of using two output capacitors



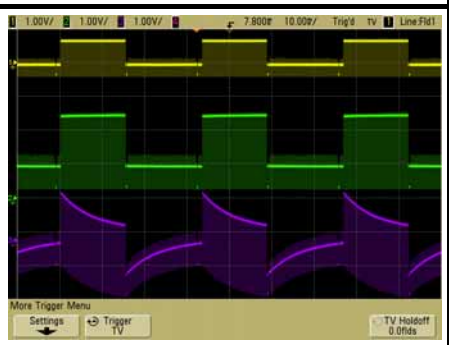
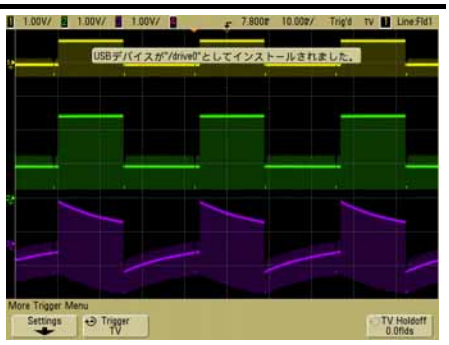
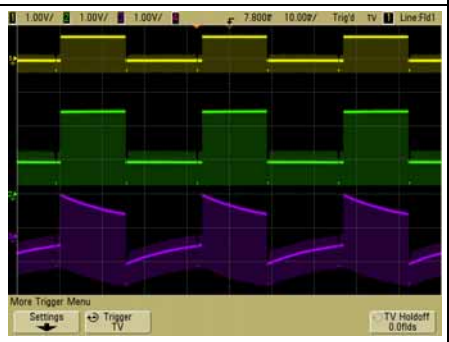
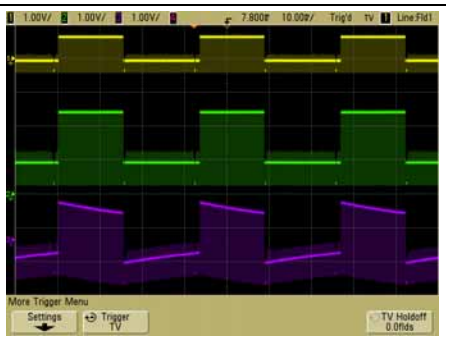
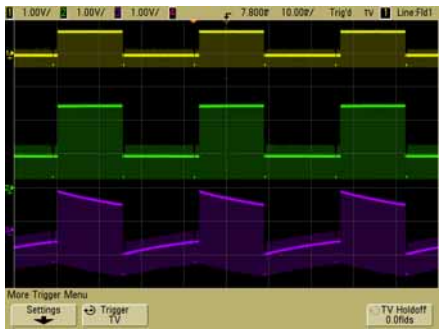
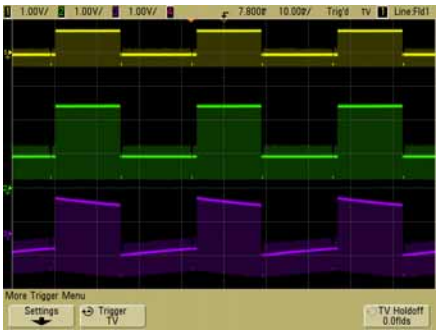
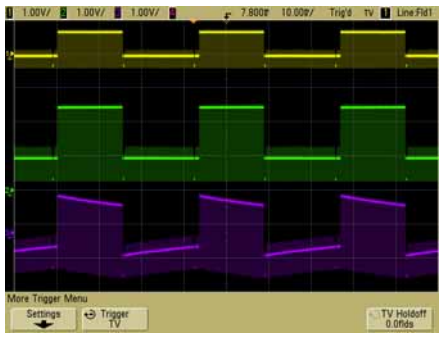
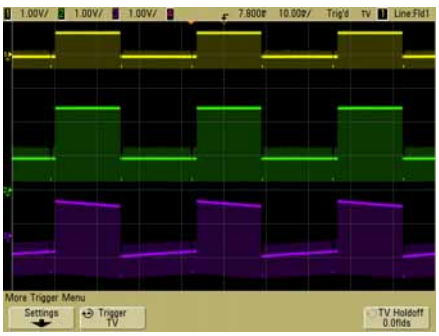
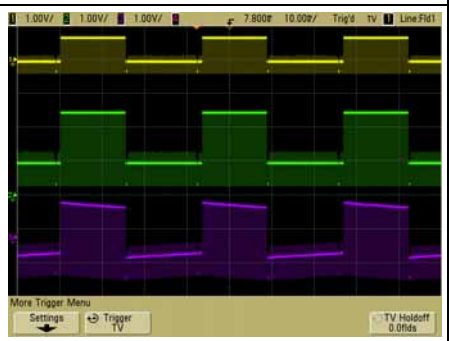
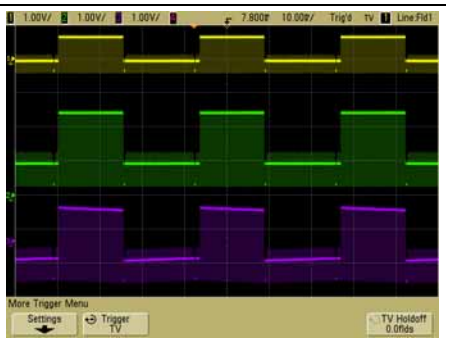
< Using SAG correction circuit >
Input signal: bounce signal (IRE0%, IRE100%, 30Hz), resistance=150Ω
Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal

	Csag=10uF	Csag=22uF	Csag=33uF
Cout=33uF			
Cout=47uF			
Cout=100uF			
Cout=220uF			
Cout=330uF			

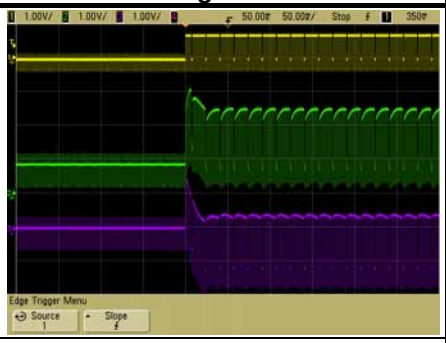
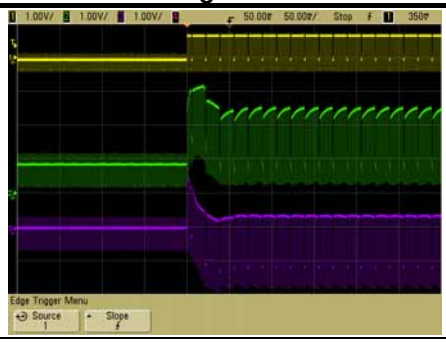
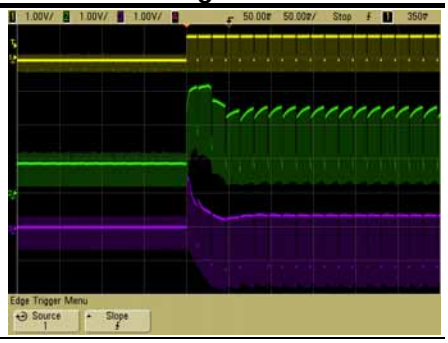
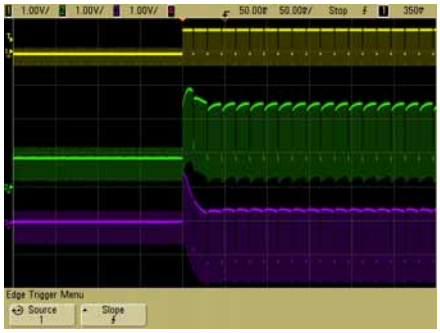
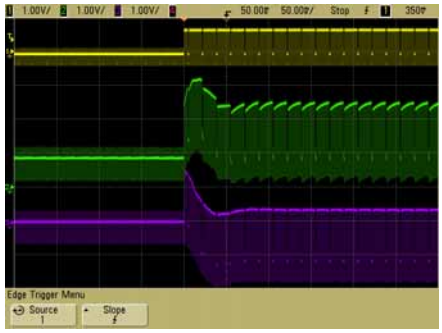
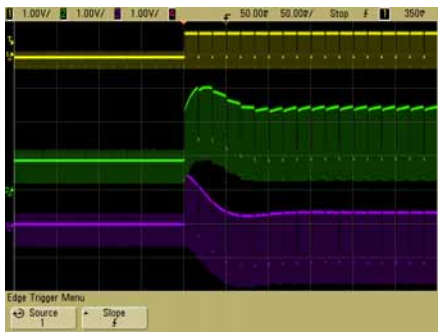
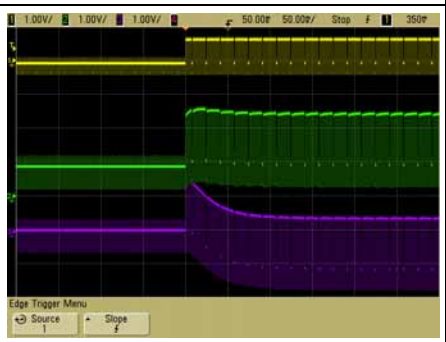
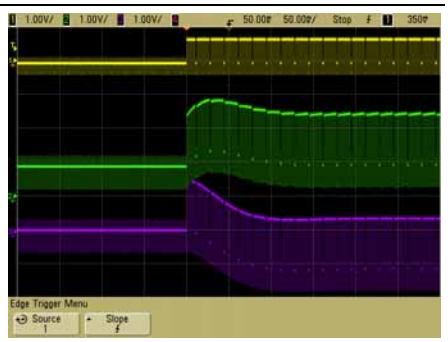
Input signal: bounce signal (IRE0%, IRE100%, 30Hz), resistance=75Ω
Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal

	Csag=10uF	Csag=22uF	Csag=33uF
Cout=100uF			
Cout=220uF			
Cout=330uF			
Cout=470uF			
Cout=1000uF			

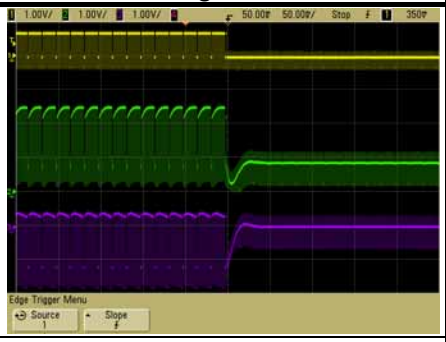
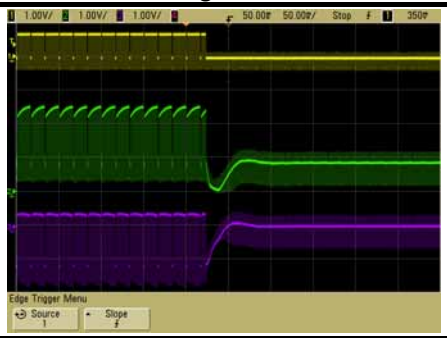
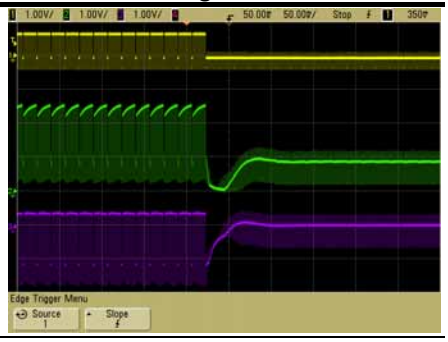
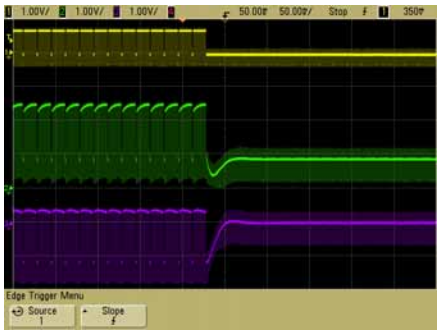
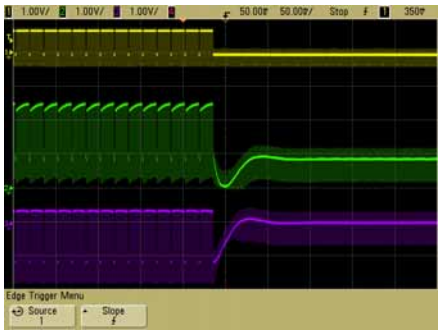
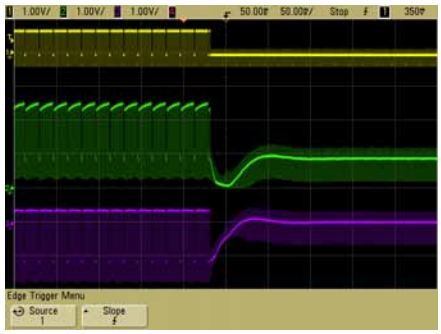
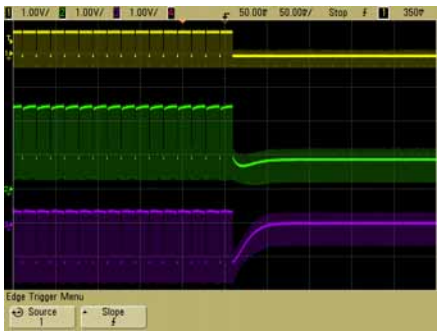
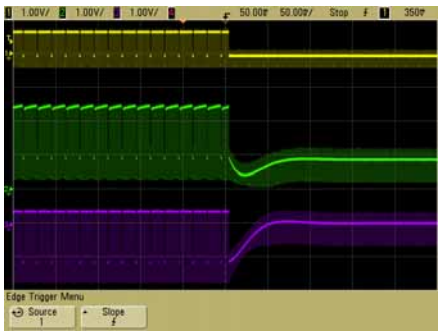
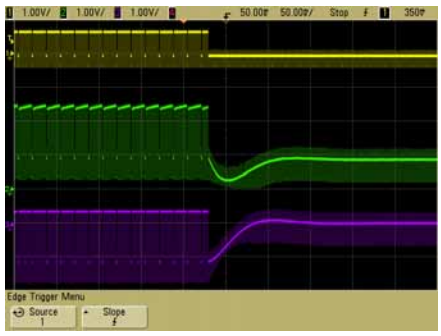
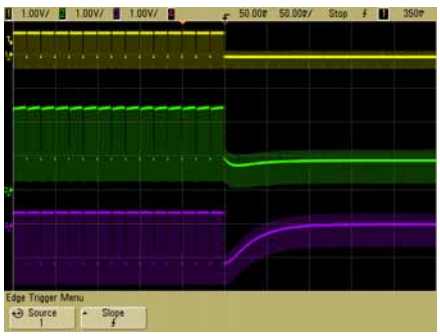
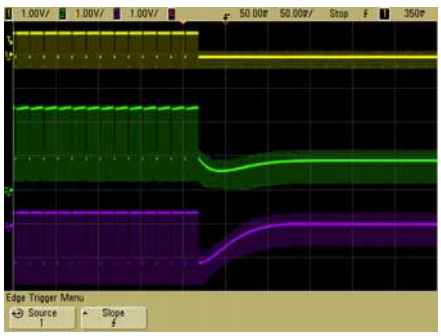
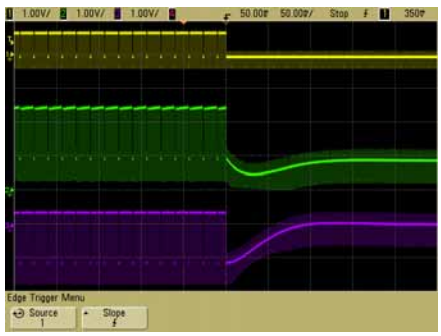
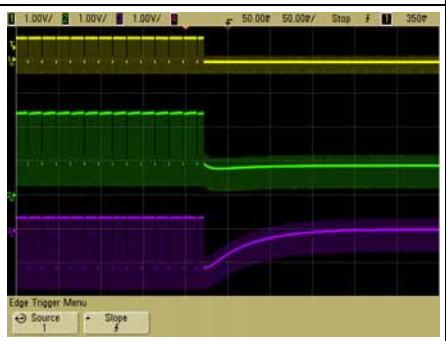
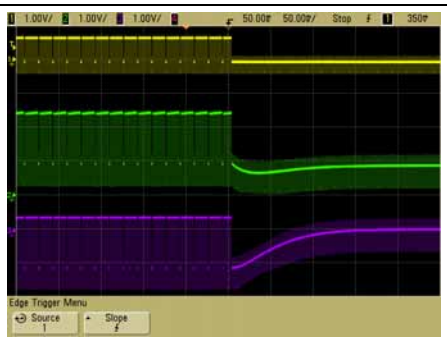
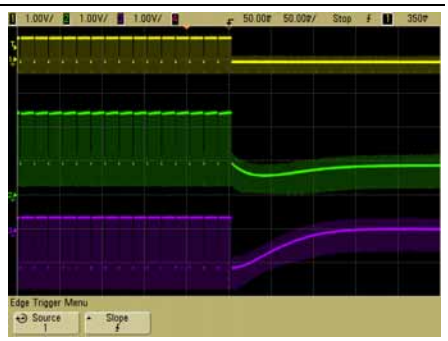
< Not using SAG correction circuit >
Input signal: bounce signal (IRE0%, IRE100%, 30Hz), resistance=150Ω
Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal

	RL=75Ω	RL=150Ω
Cout=100uF		
Cout=220uF		
Cout=330uF		
Cout=470uF		
Cout=1000uF		

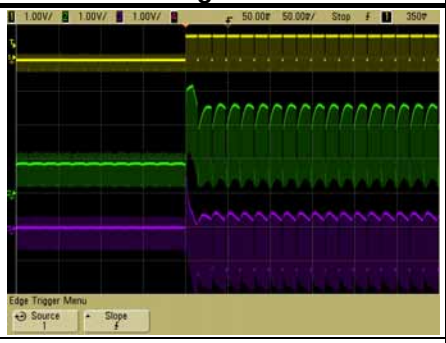
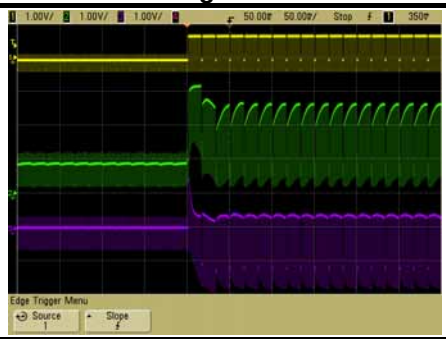
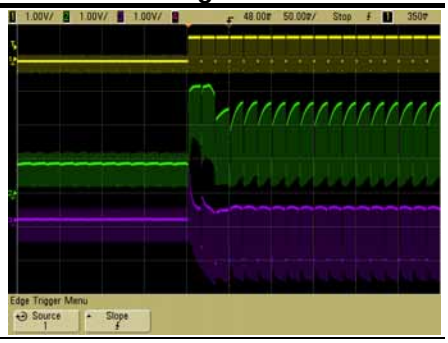
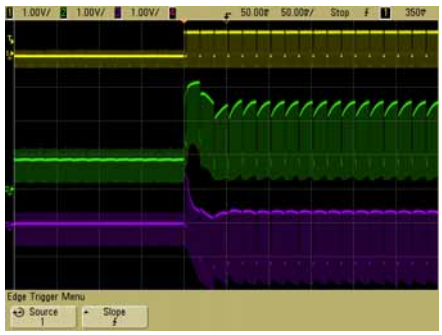
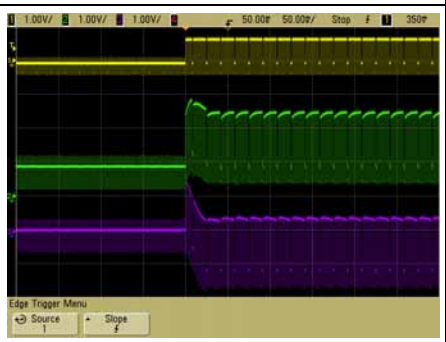
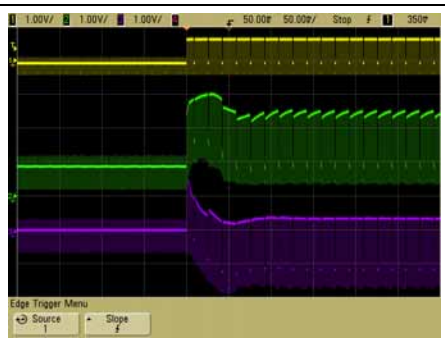
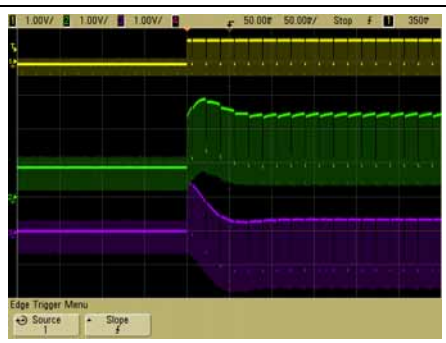
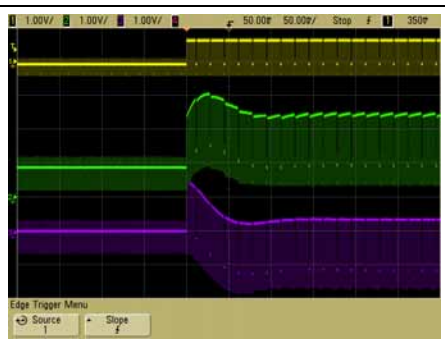
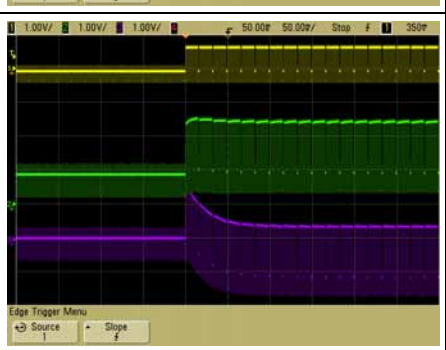
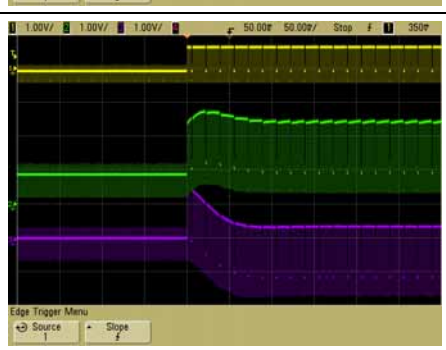
< Using SAG correction circuit >
Input signal: Black to White100%, resistance150Ω
Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal

	Csag=10uF	Csag=22uF	Csag=33uF
Cout=33uF			
Cout=47uF			
Cout=100uF			
Cout=220uF			
Cout=330uF			

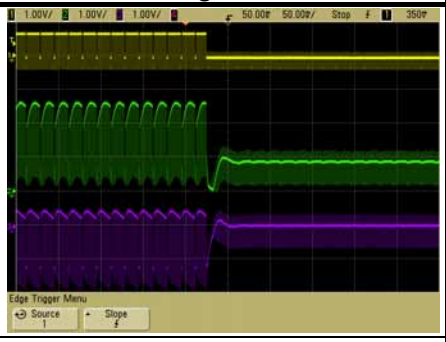
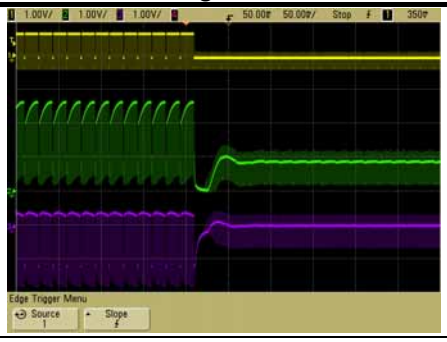
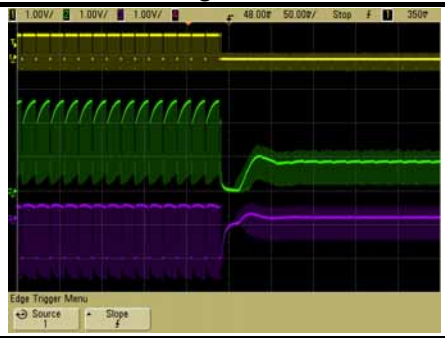
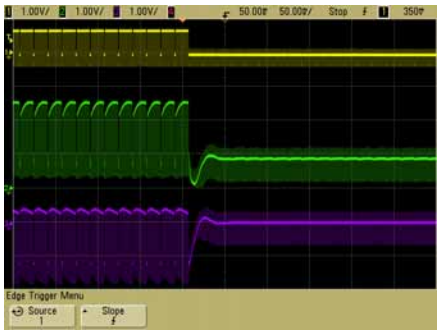
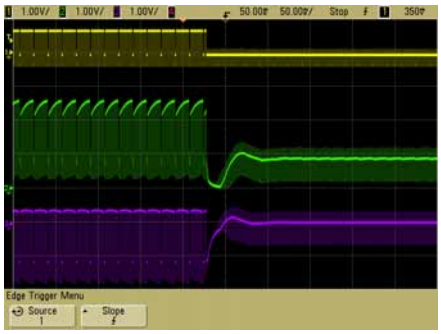
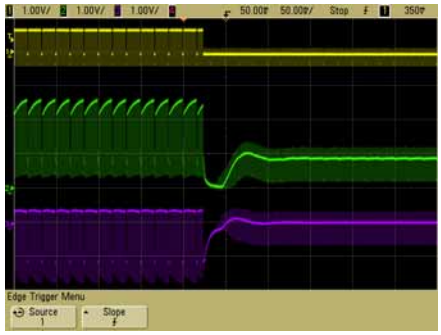
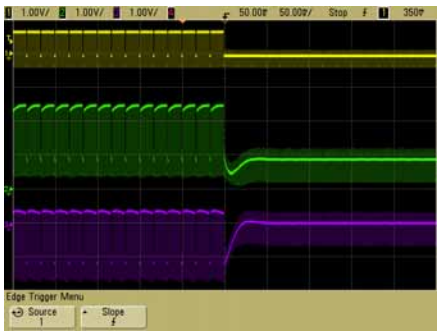
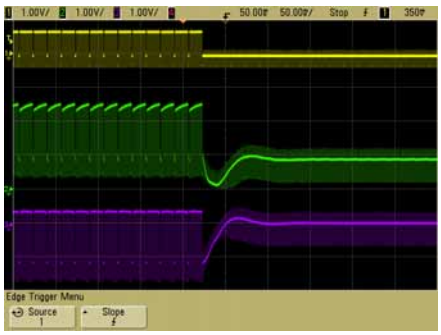
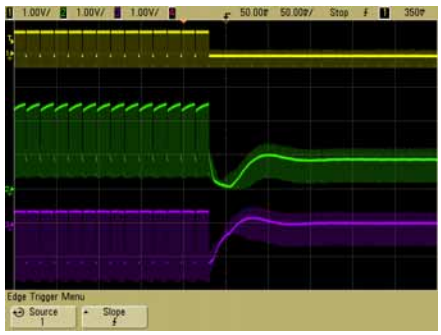
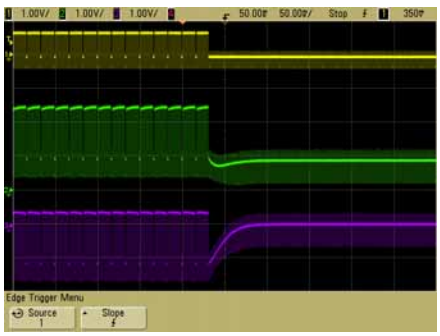
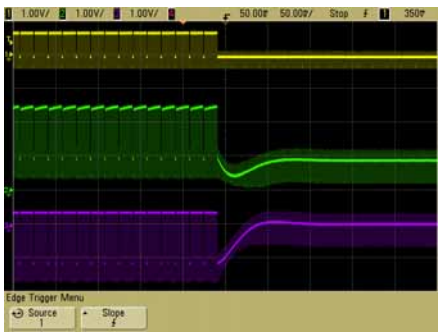
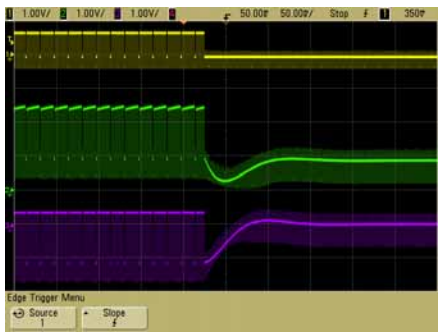
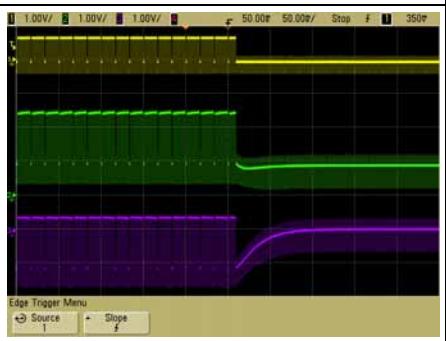
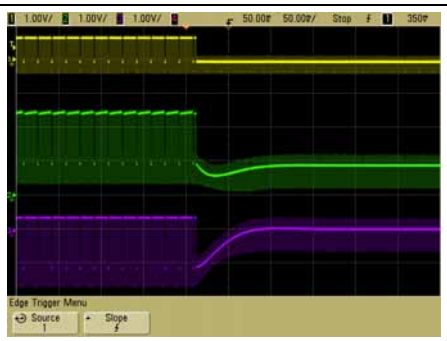
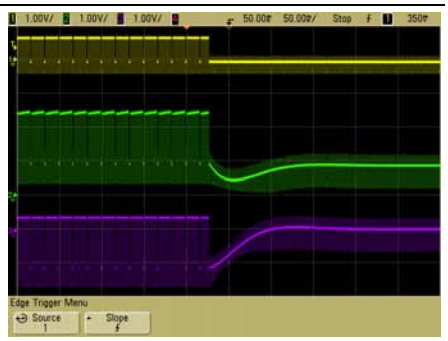
Input signal: White100% to Black, resistance150Ω
Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal

	Csag=10uF	Csag=22uF	Csag=33uF
Cout=33uF			
Cout=47uF			
Cout=100uF			
Cout=220uF			
Cout=330uF			

< Using SAG correction circuit >
Input signal: Black to White100%, resistance=75Ω
Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal

	Csag=10uF	Csag=22uF	Csag=33uF
Cout=33uF			
Cout=47uF			
Cout=100uF			
Cout=220uF			
Cout=330uF			

Input signal: White100% to Black, resistance=75Ω
Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal

	Csag=10uF	Csag=22uF	Csag=33uF
Cout=33uF			
Cout=47uF			
Cout=100uF			
Cout=220uF			
Cout=330uF			

♦**Clamp circuit**

1. Operation of Sync-tip-clamp

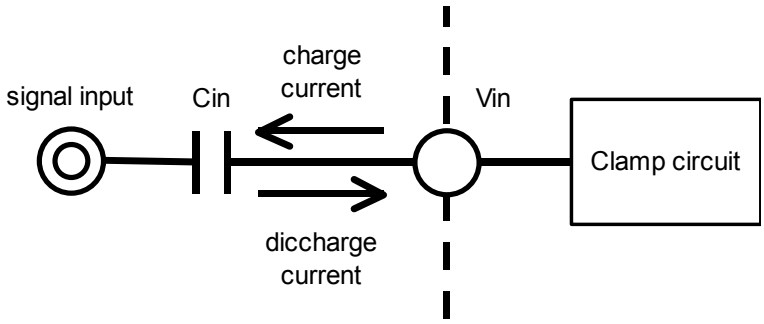
Input circuit will be explained. Sync-tip clamp circuit (below the clamp circuit) operates to keep a sync tip of the minimum potential of the video signal. Clamp circuit is a circuit of the capacitor charging and discharging of the external input Cin. It is charged to the capacitor to the external input Cin at sync tip of the video signal. Therefore, the potential of the sync tip is fixed.

And it is discharged charge by capacitor Cin at period other than the video signal sync tip. This is due to a small discharge current to the IC.

In this way, this clamp circuit is fixed sync tip of video signal to a constant potential from charging of Cin and discharging of Cin at every one horizontal period of the video signal.

The minute current be discharged an electrical charge from the input capacitor at the period other than the sync tip of video signals. Decrease of voltage on discharge is dependent on the size of the input capacitor Cin.

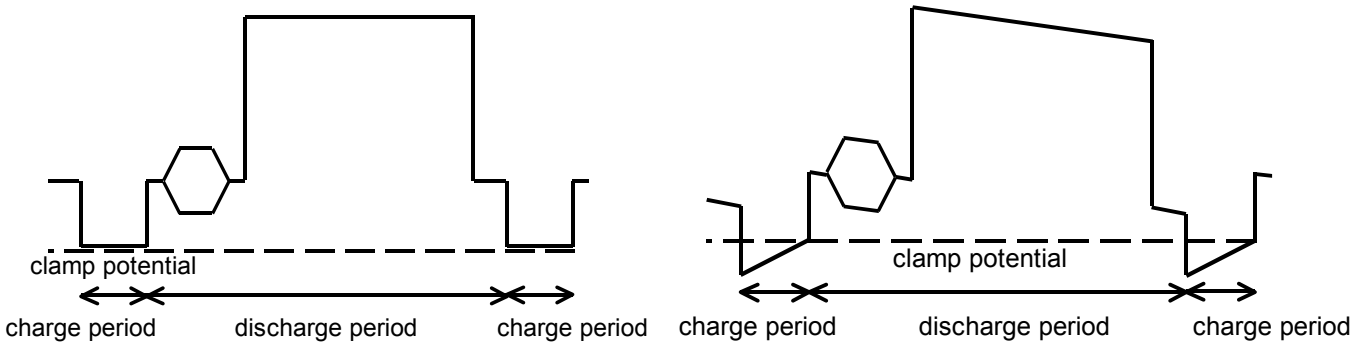
If you decrease the value of the input capacitor, will cause distortion, called the H sag. Therefore, the input capacitor recommend on more than 0.1uF.



< Clamp circuit >

A. Cin is large

B. Cin is small (H sag experience)



< Waveform of input terminal >

2. Input impedance

The input impedance of the clamp circuit is different at the capacitor discharge period and the charge period.

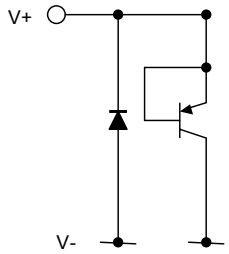
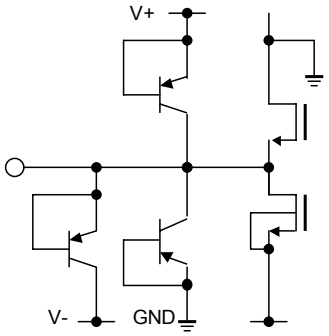
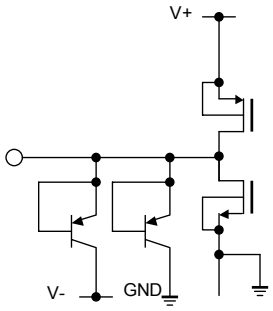
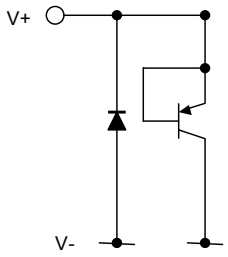
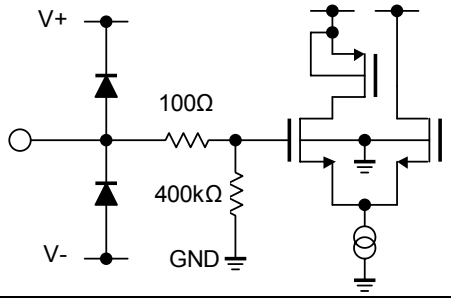
The input impedance of the charging period is a few kΩ. On the other hand, the input impedance of the discharge period is several MΩ. Because is a small discharge-current through to the IC.

Thus the input impedance will vary depending on the operating state of the clamp circuit.

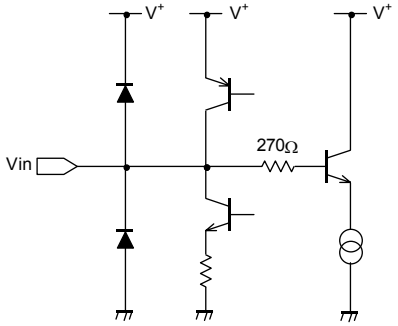
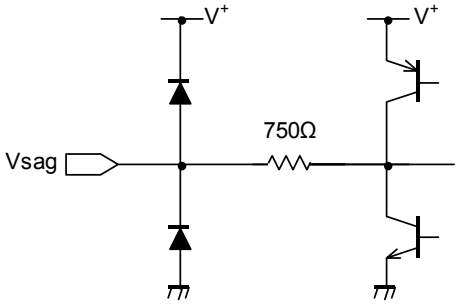
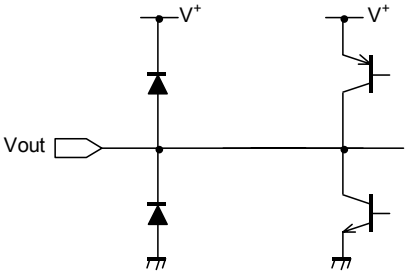
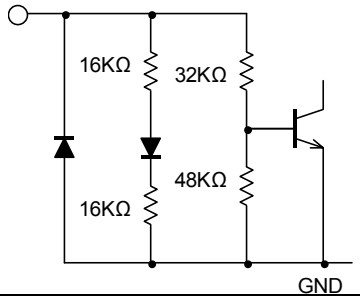
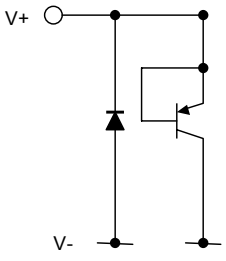
3. Impedance of signal source

Source impedance to the input terminal, please lower than 200Ω. A high source impedance, the signal may be distorted. If so, please to connect a buffer for impedance conversion.

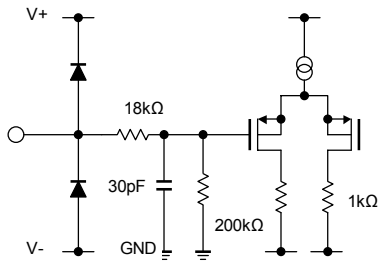
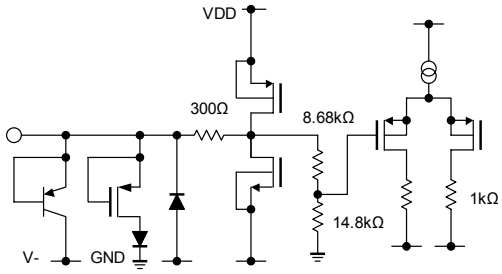
■TERMINAL DESCRIPTION

Terminal	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
1	V+1	V+ Power Supply for Audio		
2	CN	Flying Capacitor Negative Terminal for Audio		-
3	CP	Flying Capacitor Positive Terminal for Audio		-
4	V-	V- Power Supply for Audio		-[V+]
5	MUTE	Mute / Pop Noise Suppression for Audio		0V

■TERMINAL DESCRIPTION

Terminal	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
7	VIN	Video Input		1.10V
8	VS	SAG Correction		-
9	VOUT	Video Output		0.33V
10	PS	Power Save for Video		-
11	V+2	V+ Power Supply for Video		3V

■TERMINAL DESCRIPTION

Terminal	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
15 14	INL INR	Audio Input		0V
16 13	OUTL OUTR	Audio Output		0V