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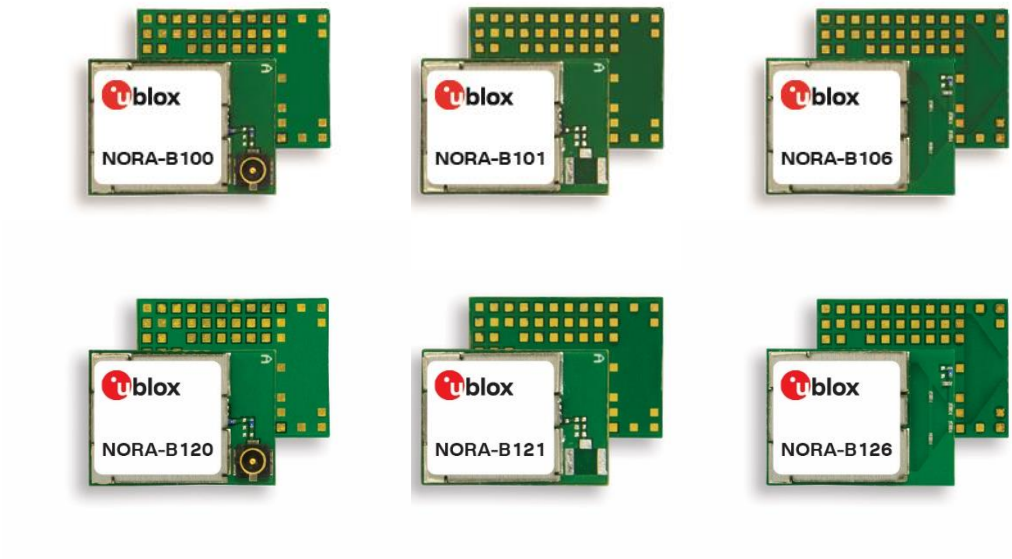
NORA-B1 series

Stand-alone dual-core Bluetooth® 5.2 Low Energy and IEEE 802.15.4 module

Data sheet



Abstract

This technical data sheet describes the NORA-B1 series stand-alone dual-core Bluetooth® Low Energy and IEEE 802.15.4 modules. OEMs can embed their own application in conjunction with the Zephyr real time operating system integrated into the Nordic Semiconductor nRF Connect SDK.

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Document information

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Product status	Corresponding content status	
Functional sample	Draft	For functional testing. Revised and supplementary data will be published later.
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Initial production	Early production information	Data from product verification. Revised and supplementary data may be published later.
Mass production/ End of life	Production information	Document contains the final product specification.

This document applies to the following products:

Product name	Type number	Firmware version	PCN reference	Product status
NORA-B100	NORA-B100-00B-00	N/A	N/A	Initial production
NORA-B101	NORA-B101-00B-00	N/A	N/A	Initial production
NORA-B106	NORA-B106-00B-00	N/A	N/A	Initial production
NORA-B120	NORA-B120-00B-00	N/A	N/A	Functional sample
NORA-B121	NORA-B121-00B-00	N/A	N/A	Functional sample
NORA-B126	NORA-B126-00B-00	N/A	N/A	Functional sample

Contents

1 Functional description

1.1 Overview

Based on the Nordic Semiconductor nRF5340 Bluetooth 5 system on chip (SoC), the NORA-B1 series of small stand-alone, dual-core modules includes Arm® Cortex®-M33 application and network processors. The application processor provides a floating-point unit (FPU), digital signal processor (DSP) instruction set, and CryptoCell™-312 security architecture while the network processor operates the radio.

NORA-B1 modules support multiple peripherals over high-speed SPI, QSPI, USB, ADC and PWM interfaces, and include a 2.4 GHz radio capable of handling Bluetooth Low Energy (LE), 802.15.4 for Thread, Zigbee, and Nordic Semiconductor proprietary protocols. The modules operate in ambient temperatures of up to 105 °C.

Direction finding (AoA/AoD) and Bluetooth LE Audio features are all supported by the hardware. The modules support multiple power supply configurations and offer multiple antenna choices, including U.FL connector, antenna pin, and on-board PCB trace antenna options.

For more information about the antennas that are approved for use with NORA-B1 series, see also the system integration manual [1].

1.2 Applications

NORA-B1 series modules provide scalable solutions for a broad range of market segments, including smart cities and buildings, industrial automation, telematics, medical and healthcare.

Specific application areas include:

- Industrial automation
- Advanced wearables
- Smart buildings and cities
- Low power sensors
- Wireless-connected and configurable equipment
- Point-of-sale
- Medical and health devices
- Real-time Location, RTLS
- Indoor positioning
- Asset tracking

1.3 Block diagram

Figure 1 shows the integration of the nRF5340 and other logical components in NORA-B10 modules.

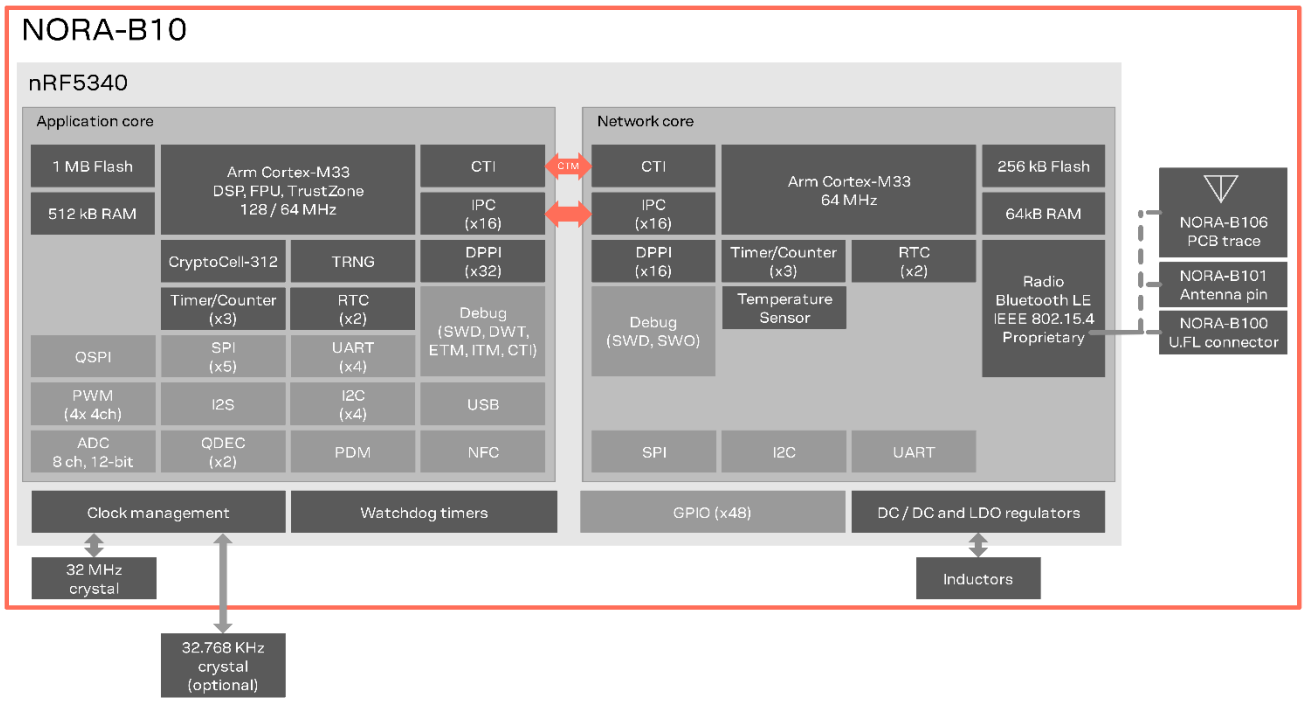


Figure 1: NORA-B10 series block diagram

Figure 2 shows the integration of the nRF5340, FEM, and other logical components in NORA-B12 modules.

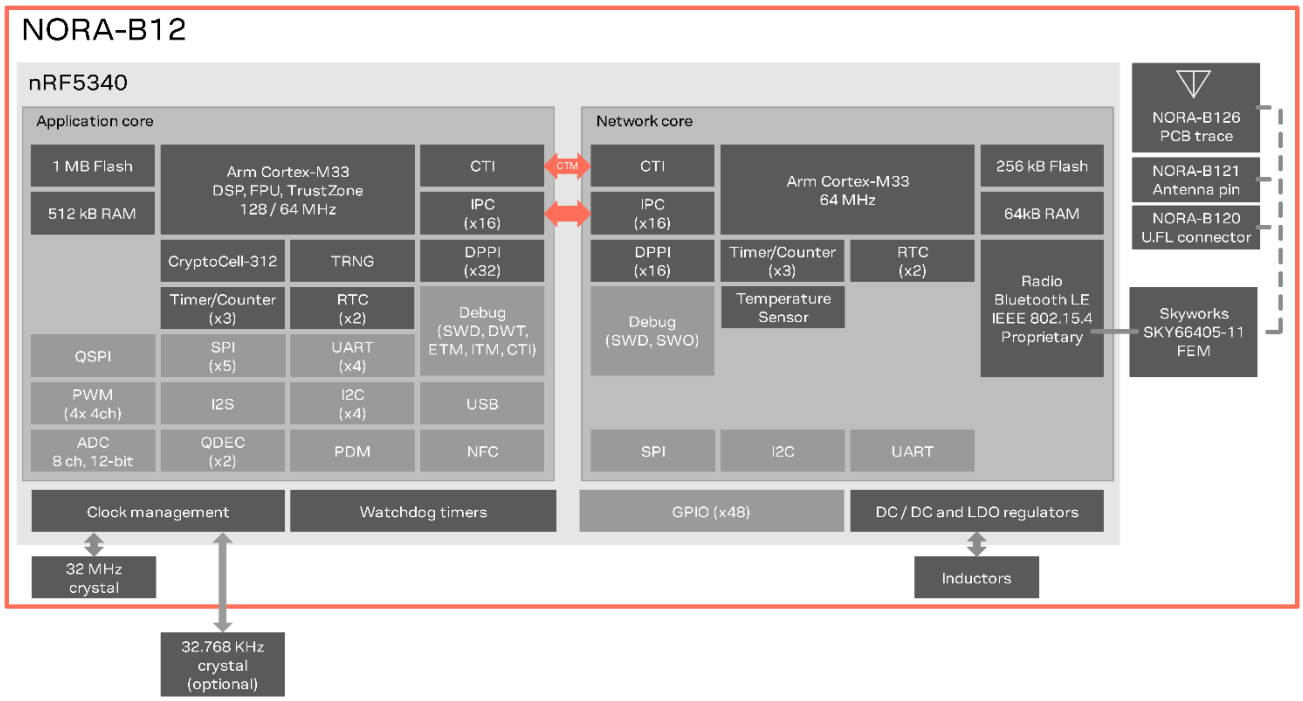


Figure 2: NORA-B12 series block diagram

1.4 Product description

Item	NORA-B100	NORA-B101	NORA-B106	NORA-B120	NORA-B121	NORA-B126
CPU	Nordic Semiconductor nRF5340					
Skyworks 66405-11 FEM	No	No	No	Yes	Yes	Yes
Operating temperature	–40 to +105 °C					
Operating voltage	+1.7 to +5.5 VDC	+1.7 to +5.5 VDC	+1.7 to +5.5 VDC	+1.7 to +3.6 VDC	+1.7 to +3.6 VDC	+1.7 to +3.6 VDC
GPIO	48 pins					
Application core	Arm Cortex-M33 with TrustZone technology					
Operating speed	128 MHz or 64 MHz					
Floating point unit (FPU)	Single precision with DSP instructions					
Debug	Data Watchpoint and Trace (DWT) Embedded Trace Microcells (ETM) Instrumentation Trace Macrocell (ITM) Cross trigger interface (CTI) Serial wire debug (SWD)					
Memory	1 MB flash 512 kB low leakage RAM					
Security	Arm TrustZone CryptoCell-312 NIST 800-90B, AIS-31, and FIPS 140-2 compliant random number generator AES-128 and 256: ECB, CBC, CMAC/CBC-MAC, CTR, CCM/CCM*, GCM SHA-1, SHA-2 up to 256 bits Keyed-hash message authentication code (HMAC) RSA public key cryptography with up to 3072-bit key size ECC support for most used curves Application key management using derived key model					
Peripherals (not all simultaneous)	QSPI (with XIP) SPI: up to 5 master or slave instances with EasyDMA I2C (TWI): up to 4 master or slave instances with EasyDMA UART: up to 4 instances with RTS/CTS flow control and EasyDMA I2S: 1 instance NFC tag: 1 instance PDM: 1 instance PWM: up to 4 instances, 4 channel each Timer/counter: up to 3 instances, 32-bit RTC, up to 2 instances, 24-bit QDEC: 1 instance DPPI: up to 32 channels IPC: up to 16 channels MUTEX: up to 16 instances					
Network core	Arm Cortex-M33					
Operating speed	64 MHz					
Debug	CTI, SWD, SWO					
Memory	256 kB flash 64 kB low leakage RAM					
Security	128-bit AES/ECB/CCM/AAR co-processor (on-the-fly packet encryption)					
Peripherals	SPI: one master or slave instance with EasyDMA I2C (TWI): one master or slave instance with EasyDMA UART: one instance with EasyDMA Timer/counter: up to 3 instances, 32-bit RTC, up to 2 instances, 24-bit Temperature sensor: 1 instance DPPI: up to 32 channels					

Item	NORA-B100	NORA-B101	NORA-B106	NORA-B120	NORA-B121	NORA-B126
	IPC: up to 16 channels MUTEX: up to 16 instances					
Radio						
Supported 2.4 GHz radio modes	Bluetooth LE, v5.2 IEEE 802.15.4 Proprietary modes					
Band support	2.4 GHz, 40 channels					
Typical conducted output power	+3.0 dBm	+3.0 dBm	+3.0 dBm	+13 dBm	+13 dBm	+13 dBm
Radiated output power (EIRP with approved antennas)	+8.3 dBm	+8.3 dBm	+5 dBm	+18 dBm	+18 dBm	+15 dBm
RX sensitivity LE 1M (Bluetooth LE, conducted) LE 2M	–98 dBm –95 dBm	–98 dBm –95 dBm	–98 dBm –95 dBm	–103 dBm –99 dBm	–103 dBm –99 dBm	–103 dBm –99 dBm
Antenna type	U.FL connector	Pin	PCB trace	U.FL connector	Pin	PCB trace
Bluetooth						
Supported Bluetooth LE modes	LE 1M PHY (1 Mbps) LE 2M PHY (2 Mbps) LE Coded PHY S=2 (500 kbps) LE Coded PHY S=8 (125 kbps)					
IEEE 802.15.4						
Thread Stack	OpenThread, Thread 1.1					
Thread security	AES-128, co-processor accelerated					
Zigbee stack	Zigbee compliant platform					
Other	1 Mbps, 2 Mbps Nordic-proprietary					
Dimensions	14.3 x 10.4 x 1.7 mm					
Weight	0.55 g	0.53 g	0.53 g	TBD	TBD	TBD

Table 1: NORA-B1 series characteristics summary

1.5 Hardware options

NORA-B10 and NORA-B12 modules are based on the Nordic Semiconductor nRF5340 SoC.

Designed for use with an external antenna, NORA-B12 modules additionally include a Skyworks SKY66405-11 front-end module (FEM) [9] with an integrated power amplifier (PA) in the transmitter and low noise amplifier (LNA) in the receiver. Both NORA-B10 and NORA-B12 module variants are equipped with either a U.FL connector, antenna pad, or PCB antenna. See also RF antenna interfaces.

Aside from the antenna interface type and FEM, NORA-B1 modules have identical hardware configurations. All module interfaces or functions must be allocated to a GPIO signal and two of these are dedicated to FEM control in NORA-B12. See also GPIO.

The integrated DC-DC converter facilitates higher efficiency under heavy load situations. See also Power management.

For more information about the antennas approved for use with NORA-B1 series, see also the system integration manual [1]

1.6 Software options

1.6.1 Open CPU

The open-CPU architecture of NORA-B1 series modules allows integrators to develop and run their own applications on the built-in Arm® Cortex®-M33 cores. u-blox recommends the Nordic Semiconductor nRF Connect SDK [5] for development.

The nRF Connect SDK integrates the Zephyr Real Time Operating System (RTOS), MCUboot secure bootloader, and Nordic Semiconductor's nrfxlib device drivers for the nRF52 and nRF53 peripherals.

1.7 Bluetooth device address

NORA-B1 modules are programmed from the factory with a unique, public Bluetooth device address stored in the OTP[0] and OTP[1] registers of the User Information Configuration Registers (UICR) of the application core and duplicated in the CUSTOMER[0] and CUSTOMER[1] registers of the User Information Configuration Registers (UICR) of the network core.

The Bluetooth device address consists of the IEEE Organizationally Unique Identifier (OUI) combined with the hexadecimal digits that are printed within a 2D data matrix. See also Labeling and ordering information. The Bluetooth device address is stored in little-endian format. The two most significant bytes of the OTP[1] and CUSTOMER[1] registers are unused and assigned the value 0xFF to complete the 32-bit register.

UICR Register in application core	Address	Description	Remarks
OTP[0]	0x00FF8100	0xAA = Bluetooth_addr [5]	IEEE OUI[1]
OTP[0]	0x00FF8101	0xBB = Bluetooth_addr [4]	IEEE OUI[1]
OTP[0]	0x00FF8102	0xCC = Bluetooth_addr [3]	IEEE OUI[1]
OTP[0]	0x00FF8103	0xDD = Bluetooth_addr [2]	Example - actual value printed on label
OTP[1]	0x00FF8104	0xEE = Bluetooth_addr [1]	Example - actual value printed on label
OTP[1]	0x00FF8105	0xFF = Bluetooth_addr [0]	Example - actual value printed on label
OTP[1]	0x00FF8106	0xFF	Unused
OTP[1]	0x00FF8107	0xFF	Unused

Table 2: Bluetooth device address in application core

UICR Register in network core	Address	Description	Remarks
CUSTOMER[0]	0x01FF8300	0xAA = Bluetooth_addr [5]	IEEE OUI[1]
CUSTOMER[0]	0x01FF8301	0xBB = Bluetooth_addr [4]	IEEE OUI[1]
CUSTOMER[0]	0x01FF8302	0xCC = Bluetooth_addr [3]	IEEE OUI[1]
CUSTOMER[0]	0x01FF8303	0xDD = Bluetooth_addr [2]	Example - actual value printed on label
CUSTOMER[1]	0x01FF8304	0xEE = Bluetooth_addr [1]	Example - actual value printed on label
CUSTOMER[1]	0x01FF8305	0xFF = Bluetooth_addr [0]	Example - actual value printed on label
CUSTOMER[1]	0x01FF8306	0xFF	Unused
CUSTOMER[1]	0x01FF8307	0xFF	Unused

Table 3: Bluetooth device address in network core

☞ For instructions describing how to read and re-program the Bluetooth device address if the UICR of either the application or network core need erased, see the NORA-B1 system integration manual [1].

[1] Example value shown. The IEEE OUI values for u-blox is one of the following: D4:CA:6E, CC:F9:57, 60:09:C3, or 6C:1D:EB

2 Interfaces

NORA-B1 provides all GPIO and interfaces available on the nRF5340 embedded within the module. For more information regarding function and use, see also the nRF5340 product specification [4].

2.1 Power management

NORA-B1 series modules utilize integrated step-down converters to transform the supply voltage presented at the **VDD** and **VDDH** pins into a stable system voltage. This makes NORA-B1 modules compatible for use in battery-powered designs without the use of an additional voltage converter. NORA-B12 modules internally connect **VDD** and **VDDH**.

2.1.1 DC-DC converters

All components to operate the DC-DC converters are included in NORA-B1 series modules. After the DC-DC converters are enabled, the module automatically switches between the LDO and DC-DC converters – depending on the current consumption of the module. Under high loads, when the radio is active for example, the DC-DC converter is more efficient. In the power saving modes, the LDO converter is more efficient.

2.1.2 High voltage and battery operation

NORA-B10 can be powered by a single power supply of 2.5 VDC to 5.5 VDC, applied to **VDDH**. This allows direct operation with Lithium-ion rechargeable batteries and makes powering directly from a USB host possible. When **VDDH** is used as the power supply, **VDD** becomes an output and is used as the reference voltage for the I/O pins. **VDD** can supply up to 1 mA in LDO mode during System OFF, and up to 7 mA when both radio and main regulators are in DC-DC mode. The **VDD** output voltage is configured through the VREGHVOUT register in the application core UICR. See also reference [6].

High voltage operation is not available for NORA-B12.

2.1.3 Normal voltage operation

If high voltage operation is not required, a single power supply of 1.7 VDC to 3.6 VDC can be applied to both **VDD** and **VDDH**. The high voltage regulator is bypassed and **VDD** is an input for the main power supply.

NORA-B12 is only capable of normal voltage operation.

2.1.4 Digital I/O interfaces reference voltage

The **VDD** power source is the reference voltage for the I/O signals.

2.2 System clocks

2.2.1 High-frequency clock

A single 32 MHz high-frequency crystal oscillator (HFXO) circuit is provided within NORA-B1 to generate the high frequency clock source (HFCLK). The HFCLK is used to derive the internal clock frequencies required to operate NORA-B1, including core clocks for the application core (128 MHz or 64 MHz) and the network core (64 MHz). The HFXO has an accuracy of ±30 ppm when considering frequency tolerance, temperature drift, and aging.

☞ XOSC32MCAPS.CAPVALUE register in the UICR should be calculated using 20 pF as the value for CAPACITANCE. See also reference [8].

2.2.2 Low-frequency clock

A 32.768 kHz low-frequency clock is used by NORA-B1 for various functions, including the timing of radio events, the real-time counter (RTC), and watchdog timer (WDT). One of four sources is required for the low-frequency clock. Choice of the LFCLK source depends on the accuracy required by the application. See references [7] and [8]:

- RC oscillator (LFRC) – fully embedded in NORA-B1, does not require external components, and provides ±250 ppm accuracy.
- Crystal oscillator (LFXO) – requires the addition of an external 32.768 kHz crystal and optional loading capacitors. Internal loading capacitors of 6 pF, 7 pF, and 9 pF are available and configured through the UICR register XOSC32KI.INTCAP. Accuracy is dependent on the selected crystal.
- External source – an externally generated 32.768 kHz clock source applied to **P0.00/XL1**. **P0.01/XL2** is either grounded or left open depending on the clock voltage level. Accuracy is dependent on the external source.
- Synthesized clock (LFSYNT) – 32.768 kHz clock generated from and assumes the accuracy of the HFCLK, ±30 ppm. LFSYNT requires HFCLK to run resulting in a higher average power consumption.

2.3 RF antenna interfaces

2.3.1 2.4 GHz radio (ANT)

NORA-B1 model versions support different 2.4 GHz antenna solutions:

- NORA-B100 and NORA-B120 modules use a U.FL connector solution for an external antenna with a nominal characteristic impedance of 50 Ω. The **ANT** pin is internally disconnected on this model.
- NORA-B101 and NORA-B121 modules include an antenna pin (**ANT**). The pin has nominal characteristic impedance of 50 Ω and can be connected to an antenna or connector on the host board using a controlled impedance trace.
- NORA-B106 and NORA-B126 modules are equipped with an internal antenna that is integrated into the module PCB. This low-profile antenna solution uses antenna technology licensed from Proant AB and is particularly useful in space constrained designs. The **ANT** pin is internally disconnected on this model.

For more information about the antennas that are approved for use with NORA-B1 series, see also the system integration manual [1]

2.3.2 Near Field Communication (NFC)

NORA-B1 series modules include an NFC interface, capable of operating as a 13.56 MHz NFC tag at a bit rate of 106 kbps. As an NFC tag, data can be read from or written to the NORA-B1 modules using an NFC reader; however, NORA-B1 modules are not capable of reading other tags or initiating NFC communications. The NFC interface can be used to wake the module from System OFF mode, meaning that the module can wake from the deepest power save mode and still react properly to an NFC field.

Two GPIO pins are available for connecting to an external NFC antenna: **P0.02/NFC1** and **P0.03/NFC2**.

2.3.3 Location services (AoA/AoD)

NORA-B1 series supports Bluetooth Direction Finding which is part of the Bluetooth 5.2 specification. It can be used to for example track assets, for indoor positioning and wayfinding. These phase-based functions require antenna arrays, estimation algorithms and processing power to make it possible to triangulate and detect the direction of a Bluetooth signal down to a sub-meter accuracy. Direction finding is available for 1 Mbps and 2 Mbps Bluetooth LE modes.

The Angle of Arrival (AoA) receiver and Angel of Departure (AoD) transmitter use the antenna arrays, switched on one by one, to be able to calculate the direction of a peer device. The received IQ samples are used to determine the relative path lengths between the antenna pairs and subsequently pinpoint the location of the transmitter.

The AoA transmitter beacon and AoD receiver peers do not require antenna arrays.

For information about additional Bluetooth location services, visit the Bluetooth SIG website [6].

2.4 System functions

2.4.1 Power modes

NORA-B1 series modules are power efficient devices capable of operating in different power saving modes and configurations. Different sections of the module can be powered off when they are not needed, and complex wake up events can be generated from different external and internal inputs. The network (radio) core operates independently of the application core.

The four main power modes are:

- System ON
- System ON idle sub-modes
- System OFF – lowest power consumption
- Network Force-OFF

Depending on the application, the module should spend most of its time in either idle or System OFF mode to minimize current consumption.

2.4.1.1 System ON

System ON is the default operation after power-on reset. You can switch on or reboot the NORA-B1 modules in one of the following ways:

- Rising edge on the VDD pin to a valid supply voltage
- Issuing a reset of the module. See also Module reset.

An event to wake up from the System OFF mode to the active mode can be triggered by:

- Programmable digital or analog sensor event. For example, a rising voltage level on an analog comparator pin
- Detecting an NFC field
- Supplying 5 V to the VBUS pin (plugging in the USB interface)

When waking up from System ON IDLE mode to System ON mode, an event can also be triggered by:

- RTC on-board Real Time Counter
- Radio interface
- Detection of an NFC field

2.4.1.2 System ON idle sub-modes

In System ON operation, when the CPU and all peripherals are IDLE, the system can reside in one of following power sub-modes:

- Constant latency – wakeup and task response are constant and kept at a minimum. This is secured by a set of resources that are always enabled.
- Low-power – lowest System ON power consumption.

2.4.1.3 System OFF

System off is the lowest power consumption mode the system can enter. The core functionality of the system is powered down and all ongoing tasks are terminated.

There is no dedicated pin to power off NORA-B1 modules. Any GPIO pin can be configured to trigger the application to enter System OFF mode which essentially powers down the module.

An under-voltage (brown-out) shutdown occurs on the NORA-B1 modules when the VDD supply drops below the operating range minimum limit. If this occurs, it is not possible to store the current parameter settings in the non-volatile area of the module memory.

To enable the lowest power operations, the network core can also be independently turned off with Network Force-OFF.

2.4.1.4 Force-OFF

The network core can be held in Force-OFF while the application core continues to run.

2.4.2 Module reset

There are several reset sources:

- **Power-on reset**: The application core starts when VDD rises above the power-on threshold. Network core remains in Force-OFF.
- **Pin reset**: Similar to power-on reset, the application core starts after asserting and deasserting the RESET_N pin. The network core remains in Force-OFF.
- **Brownout reset**: The system is placed in reset state if the VDD supply drops below the brownout threshold. The network core remains in Force-OFF.
- **Wake from System OFF mode reset**: The system is reset when waking from System OFF mode. The network core remains in Force-OFF.
- **Soft reset**: When the application core initiates a soft reset, both application and network cores are reset. The network core remains in Force-OFF. When the network core initiates a soft reset, only the network core is reset.
- **Watchdog timer (WDT) reset**: When the application core watchdog timer times out, the application core is reset, and the network core remains in Force-OFF. If the network core WDT times out, only the network core is reset.
- **Force-OFF**: in addition to the reset sources described above, the application core can programmatically hold the network core in Force-OFF. Depending on the reset source, different processor functions are affected. Refer to the system integration guide [1] for full details.

2.4.3 CPU and memory

The integrated Nordic Semiconductor nRF5340 chip in NORA-B1 series modules includes two powerful and fully programmable Arm Cortex-M33 processors. Both processor cores have a 32-bit instruction set (Thumb®-2 technology) that implements a superset of 16- and 32-bit instructions.

The application processor includes an FPU, CryptoCell-312 TrustZone® technology, and a full set of peripherals. It has 1 MB flash and 512 kB low-leakage RAM. Operation can occur at 128 MHz or 64 MHz.

The network processor includes peripherals for efficient operation of radio protocols including Bluetooth LE, IEEE 802.15.4 and proprietary 2.4 GHz protocols. It has 256 kB flash and 64 kB low-leakage RAM. Operation is at 64 MHz.

A volatile memory controller provides configurable retention of RAM sections based on the system power state.

2.4.4 Direct Memory Access

Many of the peripherals described in this data sheet utilize Direct Memory Access (DMA, also known as EasyDMA) to provide a direct interface to the RAM without involving the CPU. Fluent operation of the CPU is ensured with minimal need for interruptions. DMA should be used whenever possible to reduce the overall power consumption.

2.4.5 Distributed Programmable Peripheral Interconnect (DPPI)

Each core of the Nordic Semiconductor nRF5340 chip implemented in NORA-B1 series modules includes a distributed programmable peripheral interconnect (DPPI). Functioning as a switch matrix, the DPPI connects various control signals between the different interfaces and system functions.

With DPPI most interfaces can bypass the CPU to trigger a system function. Consequently, an incoming data packet can trigger a counter, falling voltage level on an ADC, or toggle a GPIO – without having to interrupt the CPU. This facilitates the development of smart, power-efficient applications that wake up the CPU only when it is necessary.

2.4.6 Real-Time Counter (RTC)

A key system feature available on both cores of the module is the Real-Time Counter. This counter can generate multiple interrupts and events to the CPU and radio as well as internal and external hardware blocks. These events can be precisely timed ranging from microseconds up to hours and allow periodic Bluetooth LE advertising events without involving the CPU for example.

The RTC can operate in System ON and System OFF modes. The low frequency clock is the source of the RTC. It may be generated through an optional, external crystal supplied by the host PCB, or internally through the RC oscillator function.

2.5 Serial peripherals

NORA-B1 modules support the following serial communication interfaces in their application and network cores:

Application core

- QSPI (with XIP)
- SPI: up to five master or slave instances with EasyDMA
- I2C (TWI): up to four master or slave instances with EasyDMA
- UART: up to four instances with RTS/CTS flow control and EasyDMA
- I2S: one instance

Network core

- SPI: one master or slave instance with EasyDMA
- I2C (TWI): one master or slave instance with EasyDMA
- UART: one instance with EasyDMA

☞ Most input/output pins on the module are shared between the digital interfaces, analog interfaces, and GPIOs. Unless otherwise stated, all functions can be assigned to any pin that is not already occupied.

☞ Four of the SPI interfaces share common hardware with I2C interfaces and cannot be used simultaneously. If both I2C interfaces are in use only one SPI interface is available.

2.5.1 Universal Asynchronous Receiver/Transmitter (UART)

The 4-wire UART interface supports hardware flow control with baud rates up to 1 Mbps. Up to four instances can be defined on the application core, and one on the network core.

Other characteristics of the UART interface include:

- Pin configuration:
  - **TXD**, data output pin
  - **RXD**, data input pin
  - **RTS**, Request To Send, flow control output pin (optional)
  - **CTS**, Clear To Send, flow control input pin (optional)
- Hardware flow control or no flow control is supported.
- Power saving indication available on the hardware flow control output (**RTS** pin): The line is driven to the OFF state when the module is not ready to accept data signals.
- Programmable baud rate generator allows most industry standard rates, as well as non-standard rates up to 1 Mbps.
- Frame format configuration:
  - 8 data bits
  - Even or no-parity bit
  - 1 stop bit
- 8N1default frame configuration, meaning eight (8) data bits, no (N) parity bit, and one (1) stop bit.
- Frames are transmitted in such a way that the least significant bit (LSB) is transmitted first.

2.5.2 Serial Peripheral Interface (SPI)

NORA-B1 supports up to four Serial Peripheral Interfaces with serial clock frequencies of up to 32 MHz.

Other characteristics of the SPI interfaces include:

- Pin configuration in master mode:
  - **SCLK**, Serial clock output, up to 32 MHz
  - **MOSI**, master output to slave input data line
  - **MISO**, master input from slave output data line
  - **CS**, Chip select output, active low, selects which peripheral on the bus to talk to. Only one select line is enabled by default but more can be added by customizing a GPIO pin.
  - **DCX**, Data/Command signal. An optional signal used by SPI slaves to distinguish between SPI commands and data
- Pin configuration in peripheral mode:
  - **SCLK**, Serial clock input
  - **MOSI**, master output to slave input data line
  - **MISO**, master input from slave output data line
  - **CS**, Chip select input, active low, connects/disconnects the lave interface from the bus.
- Both master and slave modes are supported on all interfaces.
- The serial clock supports both normal and inverted clock polarity (CPOL) and data should be captured on rising or falling clock edge (CPHA).

2.5.3 High-Speed Serial Peripheral Interface

SPIM4 can be set to high-speed mode – up to 32 MHz – when using the pins dedicated to high-speed use.

2.5.4 Quad Serial Peripheral Interface (QSPI)

The Quad Serial Peripheral Interface enables external memory to be connected to NORA-B1 modules. The QSPI supports eXecute In Place (XIP), which allows CPU instructions to be read and executed directly from the external memory.

Characteristics for the QSPI are listed below:

- QSPI always operates in master mode using the following pin configuration:
  - **CLK**, serial clock output, up to 96 MHz
  - **CS**, Chip select output, active low, selects which peripheral on the bus to talk to
  - **D0**, serial output (**MOSI**) data in single mode, data I/O signal in dual/quad mode
  - **D1**, serial input (**MISO**) data in single mode, data I/O signal in dual/quad mode
  - **D2**, data I/O signal in quad mode (optional)
  - **D3**, data I/O signal in quad mode (optional)
- Single/dual/quad read and write operations (1/2/4 data signals)
- Clock speeds between 2 – 32 MHz
- Data rates up to 48 MB/s in quad mode
- 32-bit addressing can address up to 4 GB of data
- Instruction set includes support for deep power down mode of the external flash
- Possible to generate and read the responses of custom flash instructions containing a 1byte opcode with up to 8 bytes of additional data

2.5.5 Inter-Integrated Circuit Interface (I2C)

The Inter-Integrated Circuit (I2C) interfaces can be used to transfer and/or receive data on a 2-wire bus network. NORA-B1 modules can operate as both master and slave on the I2C bus using 100 kbps (standard), 250 kbps, and 400 kbps (fast) transmission speeds. The interface supports clock stretching, which allows NORA-B1 modules to temporarily pause any I2C communications. Up to 127 individually addressable I2C devices can be connected to the same two signals.

Pin configuration:

- **SCL**, clock output in master mode, input in slave mode
- **SDA**, data input/output pin

To work properly in the master mode the I2C requires external pull-up resistors referenced to **VDD**. Pull-up resistors referenced to **VDD** are required in the peripheral mode as well but should be placed at the master end of the interface. See also I2C pull-up resistor values.

2.5.6 Inter-IC Sound interface (I2S)

The Inter-IC Sound (I2S) interface is used to transfer audio sample streams between NORA-B1 and external audio devices such as codecs, DACs, and microphones. It supports original I2S and left or right-aligned interface formats in both master and slave modes.

Pin configuration:

- **MCK**, master clock
- **LRCK**, left right/word/sample clock
- **SCK**, serial clock

- **SDIN**, serial data in
- **SDOUT**, serial data out

The master side of an I2S interface always provides the **LRCK** and **SCK** clock signals, but some master devices cannot generate a **MCK** clock signal. NORA-B1 can supply a **MCK** clock signal in both master and slave modes to provide to those external systems that cannot generate their own clock signal. The two data signals, **SDIN** and **SDOUT**, allow for simultaneous bi-directional audio streaming. The interface supports 8, 16, and 24-bit sample widths with up to 48 kHz sample rate.

2.5.7 USB 2.0 interface

NORA-B1 series modules include a full speed Universal Serial Bus (USB) device interface which is compliant to version 2.0 of the USB specification.

Characteristics of the USB interface include:

- Full speed device, up to 12 Mbps transfer speed
- MAC and PHY implemented in the hardware
- Automatic or software controlled internal pull-up of the **USB_DP** pin

Pin configuration:

- **VBUS**, 5 V supply input, required to use the interface
- **USB_DP**, **USB_DM**, differential data pair

The USB interface has a dedicated power supply that requires a 5 V supply voltage from the upstream host to be applied to the **VBUS** pin. This allows the USB interface to be used even though the rest of the module might be battery powered or supplied by a 1.8 V supply, or similar.

2.6 GPIO

NORA-B1 series modules have a versatile pin-out. In an un-configured state, NORA-B1 supports a total of 48 GPIO pins and no analog or digital interfaces. All interfaces or functions must then be allocated to a GPIO pin before use and configured within the operating context of the Application core.

10 out of the 48 GPIO pins are analog enabled, meaning that they can have an analog function allocated to them. Table 4 shows the number of digital and analog functions that can be assigned to a GPIO pin.

☞ **P0.00/XL1** and **P0.01/XL2** default to GPIO but can be configured to connect an external 32.768 kHz crystal circuit.

☞ **P0.02/NFC1** and **P0.03/NFC2** default to NFC provided by the application core but can also be configured to operate as GPIO.

☞ In NORA-B12, **P1.09/CRX** and **P1.08/CTX** are dedicated to FEM control.

2.6.1 Drive strength

All GPIO pins are normally configured for low current consumption. Using this standard drive strength, a pin configured as output can only source or sink a certain amount of current. If the timing requirements of a digital interface cannot be met, or if an LED requires more current, a high drive strength mode is available so the digital output can draw more current. In addition to drive strength, GPIO pins configured for output can be set for push-pull or open-drain. GPIO pins configured for input can float or enable internal pull-up or pull-down resistors. See also Digital pins.

Function	Description	Default NORA pin	Configurable GPIOs
General purpose input	Digital input with configurable pull-up, pull-down, edge detection and interrupt generation		Any

Function	Description	Default NORA pin	Configurable GPIOs
General purpose output	Digital output with configurable drive strength, push-pull or open drain output		Any
Pin disabled	Pin is disconnected from the input and output buffers	All*	Any
Timer/ counter	High-precision time measurement between two pulses/ Pulse counting with interrupt/event generation		Any
Interrupt/ Event trigger	Interrupt/event trigger to the software application/ Wake up event		Any
HIGH/LOW/Toggle on event	Programmable digital level triggered by internal or external events without CPU involvement		Any
ADC input	8/10/12/14-bit analog to digital converter		Any analog
Analog comparator input	Compares two voltages. Capable of generating wake-up events and interrupts		Any analog
PWM output	Simple output or complex pulse-width modulation waveforms		Any

* = If left unconfigured

Table 4: GPIO custom functions configuration

2.7 Digital peripherals

2.7.1 Pulse Width Modulation (PWM)

NORA-B1 modules provide up to four PWM units each with four PWM channels that can be used to generate complex waveforms. These waveforms can be used to control motors, dim LEDs, or function as audio signals when connected to speakers. Duty-cycle sequences can be stored in the RAM, chained, and looped into complex sequences without CPU intervention. Each channel uses a single GPIO pin as output.

2.7.2 Pulse Density Modulation (PDM)

The pulse density modulation interface is used to read signals from external audio frontends like digital microphones. It supports single or dual-channel (left and right) data input over a single GPIO pin. It supports up to 16 kHz sample rate and 16-bit samples. The interface uses the EasyDMA to automatically move the sample data into RAM without CPU intervention. The interface uses two signals: **CLK** to output the sample clock and **DIN** to read the sample data.

2.7.3 Quadrature Decoder (QDEC)

The quadrature decoder is used to read quadrature encoded data from mechanical and optical sensors in the form of digital waveforms. Quadrature encoded data is often used to indicate rotation of a mechanical shaft in either a positive or negative direction. The QDEC uses two inputs, **PHASE_A** and **PHASE_B**, and an optional **LED** output signal. The interface has a selectable sample period ranging from 128 µs to 131 ms.

2.8 Analog interfaces

10 out of the 48 digital GPIOs can be multiplexed to analog functions. The following analog functions are available:

- 1x 8-channel ADC[2]
- 1x Analog comparator[2,3]
- 1x Low-power analog comparator[2,3]

[2] Each analog pin may only be assigned to one function at any given time, ADC, COMP, or LPCOMP
[3] Only one comparator type may be enabled at any given time, COMP or LPCOMP

2.8.1 Analog to Digital Converter (ADC)

The Analog to Digital Converter (ADC) is used to sample analog voltage on the analog function enabled pins of the NORA-B1. Any of the 8 analog inputs can be used.

Characteristics of the ADC include:

- Full swing input range of 0 V to **VDD**
- 8/10/12-bit resolution
- 14-bit resolution while using oversampling
- Up to 200 kHz sample rate
- Single shot or continuous sampling
- Two operation modes: Single-ended or Differential
  - Single-ended mode, where a single input pin is used
  - Differential mode, where two inputs are used and the voltage level difference between them is sampled

If the sampled signal level is much lower than the **VDD**, it is possible to lower the input range of the ADC to better encompass the wanted signal. This produces higher effective resolution. Continuous sampling can be configured to sample at a configurable time interval or at different internal or external events – without CPU involvement.

2.8.2 Comparator

The analog comparator compares the analog voltage on one of the analog enabled pins in NORA-B1 with a highly configurable internal or external reference voltage. Events can be generated and distributed to the rest of the system when the voltage levels cross.
Further characteristics of the comparator include:

- Full swing input range of 0 V to **VDD**
- Two operation modes: Single-ended or Differential
- Single-ended mode:
  - A single reference level or an upper and lower hysteresis selectable from a 64-level reference ladder with a range from 0 V to **VREF** (described in Table 5)
- Differential mode:
  - Two analog pin voltage levels are compared, optionally with a configurable hysteresis
- Three selectable performance modes - High speed, balanced, or power save

For information about the electrical specifications of the various analog comparator options, see also Analog comparators .

2.8.3 Low power comparator

In addition to the power save mode available for the comparator, there is a separate low power comparator available on the NORA-B1 module. This allows for even lower power operation, at a slightly lower performance and with less configuration options.

Characteristics of the low power comparator include:

- Full swing input range of 0 to **VDD**
- Two operation modes - Single-ended or Differential
- Single-ended mode:
  - The reference voltage **LP_VIN–** is selected from a 15-level reference ladder
- Differential mode:
  - Pin **P0.04/AIN0** or **P0.05/AIN1** is used as reference voltage **LP_VIN–**
- Can be used to wake the system from sleep mode

For information about the electrical specifications of the various analog comparator options, see also Analog comparators. For a summary of the analog pin options, see also Table 5.

Since the run current of the low power comparator is very low, it can be used in the module sleep mode as an analog trigger to wake up the CPU. See also Power modes.

2.8.4 Analog pin options

Table 5 shows the supported connections of the analog functions.

☞ An analog pin may not be simultaneously connected to multiple functions.

Symbol	Analog function	Can be connected to
ADCP	ADC single-ended or differential positive input	Any analog pin or **VDD**
ADCN	ADC differential negative input	Any analog pin or **VDD**
VIN+	Comparator input	Any analog pin
VREF	Comparator single-ended mode reference ladder input	Any analog pin, **VDD**, 1.2 V, 1.8V or 2.4 V
VIN-	Comparator differential mode negative input	Any analog pin
LP_VIN+	Low-power comparator IN+	Any analog pin
LP_VIN-	Low-power comparator IN-	**P0.04/AIN0** or **P0.05/AIN1**, 1/16 to 15/16 **VDD** in steps of 1/16 **VDD**

Table 5: Possible uses of the analog pins

2.9 Debug

2.9.1 Multi-drop Serial Wire Debug (SWD)

NORA-B1 series modules provide ARM Multi-drop SWD technology for flashing and debugging. Each core shares an external connection to one set SWD signals — **SWDIO** and **SWDCLK**. The cores are then addressed individually. Additionally, NORA-B1 can be connected over the same SWD interface to other CPUs that support Multi-drop SWD.

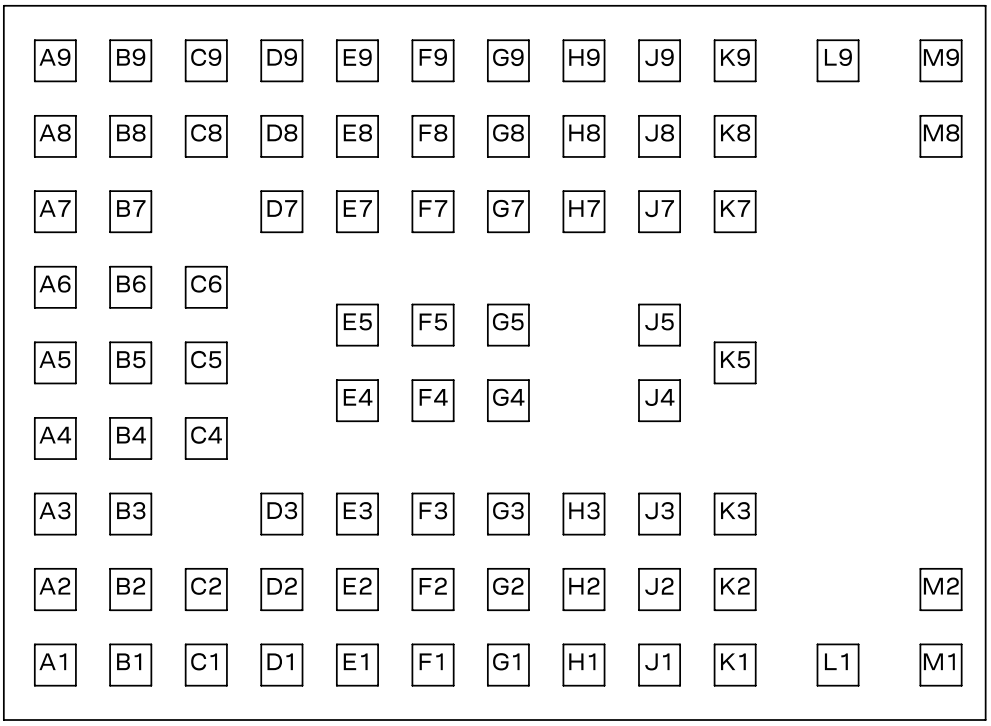
2.9.2 Parallel trace

The application core within NORA-B1 series modules supports parallel trace output. This facilitates output from the Embedded Trace Macrocell (ETM) and Instrumentation Trace Macrocell (ITM) embedded in the Arm Cortex-M33 core integrated in NORA-B1. The ETM trace data allows a user to record exactly how the application processes the CPU instructions in real time.

The parallel trace interface uses one clock signal and four data signals respectively: **TRACE_CLK**, **TRACE_D0**, **TRACE_D1**, **TRACE_D2** and **TRACE_D3**. For information about the shared assignments of the GPIO pins, see the pin assignments Table 6.

3 Pin definition

3.1 NORA-B1 pin assignment



TOP VIEW

Figure 3: Pin assignment

The pin-out assignment in Table 6 shows the module in an unconfigured state.

Most of the digital functions described in this data sheet can be freely assigned to any GPIO pin that is marked “Px.xx”. NORA-B12 reserves **P1.09/CRX** and **P1.08/CTX** for FEM control.

Alternative, dedicated pin functions are shown after the GPIO pin name.

Do not apply an NFC field to the NFC pins when they are configured as GPIOs. Failure to observe this can cause permanent damage to the module. When driving different logic levels on these pins in the GPIO mode, a small current leakage occurs. Make sure these pins are set to the same logic level before entering any of the power saving modes. See also RESET_N pin.

No	Name	I/O	Description
A1	VSS	Power	Ground pad
A2	P0.12/TRACECLK/DCX	I/O	GPIO/Trace buffer clock/Dedicated pin for high-speed SPIM4
A3	P1.03/TWI	I/O	GPIO/High-speed pin for 1 Mbps TWI
A4	P1.00	I/O	GPIO
A5	P0.20	I/O	GPIO
A6	N/C		Reserved – do not connect
A7	VDD	Power	1.7 VDC to 3.6 VDC power supply input and GPIO reference voltage

No	Name	I/O	Description
A8	VDDH	Power	High voltage mode: 2.5 VDC to 5.5 VDC power supply input Normal voltage mode: connect to VDD NORA-B12: internally connected to VDD
A9	VSS	Power	Ground pad
B1	P0.08/TRACEDATA3/SCK	I/O	GPIO/Trace buffer TRACEDATA[3]/Dedicated pin for high-speed SPIM4
B2	VSS	Power	Ground pad
B3	P0.11/TRACEDATA0/CSN	I/O	GPIO/Trace buffer TRACEDATA[0]/Dedicated pin for high-speed SPIM4
B4	P1.02/TWI	I/O	GPIO/High-speed pin for 1 Mbps TWI
B5	P0.03/NFC2	I/O	GPIO/NFC antenna connection
B6	P0.01/XL2	I/O	GPIO/Connection for 32 kHz crystal
B7	VDD	Power	1.7 VDC to 3.6 VDC power supply input and GPIO reference voltage
B8	VSS	Power	Ground pad
B9	VBUS	Power	4.35 VDC to 5.5V DC power supply for USB operation
C1	P0.10/TRACEDATA1/MISO	I/O	GPIO/Trace buffer TRACEDATA[1]/Dedicated pin for high-speed SPIM4
C2	P0.09/TRACEDATA2/MOSI	I/O	GPIO/Trace buffer TRACEDATA[2]/Dedicated pin for high-speed SPIM4
C4	P1.01	I/O	GPIO
C5	P0.02/NFC1	I/O	GPIO/NFC antenna connection
C6	P0.00/XL1	I/O	GPIO/Connection for 32 kHz crystal
C8	P0.22	I/O	GPIO
C9	USB_DP	I/O	USB D+
D1	P0.15/IO2	I/O	GPIO/Dedicated pin for Quad SPI
D2	P0.13/IO0	I/O	GPIO/Dedicated pin for Quad SPI
D3	P0.07/AIN3	I/O	GPIO/Analog input
D7	P0.23	I/O	GPIO
D8	P0.04/AIN0	I/O	GPIO/Analog input
D9	USB_DM	I/O	USB D–
E1	P0.18/CSN	I/O	GPIO/Dedicated pin for Quad SPI
E2	P0.14/IO1	I/O	GPIO/Dedicated pin for Quad SPI
E3	P0.21	I/O	GPIO
E4	VSS	Power	Ground pad
E5	VSS	Power	Ground pad
E7	P0.06/AIN2	I/O	GPIO/Analog input
E8	P0.05/AIN1	I/O	GPIO/Analog input
E9	P1.05	I/O	GPIO
F1	P0.17/SCK	I/O	GPIO/Dedicated pin for Quad SPI
F2	P0.16/IO3	I/O	GPIO/Dedicated pin for Quad SPI
F3	P0.19	I/O	GPIO
F4	VSS	Power	Ground pad
F5	VSS	Power	Ground pad
F7	P1.07	I/O	GPIO
F8	P1.14	I/O	GPIO
F9	P1.15	I/O	GPIO
G1	P1.06	I/O	GPIO
G2	P0.26/AIN5	I/O	GPIO
G3	P0.25/AIN4	I/O	GPIO/Analog input
G4	P1.04	I/O	GPIO

No	Name	I/O	Description
G5	P1.08 (P1.08/CTX)	I/O	GPIO, reserved for FEM PA enable on NORA-B12
G7	P1.09 (P1.09/CRX)	I/O	GPIO, reserved for FEM LNA enable on NORA-B12
G8	P1.12	I/O	GPIO
G9	P1.13	I/O	GPIO
H1	P0.24	I/O	GPIO
H2	SWDIO	Debug	Serial wire debug I/O for debug and programming
H3	P0.27/AIN6	I/O	GPIO/Analog input
H7	P0.29	I/O	GPIO
H8	P0.30	I/O	GPIO
H9	P1.11	I/O	GPIO
J1	N/C		Reserved – do not connect
J2	SWDCLK	Debug	Serial wire debug clock input for debug and programming
J3	RESET_N	I	Pin RESET with internal pull-up resistor
J4	N/C		Reserved – do not connect
J5	N/C		Reserved – do not connect
J7	P1.10	I/O	GPIO
J8	P0.28/AIN7	I/O	GPIO/Analog input
J9	P0.31	I/O	GPIO
K1	N/C		Reserved – do not connect
K2	VSS	Power	Ground pad
K3	VSS	Power	Ground pad
K5	VSS	Power	Ground pad
K7	VSS	Power	Ground pad
K8	VSS	Power	Ground pad
K9	ANT	I/O	Single-ended antenna connection Only connected on NORA-B101 and NORA-B121
L1	VSS	Power	Ground pad
L9	VSS	Power	Ground pad
M1	VSS	Power	Ground pad
M2	VSS	Power	Ground pad
M8	VSS	Power	Ground pad
M9	VSS	Power	Ground pad

Table 6: Pinout – captions and table contents are all 8pt bold

3.2 Dedicated peripheral pin configuration

In addition to the pins described in Table 6, the following peripherals also have dedicated pins that should be used for proper operation:

- **TWI**: For the fastest TWI 1 Mbps mode, the two high-speed **TWI** pins must be configured in the PSEL registers of the TWI peripheral. The 20 mA open-drain driver must also be enabled using the E0E1 drive setting in the DRIVE field of the PIN_CNF GPIO register.
- **QSPI**: Enabling QSPI requires the use of dedicated GPIO pins shown in Table 7. These must be enabled using the Peripheral setting of the MCUSEL field of the PIN_CNF register. The high drive H0H1 configuration must be set in the DRIVE field of the PIN_CNF GPIO register.

- **SPIM4**: For the fastest SPI mode, the special purpose GPIO pins are enabled using the Peripheral setting of the **MCUSEL** pin of the PIN_CNF register. When activated, the SPIM PSEL settings are ignored, and the dedicated pins are used. The GPIO must use the extra high drive E0E1 configuration in the DRIVE field of the PIN_CNF GPIO register.
- **TRACE**: When using trace, the **TRACEDATA[n]** and **TRACECLK** GPIO pins must all use the extra high drive E0E1 configuration in the DRIVE field of the PIN_CNF GPIO register. The TND option of the MCUSEL field of the PIN_CNF register must be used.

GPIO pin	Description
P0.08 - P0.12	Drive configuration E0E1 is available and must be used for TRACE. For 32 Mbps high-speed SPI using SPIM4, drive configuration H0H1 must be used.
P0.13 - P0.18	The H0H1 drive configuration features the highest speeds of quad SPI using the direct connection of the QSPI peripheral.
P1.02 and P1.03	The E0E1 drive configuration activates a 20 mA open-drain driver specifically designed for high-speed TWI.
Remaining pins	The E0E1 drive configuration is not supported. Using the E0E1 drive configuration will cause incorrect operation.

Table 7: Dedicated peripheral pin configuration

3.2.1 RF front end – PA / LNA

NORA-B12 uses an RF front end module that incorporates a PA and LNA to achieve superior RF performance. The Skyworks SKY66405-11 FEM IC used to increase TX power and RX sensitivity, which significantly improve the link budget for long-range connections. This section describes how to configure the SKY66405-11 through GPIO for radio operation.

By default, if all nRF5340 GPIOs are left in their default state the SKY66405-11 will be in a sleep mode.

The table below shows the control signal names, pin names and the state for each mode. Switching time between states is < 1µS.

State	P1.08/CTX	P1.09/CRX
Sleep	Low	Low
Transmit (PA enabled)	High	Low
Receive (LNA enabled)	Low	High
Bypass	High	High

Table 8: FEM control logic

The Skyworks SKY66405-11 is controlled through the application software loaded onto the network core of NORA-B12. The Zephyr board support package available on the u-blox GitHub site or directly through Zephyr enable FEM control through the nRF Connect SDK. See also the NORA-B1 SIM [1].

4 Electrical specifications

⚠ Stressing the device above one or more of the absolute maximum ratings can cause permanent damage. These are stress ratings only. Operating the module at these or at any conditions other than those specified in the recommended operating conditions should be avoided. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

☞ Operating condition ranges define those limits within which the functionality of the device is guaranteed. Where application information is given, it is advisory only and does not form part of the specification.

4.1 Absolute maximum ratings

Signal	Description	Condition	Min	Max	Unit
VDD	NORA-B10 Module supply voltage	Input DC voltage at VDD pin	–0.3	+3.9	V
VDD	NORA-B12 Module supply voltage	Input DC voltage at VDD pin	–0.3	+3.6	V
VDDH	NORA-B10 Module supply high voltage	Input DC voltage at VDDH pin	–0.3	+5.8	V
VDDH	NORA-B12 Module supply high voltage	Internally connected to VDD pin	–0.3	+3.6	V
VBUS	USB supply input	Input DC voltage at VDDH pin	–0.3	+5.8	V
VSS				0	V
$V_{I/O}$	Digital pin voltage	Input DC voltage at any digital I/O pin, VDD ≤ 3.6 V	–0.3	VDD + 0.3	V
		Input DC voltage at any digital I/O pin, VDD > 3.6 V	–0.3	+3.9	V
P_ANT	Maximum power at receiver	Input RF power at antenna pin		+10	dBm

Table 9: Absolute maximum ratings

⚠ The product is not protected against overvoltage or reversed voltages. Use appropriate protection devices to ensure that voltage spikes exceeding the power supply voltage specifications in Table 9 are kept within the specified limits.

4.1.1 Maximum ESD ratings

Parameter	Min	Typ	Max	Unit	Remarks
ESD sensitivity for all pins except **ANT** pin			2	kV	Human body model class 3A according to JEDEC JS001
			500	V	Charged device model according to JESD22-C101

Table 10: Maximum ESD ratings

⚠ NORA-B1 series modules are Electrostatic Sensitive Devices and require special precautions while handling. For ESD handling instructions, see also ESD precautions.

4.1.2 Flash memory endurance

Parameter	Value	Unit
Endurance	10,000	Write/erase cycles
Retention	10	Years at 40 °C

Table 11: Flash memory endurance

4.2 Recommended operating conditions

Unless otherwise specified, all given specifications have been measured at an ambient temperature of 25 °C with a supply voltage of 3.3 V.

Operation beyond the specified operating conditions is not recommended and extended exposure beyond them may affect device reliability.

4.2.1 Operating and storage temperature range

Parameter	Min	Typ	Max	Unit
Storage temperature	–40	+25	+125	°C
Operating temperature	–40	+25	+105	°C

Table 12: Temperature range

4.2.2 Supply/power pins

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Module supply voltage	1.7	3.3	3.6	V
VDDH	NORA-B10 module supply high voltage	2.5	3.7	5.5	V
VDDH	NORA-B12 module supply high voltage – connect to VDD	1.7	3.3	3.6	V
VBUS	USB supply input	4.35	5.0	5.5	V
t_RISE (10 µs)	VREGHOUT regulator start-up time with VDDH rise time of 10 µs		0.2	1.6	ms
t_RISE (10 mS)	VREGHOUT regulator start-up time with VDDH rise time of 10 ms		5		ms
t_RISE (50 mS)	VREGHOUT regulator start-up time with VDDH rise time of 50 ms	30	50	80	ms
VDD_ripple	VDD input noise peak to peak			100	mV
VDDH_ripple	VDDH input noise peak to peak			100	mV

Table 13: Input characteristics of voltage supply pins

4.2.3 Current consumption

Table 14 shows the typical current consumption of a NORA-B10 module at 3 V supply, independent of the software used.

Condition	Min	Typ	Max	Units
System Off, 0 kB application RAM, wake on reset			1.0	µA
System ON, wake on any event, power-fail comparator enabled			1.3	µA
System ON, 64 kB network RAM, wake on network RTC (running from LFXO clock)			1.5	µA
Application core running CoreMark benchmarking tests @ 128 MHz from flash, DC/DC			8.0	mA
Network core running CoreMark benchmarking tests @ 64 MHz from flash, DC/DC			2.6	mA
Radio RX only @ 1 Mbps Bluetooth LE mode			2.7	mA
Radio TX only, 0 dBm output power (DC-DC converter enabled)			3.4	mA
Radio TX only, +3 dBm output power (DC-DC converter enabled)			5.1	mA

Table 14: NORA-B10 VDD current consumption

Table 15 shows the typical current consumption of a NORA-B12 module at 3 V supply, independent of the software used.

Condition	Min	Typ	Max	Units
System Off, 0 kB application RAM, wake on reset (FEM in sleep mode)			2.0	µA
System ON, wake on any event, power-fail comparator enabled (FEM in sleep mode)			2.3	µA
System ON, 64 kB network RAM, wake on network RTC (running from LFXO clock (FEM in sleep mode)			3.5	µA
Application core running CoreMark benchmarking tests @ 128 MHz from flash, DC/DC (FEM in sleep mode)			8.0	mA
Network core running CoreMark benchmarking tests @ 64 MHz from flash, DC/DC (FEM in sleep mode)			2.6	mA
Radio RX only @ 1 Mbps Bluetooth LE mode (FEM LNA enabled)			8.2	mA
Radio TX only, +13 dBm output power (DC-DC converter enabled, FEM PA enabled)			22.1	mA

Table 15: NORA-B12 VDD current consumption

4.2.4 RF performance

Parameter	Test condition	Min	Typ	Max	Unit
Receiver input sensitivity	Conducted at 25 °C, 1 Mbit/s Bluetooth LE mode		–98		dBm
	Conducted at 25 °C, 2 Mbit/s Bluetooth LE mode		–95		dBm
	Conducted at 25 °C, 500 kbit/s Bluetooth LE mode		–100		dBm
	Conducted at 25 °C, 125 kbit/s Bluetooth LE mode		–104		dBm
Maximum output power	Conducted at 25 °C		+3		dBm
NORA-B106 antenna gain	Integral to EVK-NORA-B106		+2		dBi

Table 16: NORA-B10 RF performance

Parameter	Test condition	Min	Typ	Max	Unit
Receiver input sensitivity FEM LNA enabled	Conducted at 25 °C, 1 Mbit/s Bluetooth LE mode		–103		dBm
	Conducted at 25 °C, 2 Mbit/s Bluetooth LE mode		–99		dBm
	Conducted at 25 °C, 500 kbit/s Bluetooth LE mode		–105		dBm
	Conducted at 25 °C, 125 kbit/s Bluetooth LE mode		–109		dBm
Maximum output power FEM PA enabled	Conducted at 25 °C		+13		dBm
NORA-B126 antenna gain	Integral to EVK-NORA-B126		+2		dBi

Table 17: NORA-B12 RF performance

4.2.5 RESET_N pin

Pin name	Parameter	Min	Typ	Max	Unit	Remarks
RESET_N	Low-level input	0		0.3*VDD	V	
	Internal pull-up resistance		13		kΩ	
	RESET duration		13	40	ms	Time taken to release a pin reset with 500 nF capacitance at reset pin

Table 18: RESET_N pin characteristics

4.2.6 Digital pins

Pin name	Parameter	Min	Typ	Max	Unit	Remarks
Any digital pin	Input characteristic: Low-level input	0		0.3*VDD	V	
	Input characteristic: high-level input	0.7*VDD		VDD	V	
	Output characteristic: Low-level output	0		0.4	V	Standard drive strength
		0		0.4	V	High drive strength
	Output characteristic: High-level output	VDD-0.4		VDD	V	Standard drive strength
		VDD-0.4		VDD	V	High drive strength
	Sink/Source current	1	2	4	mA	Standard drive strength
		3			mA	High drive strength, VDD < 2.7 V
		6			mA	High drive strength, sink, VDD ≥ 2.7 V
		6			mA	High drive strength, source, VDD ≥ 2.7 V
	Rise/Fall time		9 – 26		ns	Standard drive strength, depending on load capacitance
			4–9		ns	High drive strength, depending on load capacitance
	Input pull-up resistance		13		kΩ	Can be added to any GPIO pin configured as input
	Input pull-down resistance		13		kΩ	Can be added to any GPIO pin configured as input
P0.02/NFC1, P0.03/NFC2	Leakage current		1	10	µA	When not configured for NFC and driven to different logic levels

Table 19: Digital pin characteristics

4.2.7 I2C pull-up resistor values

Symbol	Parameter	Bus capacitance	Min	Typ	Max	Unit
R_PU_standard	External pull-up resistance required on I2C interface in standard mode (100 Kbps), internal pull-up disabled	50 pF	1	-	12	kΩ
		200 pF	1	-	6	kΩ
		400 pF	1	-	5	kΩ
R_PU_fast	External pull-up resistance required on I2C interface in fast mode (400 Kbps), internal pull-up disabled	50 pF	1	-	3.5	kΩ
		200 pF	1	-	2	kΩ
		400 pF	1	-	1	kΩ

Table 20: Suggested pull-up resistor values

4.2.8 Analog comparators

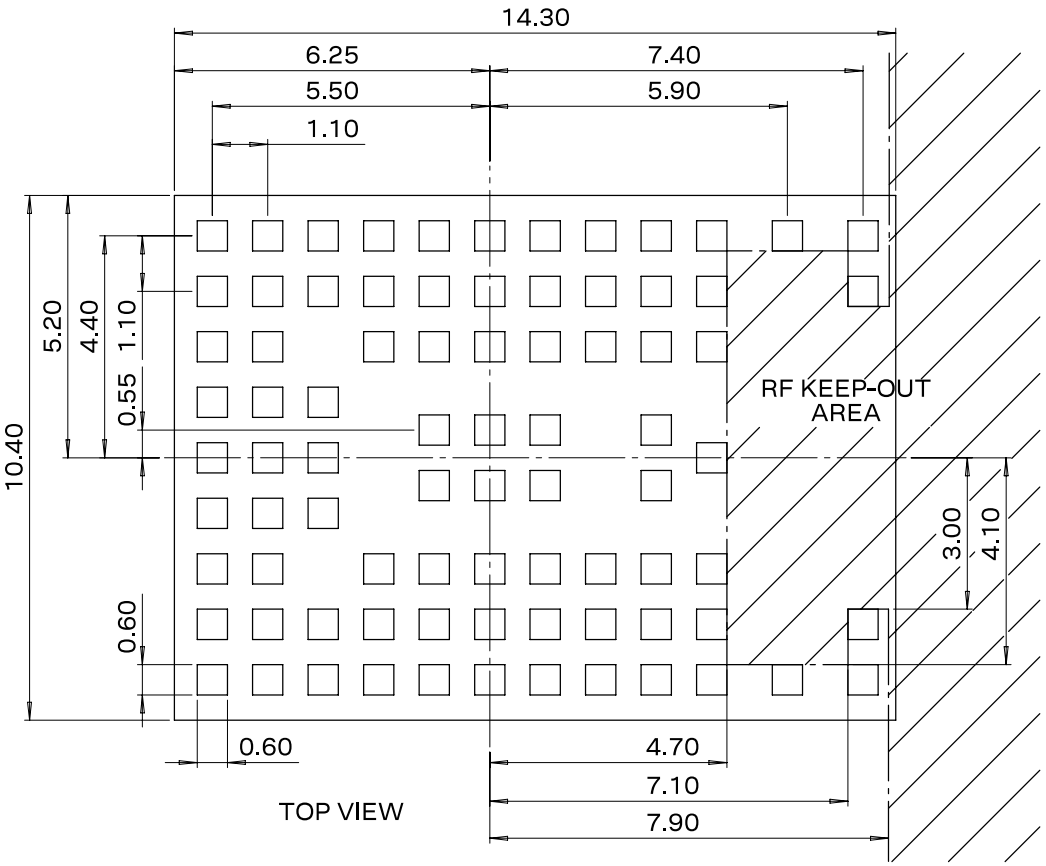
Symbol	Parameter	Comparator	Min	Typ	Max	Unit
t_powersave	Time to generate interrupt/event when the comparator is in “power save” mode	COMP		0.6		µs
t_balanced	Time to generate interrupt/event when the comparator is in “balanced” mode	COMP		0.2		µs
t_speed	Time to generate interrupt/event when the comparator is in “high speed” mode	COMP		0.1		µs
t_lpcanadet	Time from VIN crossing (≥ 50 mV above threshold) to ANADETECT signal generation	LPCOMP		2.7		µs

Table 21: Electrical specification of the two analog comparators

5 Mechanical specifications

5.1 NORA-B1 footprint dimensions

Figure 4 shows the common footprint and dimensions of NORA-B1 series modules that are shared across the whole product family.

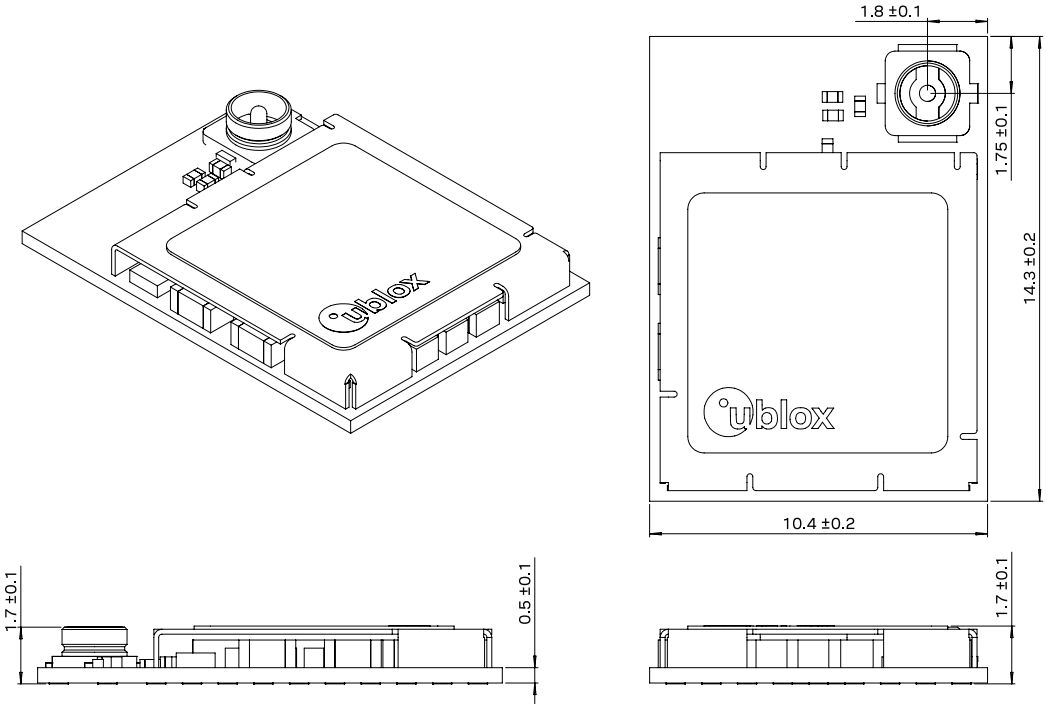


All dimensions in mm.

Figure 4: NORA-B1 footprint dimensions

5.2 NORA-B1 mechanical specifications

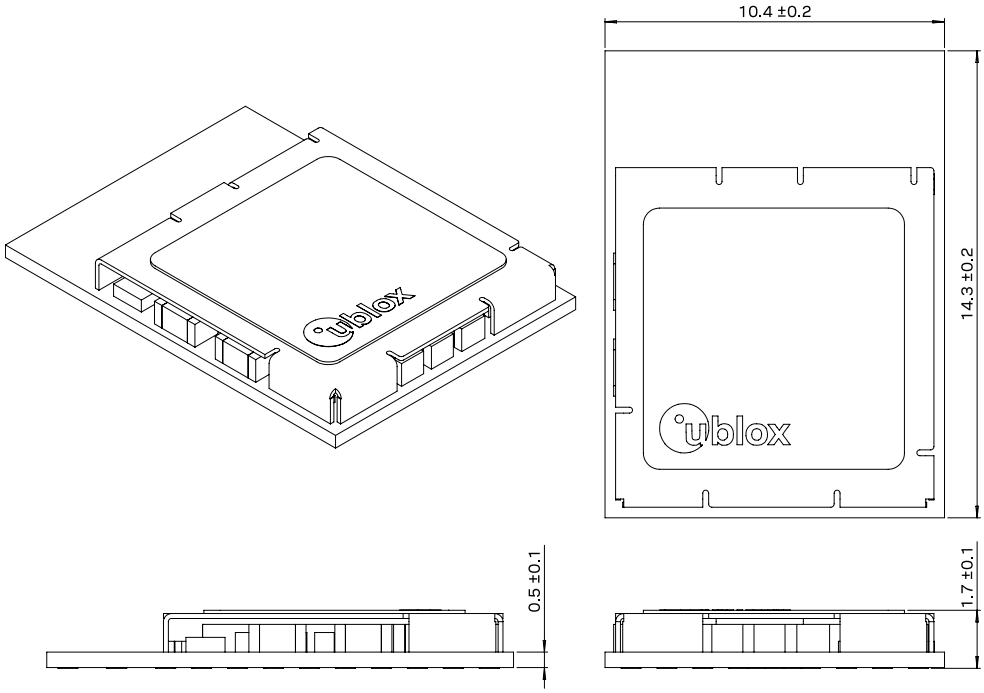
5.2.1 NORA-B100 and NORA-B120 mechanical specifications



Dimensions in mm

Figure 5: NORA-B100 and NORA-B120 mechanical specification

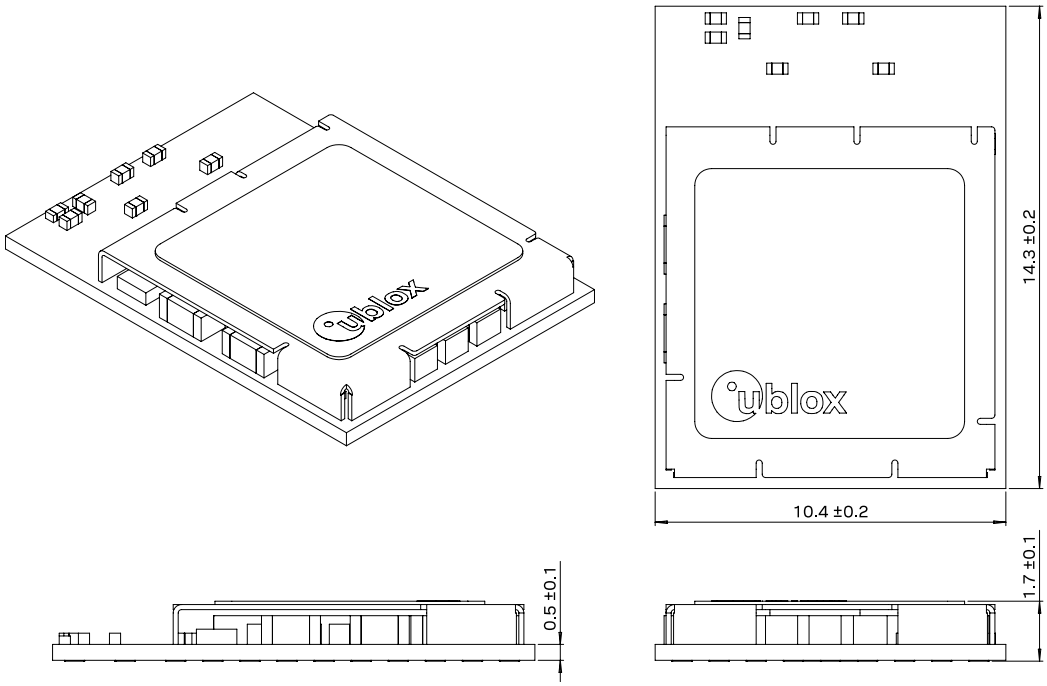
5.2.2 NORA-B101 and NORA-B121 mechanical specifications



Dimensions in mm

Figure 6: NORA-B101 and NORA-B121 mechanical specification

5.2.3 NORA-B106 and NORA-B126 mechanical specifications



Dimensions in mm

Figure 7: NORA-B106 and NORA-B126 dimensions

6 Qualifications and approvals

⚠ Approvals are pending.

The development status of NORA-B1 series modules is described in the document information. Consequently, the information given in this chapter only becomes valid after each module variant has been fully tested and approved during the Initial Production stage.

6.1 Country approvals

NORA-B1 modules are certified for use in the following countries/regions:

Country/region	NORA-B100	NORA-B101	NORA-B106	NORA-B120	NORA-B121	NORA-B126
Europe	Approved	Approved	Approved	Pending	Pending	Pending
USA	Approved	Approved	Approved	Pending	Pending	Pending
Canada	Approved	Approved	Approved	Pending	Pending	Pending
Brazil	Approved	Approved	Approved	Pending	Pending	Pending
Japan	Pending	Pending	Pending	Pending	Pending	Pending
Taiwan	Pending	Pending	Pending	Pending	Pending	Pending
South Korea	Pending	Pending	Pending	Pending	Pending	Pending
Australia	Pending	Pending	Pending	Pending	Pending	Pending
New Zealand	Pending	Pending	Pending	Pending	Pending	Pending
South Africa	Pending	Pending	Pending	Pending	Pending	Pending

Table 22: Country approvals

☞ For detailed information about the regulatory requirements that must be met for all end-product applications based on NORA-B1 modules, see the system integration manual [1].

6.2 Bluetooth qualification

NORA-B1 series modules are qualified as Component (Tested) devices according to the Bluetooth 5.2 specification.

Product type	QD ID	Listing date
NORA-B10 RF-PHY Component (tested)	164871	2021-03-08
NORA-B12 RF-PHY Component (tested)	Pending	Pending

Table 23: NORA-B1 series Bluetooth qualified design ID

7 Product handling

7.1 Packaging

NORA-B1 series modules are delivered as hermetically sealed, reeled tapes to enable efficient production, production lot set-up and tear-down. For more information about packaging, see also the u-blox package information guide [2].

7.1.1 Reels

NORA-B1 series modules are deliverable in quantities of 500 pieces on a reel. The reel types for the modules are shown in Table 24.

For more detailed information, see also the u-blox package Information guide [2].

Model	Reel type
NORA-B100	A3
NORA-B101	A3
NORA-B106	A3
NORA-B120	A3
NORA-B121	A3
NORA-B126	A3

Table 24: Reel types for different models of the NORA-B1 series

7.1.2 Tapes

Figure 8 shows the position and orientation of the NORA-B1 series modules as they are delivered on tape.

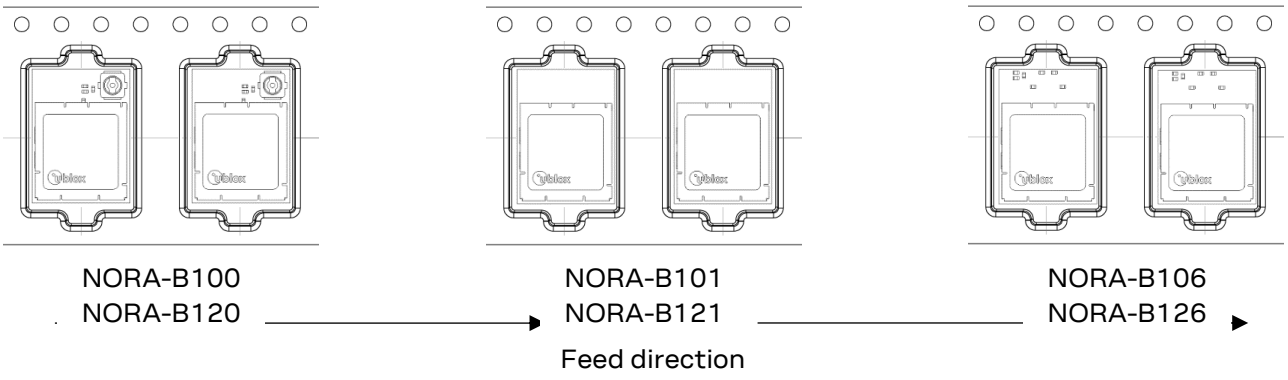


Figure 8: Orientation of NORA-B1 series modules on tape

Figure 9 shows the tape and pocket dimensions.

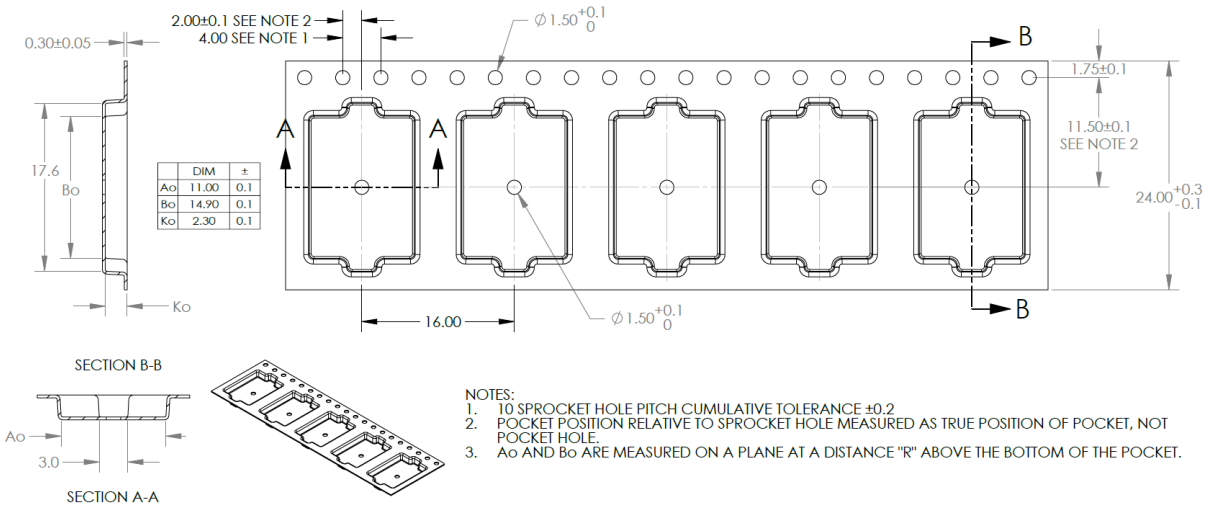


Figure 9: Tape and pocket dimensions

7.2 Moisture sensitivity levels

⚠ NORA-B1 series modules are classified as Moisture Sensitive Devices (MSD) in accordance with the IPC/JEDEC specification.

The Moisture Sensitivity Level (MSL) relates to the required packaging and handling precautions. NORA-B1 series modules are rated at **MSL level 3**. For more information regarding moisture sensitivity levels, labeling and storage, see the u-blox package information guide [2].

☞ For MSL standards, see also IPC/JEDEC J-STD-020. The standards can be downloaded from the JEDEC website [11].

7.3 Reflow soldering

Reflow profiles are selected according to u-blox recommendations. See the NORA-B1 series system integration manual [1] for more information.

⚠ Failure to follow these recommendations can result in severe damage to the device.

7.4 ESD precautions

⚠ NORA-B1 series modules contain highly sensitive electronic circuitry and are Electrostatic Sensitive Devices (ESD). Handling the NORA-B1 series modules without proper ESD protection may destroy or damage them permanently.

NORA-B1 series modules are electrostatic sensitive devices (ESD) and require special ESD precautions typically applied to the ESD sensitive components. See also Maximum ESD ratings.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling, and operation of any application that incorporates the NORA-B1 series module. Failure to observe t hese recommendations can result in severe damage to the device.

8 Labeling and ordering information

The labels on NORA-B1 series modules include important product information.

8.1 Module marking

Figure 13 shows the label applied to NORA-B1 series modules. Each of the given label references are described in Table 25.

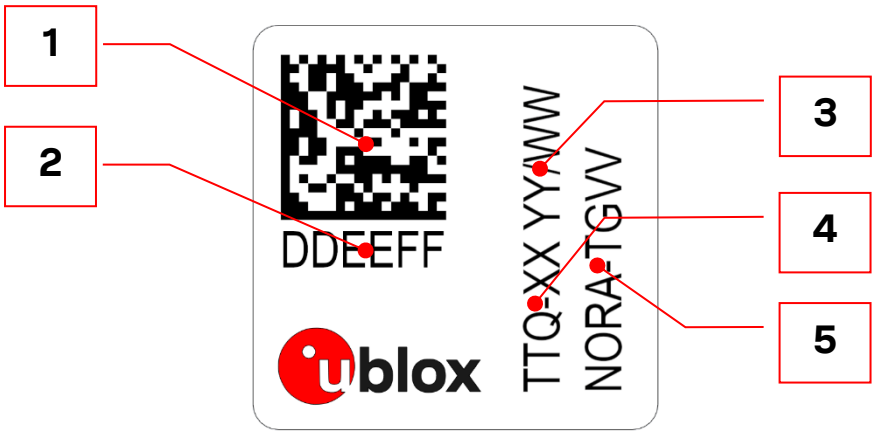


Figure 13: NORA-B1 series module marking

Reference	Description
1	Data Matrix with unique serial number comprising 19 alphanumeric symbols: - The first 3 symbols are used for production tracking and are an abbreviated representation of the Type number that is unique to each module variant. - The following 12 symbols represent the unique hexadecimal Bluetooth address of the module AABBCCDDEEFF, and The last 4 symbols represent the hardware and firmware version encoded HHFF.
2	Second half of the Bluetooth device address
3	Date of production encoded YY/WW (year / week)
4	Type number suffix
5	Product name (Model)

Table 25: NORA-B1 series module marking

8.2 Product identifiers

Table 26 describes the three product identifiers, namely the Type number, Model name and Ordering code.

Format	Description	Nomenclature
Model name	Describes the form factor, platform technology and platform variant. Used mostly in product documentation like this data sheet, the model name represents the most common identity for all u-blox products.	PPPP-TGVV
Ordering code	Comprises the model name – with additional identifiers to describe the major product version and quality grade.	PPPP-TGVV-TTQ
Type number	Comprises the model name and ordering code – with additional identifiers to describe minor product versions.	PPPP -TGVV-TTQ-XX

Table 26: Product code formats

8.3 Identification codes

Table 27 explains the parts of the product code.

Code	Meaning	Example
PPPP	Form factor	NORA
TG	Platform (Technology and Generation) T – Dominant technology, for example, W: Wi-Fi, B: Bluetooth G - Generation	B1: Bluetooth Generation 1 of NORA form factor
VV	Variant based on the same platform; range [00…99]	00: default configuration, with U.FL connector
TT	Major product version	00: first revision
Q	Quality grade A: Automotive B: Professional C: Standard	B: professional grade
XX	Minor product version (not relevant for certification)	Default value is 00

Table 27: Part identification code

8.4 Ordering information

Ordering Code	Product
NORA-B100-00B	NORA-B10 module with antenna connector U.FL, open CPU for custom applications
NORA-B101-00B	NORA-B10 module with antenna pin, open CPU for custom applications
NORA-B106-00B	NORA-B10 module with internal PCB antenna, open CPU for custom applications
NORA-B120-00B	NORA-B12 module with antenna connector U.FL, open CPU for custom applications
NORA-B121-00B	NORA-B12 module with antenna pin, open CPU for custom applications
NORA-B126-00B	NORA-B12 module with internal PCB antenna, open CPU for custom applications

Table 28: Product ordering codes

Appendix

A Glossary

Abbreviation	Definition
ADC	Analog to Digital Converter
AoA	Angle of Arrival
AoD	Angle of Departure
BPF	Band Pass Filter
CBC-MAC	cipher block chaining - message authentication code
CCM	Counter with cipher block chaining - message authentication code
CMAC	Cipher-based Message Authentication Code
CPU	Central Processing Unit
CTI	Cross Trigger Interface
CTR	AES CCM combines counter
CTS	Clear To Send
DC	Direct Current
DMA	Direct Memory Access
DPPI	Distributed Programmable Peripheral Interconnect
DWT	Data Watchpoint and Trace
ECB	Electronic CodeBook
EDM	Extended Data Mode
ESD	ElectroStatic Discharge
ETM	Embedded Trace Macrocell
FCC	Federal Communications Commission (United States)
FEM	Front End Module
FPU	Floating Point Unit
GATT	Generic ATTribute profile
GCM	Galois/Counter Mode
GPIO	General Purpose Input/Output
I2C	Inter-Integrated Circuit
ISED	Innovation, Science and Economic Development (Canada)
IEEE	Institute of Electrical and Electronics Engineers
IPC	Inter-Processor Communication
ITM	Instrumentation Trace Macrocell
LE	Low Energy
LNA	Low Noise Amplifier
MUTEX	Mutually Exclusive Peripheral
NFC	Near Field Communication
OEM	Original Equipment Manufacturer
OTP	One-Time Programmable
OUI	Organizationally Unique Identifier
PA	Power Amplifier
PDM	Pulse Density Modulation
PWM	Pulse Width Modulation
QDEC	Quadrature DECoder

Abbreviation	Definition
QSPI	Quad Serial Peripheral Interface
RAM	Random Access Memory
RNG	Random Number Generator
RTC	Real-Time Counter
RTLS	Real-Time Location Service
RTS	Request To Send
SDK	Software Development Kit
SPI	Serial Peripheral Interface
SWD	Serial Wire Debug
TBD	To Be Defined
TWI	Two-Wire Interface (See I2C)
UART	Universal Asynchronous Receiver/Transmitter
UICR	User Information Control Registers
WDT	WatchDog Timer
XIP	eXecute In Place

Table 29: Explanation of the abbreviations and terms used

Related documents

[1] NORA-B1 system integration manual, UBX-20027617
[2] u-blox package information guide, UBX-14001652
[3] u-blox GitHub repository
[4] Nordic Semiconductor nRF5340 product specification
[5] Nordic Semiconductor nRF Connect SDK
[6] Nordic Semiconductor nRF5340 power regulators
[7] Nordic Semiconductor nRF5340 clocks
[8] Nordic Semiconductor nRF5340 oscillators
[9] Skyworks SKY66405-11 data sheet
[10] Bluetooth SIG location services information
[11] JEDEC website

For product change notifications and regular updates of u-blox documentation, register on our website, www.u-blox.com.

Revision history

Revision	Date	Name	Comments
R01	29-Sep-2020	brec	Initial release
R02	12-Oct-2020	brec	Revised block diagram in section 1.3 to show ARM cortex M33
R03	09-Feb-2021	brec	Added tape and reel images for Figure 8 and Figure 9, updated dimensional drawings, updated specifications to match nRF5340 PS
R04	30-Jun-2021	brec	Updated product status to Initial Production. Updated specifications to match Nordic Semiconductor nRF5340 product specification, v1.1, added RED, FCC, ISED and Bluetooth certification information.
R05	19-Aug-2021	brec	Added information for NORA-B12 series throughout the document

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