

## Ground noise isolation Amplifier with Adjustable Differential Gain

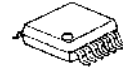
### ■ GENERAL DESCRIPTION

The **NJM2795** is a ground noise isolation amplifier. It contains dual channel differential amplifier with Adjustable Differential Gain.

It is developed for those car audio applications where long connections between head unit and other components are necessary and ground noise has to be eliminated.

Further the **NJM2795** allow the user to alter the gain to optimize the signal-to-noise ratio of their system. It is useful in microphone amplifier applications.

### ■ PACKAGE OUTLINE

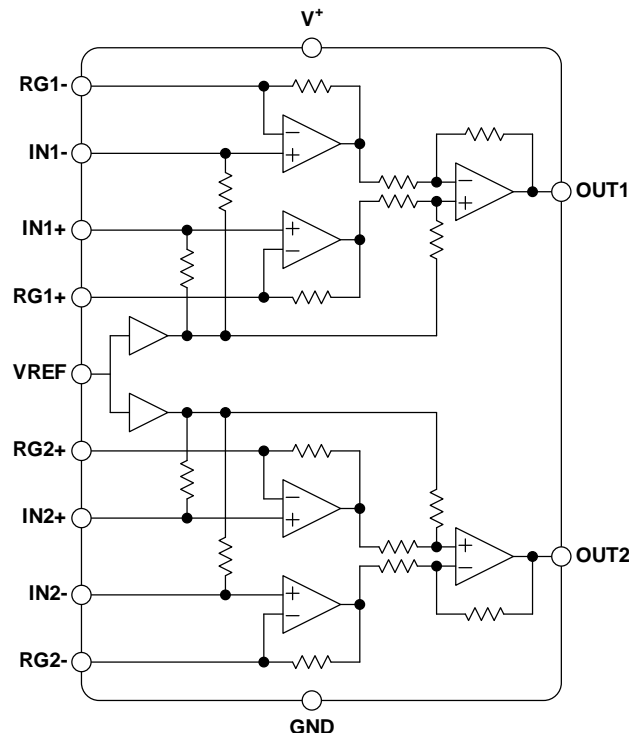


NJM2795V

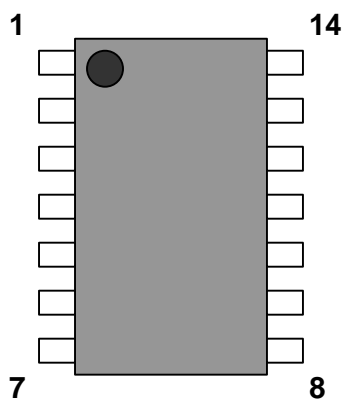
### ■ FEATURES

- Dual Channel Differential Amplifier
- Adjustable Differential Gain                   +6dB to +52dB
- Operating Voltage                               4.3 to 20V
- Operating Current                               7mA typ.
- Maximum Output Voltage                   2Vrms min., @ THD=1%
- Common mode rejection ratio           80dB typ.
- Supply Voltage Rejection Ratio       65dB typ.
- Total Harmonic Distortion               0.005% typ.
- Equivalent Input Noise Voltage       2 $\mu$ Vrms typ. @ Gv=+20dB
- Bipolar Technology
- Package Outline                               SSOP14

### ■ BLOCK DIAGRAM



## ■ PIN CONFIGURATION



No.	端子名	機能
1	OUT1	Output1
2	RG1-	Gain Adjustment 1+
3	GND	Ground
4	VREF	Reference Voltage
5	V <sup>+</sup>	Power Supply
6	RG2+	Gain Adjustment 2+
7	OUT2	Output2
8	IN2+	+Input2
9	RG2-	Gain Adjustment 2-
10	IN2-	-Input2
11	NC	No Connect
12	IN1-	-Input1
13	RG1+	Gain Adjustment 1+
14	IN1+	+Input1

## ■ ABSOLUTE MAXIMUM RANGES (Ta=25°C)

PARAMETER	SYMBOL	RANGE	UNIT
Supply Voltage	V <sup>+</sup>	+22	V
Maximum Input Voltage	V <sub>IM</sub>	0 to V <sup>+</sup> (*)	V
Power Dissipation	P <sub>D</sub>	SSOP14 : 555* <small>NOTE: EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 2layer, FR-4) mounting</small>	mW
Operating Temperature	Topr	-40 to +85	°C
Storage Temperature	Tstg	-40 to +150	°C

(\*) For the maximum input voltage less than 0 to V<sup>+</sup>

## ■ ELECTRICAL CHARACTERISTIC (V<sup>+</sup>=9V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
<b>DC CHARACTERISTIC</b>						
Operating Voltage	V <sup>+</sup>		4.3	9	20	V
Operating Current	I <sub>CC</sub>	No Signal	-	7	10	mA
Reference Voltage	V <sub>REF</sub>		4.0	4.5	5.0	V
<b>AC CHARACTERISTIC</b> (Non-inverting circuit, f=1kHz, V <sub>in</sub> =100mVrms, R <sub>G</sub> =0Ω, R <sub>G</sub> =10kΩ, R <sub>L</sub> =10kΩ unless otherwise specified)						
Voltage Gain 1	G <sub>V1</sub>	R <sub>G</sub> =91kΩ	+4.0	+6.0	+8.0	dB
Voltage Gain 2	G <sub>V2</sub>	R <sub>G</sub> =10kΩ	+18.0	+20.0	+22.0	dB
Voltage Gain 3	G <sub>V3</sub>	R <sub>G</sub> =220Ω, V <sub>in</sub> =2.5mVrms	+50.0	+52.0	+54.0	dB
Channel Separation	CS	V <sub>O</sub> =2Vrms, A-weighted	90	100	-	dB
Channel Balance	BAL		-	-	0.5	dB
Roll-off High Frequency	f <sub>RH</sub>	-3dB	100	-	-	kHz
Input Resistance	R <sub>IN</sub>		160	200	240	kΩ
Output Resistance	R <sub>OUT</sub>		-	200	-	Ω
Maximum Output Voltage 1	V <sub>OM1</sub>	THD=1%	2	2.5	-	Vrms
Maximum Output Voltage 2	V <sub>OM2</sub>	Inverting, THD=1%	-	2.5	-	Vrms
Equivalent Input Noise Voltage	V <sub>NI</sub>	R <sub>G</sub> =600Ω, A-weighted, G <sub>v</sub> =+20dB	-	2	3	μVrms
Total Harmonic Distortion	THD	V <sub>O</sub> =1Vrms, BW=400Hz to 30kHz	-	0.005	0.05	%
Common Mode Rejection Ratio (*)	CMRR	V <sub>ICM</sub> =1Vrms	70	80	-	dB
Supply Voltage Rejection Ratio	SVR	f=100Hz, V <sub>ripple</sub> =100mVrms	55	65	-	dB

Note (\*):

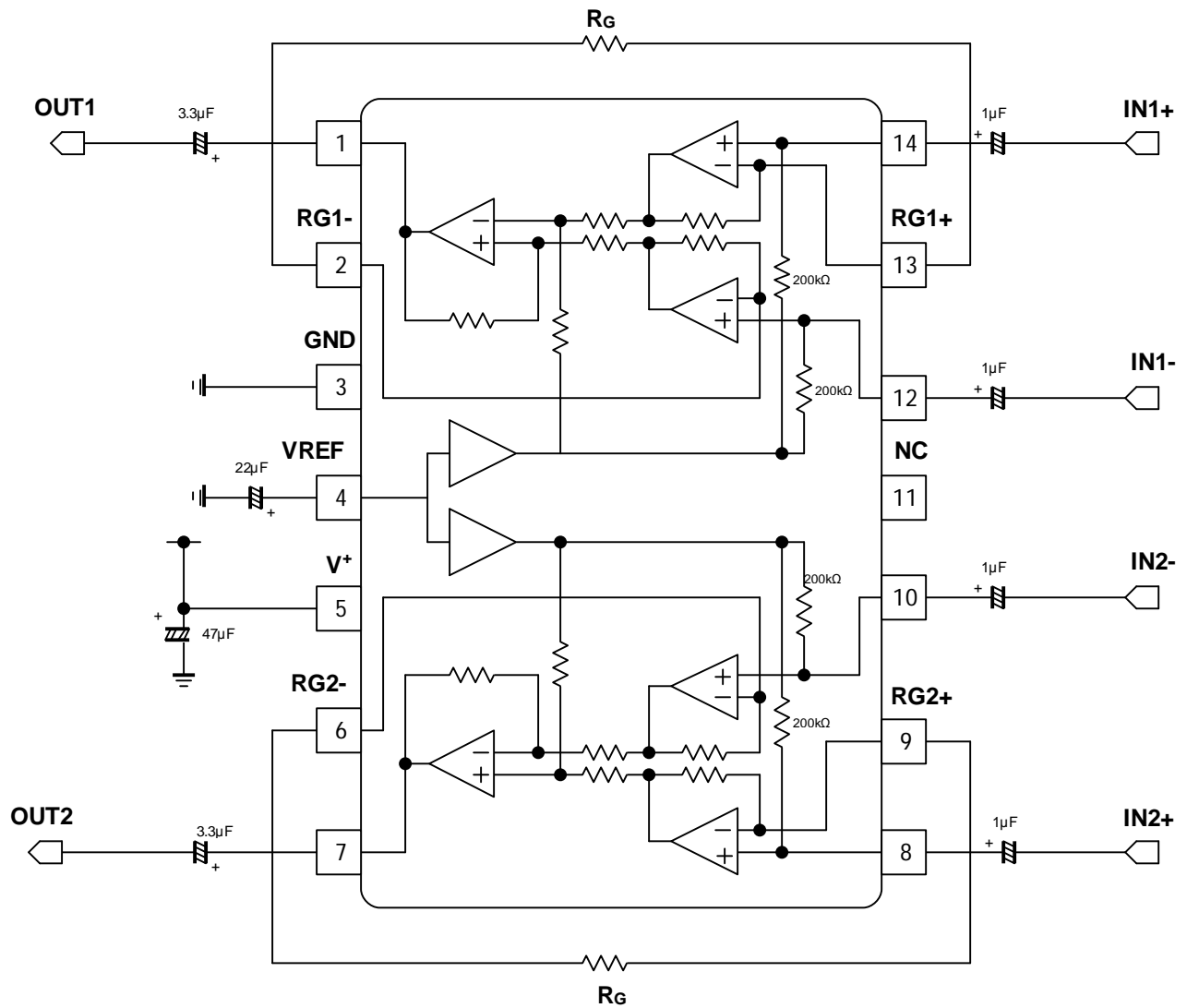
$$CMRR = \frac{G_{V2}}{G_{VCM}}, \text{ Where } G_{V2} \text{ is the Differential Mode Gain and } G_{VCM} \text{ is the Common Mode Gain.}$$

$$G_{VCM} = 20 * \log \left( \frac{V_{OCM}}{V_{ICM}} \right), \text{ Where } V_{OCM} \text{ is the Common Mode Output and } V_{ICM} \text{ is the Common Mode Input.}$$

■ TERMINAL DESCRIPTION

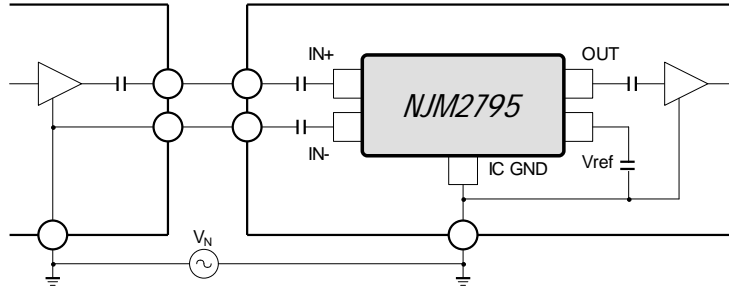
PIN NO.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	TERMINAL DC VOLTAGE
1 7	OUT1 OUT2	Output1 Output2		$V^+ \times 0.5$
2 6 9 13	RG1- RG2- RG2+ RG1+	Gain Adjustment 1- Gain Adjustment 2- Gain Adjustment 2+ Gain Adjustment 1+		$V^+ \times 0.5$
8 10 12 14	IN2+ IN2- IN1- IN1+	+Input2 -Input2 -Input1 +Input1		$V^+ \times 0.5$
4	VREF	Reference Voltage		$V^+ \times 0.5$

## APPLICATION CIRCUIT

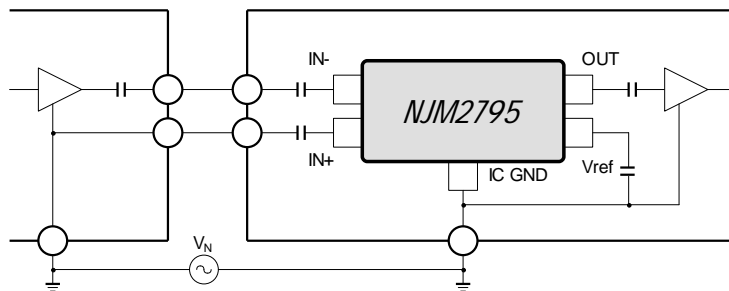


■ APPLICATION BLOCK DIAGRAM

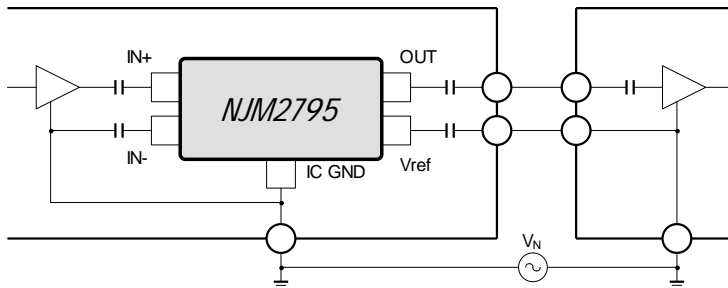
(1) Non-inverting line input



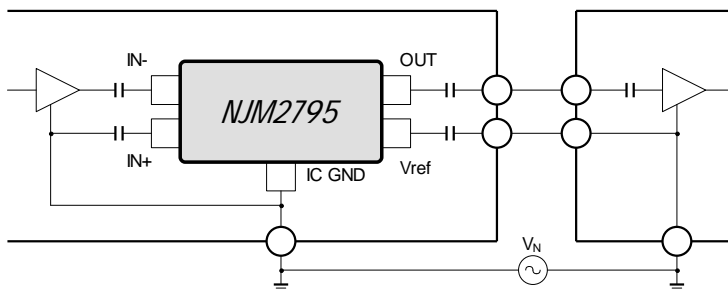
(2) Inverting line input



(3) Non-inverting line output



(4) Inverting line output



[CAUTION]  
 The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.