

**FEATURES**

- LIN 2.x/ISO 17987-4:2016 (12V)/SAE J2602 compliant
- Thermally protected
- AEC-Q100 qualified
- Transmit data (TXD) dominant time-out function
- Bus terminal current limit protected
- Under voltage on battery
- Very low current consumption in Sleep mode
- Support local and remote wake-up
- Enable an external high voltage regulator by INH
- Baud rates up to 20 kBd
- Very low ElectroMagnetic Emission (EME)
- High ElectroMagnetic Immunity (EMI)
- Available in SOP8 and DFN3\*3-8/HVSON8 packages

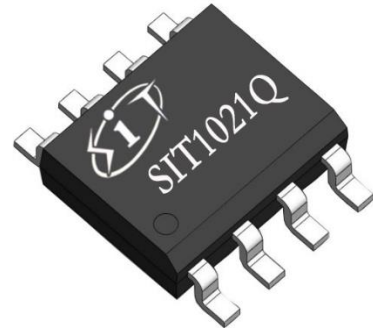
**PRODUCT APPEARANCE**

Fig 1. Provide green and environmentally friendly lead-free package

**DESCRIPTION**

The SIT1021Q is a physical layer transceiver of Local Interconnect Network (LIN). It is compliant with LIN 2.0/LIN 2.1/LIN 2.2/LIN 2.2A/ISO 17987-4:2016 (12V) and SAE J2602 standards. It is typically used for low speed in-vehicle networks using baud rates from 1 kBd to 20 kBd. The LIN protocol data stream at the transmit data input (TXD) is converted by the SIT1021Q into a bus signal with optimized wave shaping to minimize ElectroMagnetic Emission (EME). The SIT1021Q converts the data stream on LIN bus to logic level signals that are sent to the microprocessor via the pin RXD. The LIN bus is pulled high by the internal slave resistor and a series diode. Master applications require an external pull-up resistor in series with a diode to connect pin VBAT and pin LIN.

The SIT1021Q has an extremely low current consumption in sleep mode. The power consumption is reduced to a minimum if in failure modes. It also provides a high voltage output pin INH to enable an external high voltage regulator which is used to support the microprocessor.

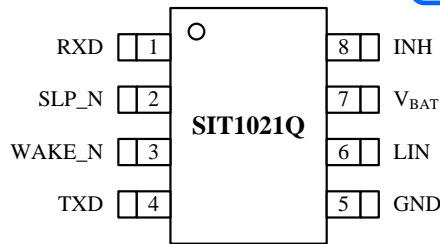
**PIN CONFIGURATION**


Fig 2. SIT1021Q pin configuration diagrams

**PIN DESCRIPTION**

Table 1. Pin description

Pin	Symbol	Description
1	RXD	receive data output (open-drain); active LOW after a wake-up event
2	SLP_N	sleep control input (active LOW); controls inhibit output; resets wake-up source flag on TXD and wake-up request on RXD
3	WAKE_N	local wake-up input (active LOW); negative edge triggered
4	TXD	transmit data input; active LOW output after a local wake-up event
5	GND	ground
6	LIN	LIN bus line input/output
7	V <sub>BAT</sub>	battery supply voltage
8	INH	battery related inhibit output for controlling an external voltage regulator; active HIGH after a wake-up event

NOTE: The exposed center pad of the DFN3\*3-8/HVSON8 package is internal connected to the GND pin of the chip. For enhanced thermal performance, the exposed center pad of the DFN3\*3-8/HVSON8 package could be soldered to board ground.

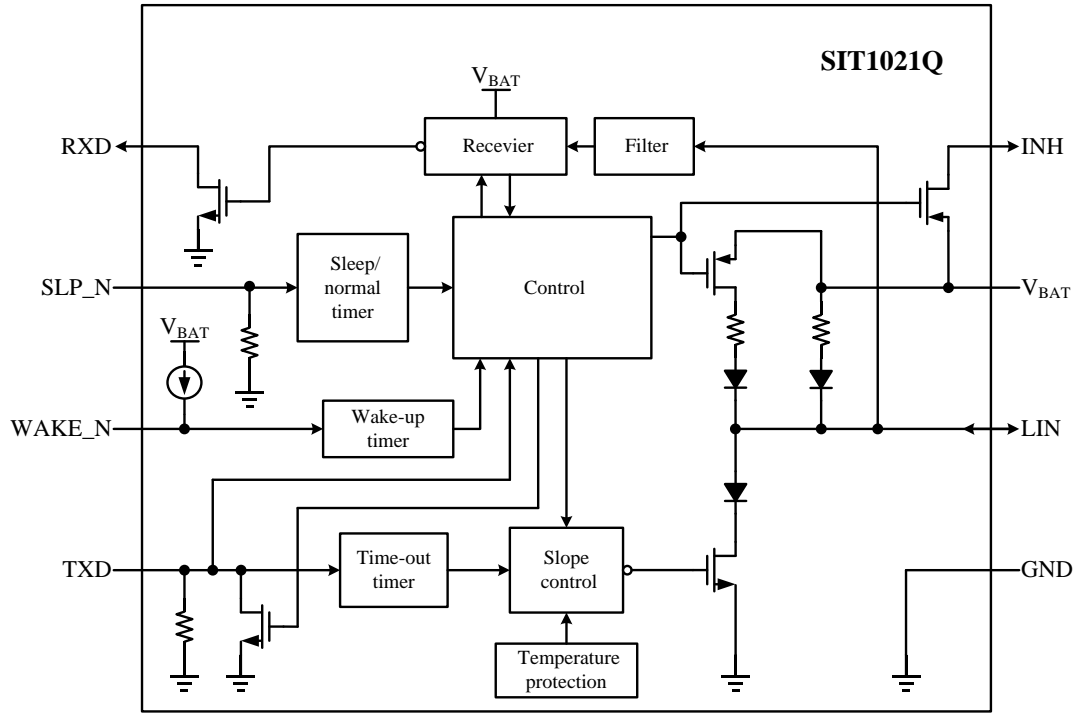


Fig 3. Block diagram

**FEATURE DESCRIPTION**

## 1 Overview

The SIT1021Q is an interface device used between the LIN protocol controller and the physical bus. It can be used in trucks, buses, cars and industrial control with a data rate up to 20kBd. The SIT1021Q receives the data stream sent by protocol controller at the pin TXD, and converts it into a bus signal with appropriate slew rate and waveform shaping. The input data on LIN bus is output to external microcontroller by pin RXD. This device is compliant with LIN 2.0/LIN 2.1/LIN 2.2/LIN 2.2A/ISO 17987-4:2016 (12V) and SAE J2602 standards.

## 2 Short-circuit protection

Pin TXD provides an internal pull-down to GND to apply a predefined level on TXD when it is not enabled. The pin SLP\_N also provides an internal pull-down to force the transceiver to enter sleep mode when SLP\_N is not enabled.

Pin RXD will be left floating and limit the output current of transmitter to prevent a short-circuit between LIN and VBAT or GND if the supply on pin VBAT is turned off. There is no reverse current at the bus terminal, and the connection between LIN supply can be shut off without affecting the bus.

## 3 Thermal Shutdown

In normal mode, the over-temperature protection circuit will disable the output driver when the junction temperature of SIT1021Q exceeds the shutdown junction temperature  $T_{j(sd)}$ . The driver is enabled again when the junction temperature has dropped below  $T_{j(sd)}$  and a recessive level is present at pin TXD.

## 4 TXD dominant time-out function

A TXD dominant time-out timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD. If the duration of the LOW level on pin TXD exceeds the internal timer value ( $t_{dom}$ ), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD.

## 5 Operating modes

As shown in Fig 4, the SIT1021Q supports four functional modes for normal operation (Normal mode), power-up (Power-on mode), standby operation (Standby mode) and very-low-power operation (Sleep mode). The operating states in each mode are shown in Table 2.

**Sleep mode:** This mode is the lowest power consumption mode of the SIT1021Q. It can be woken up remotely via pin LIN, or woken up locally via pin WAKE\_N, or activated directly via pin SLP\_N. The pin WAKE\_N, pin SLP\_N and pin LIN are filtered to prevent accidental wake up events. The wake-up events for SIT1021Q in sleep mode is: the remote wake up time via pin LIN must be longer than  $t_{\text{wake}(\text{dom})\text{LIN}}$ ; the local wake up time via pin WAKE\_N must be longer than  $t_{\text{wake}(\text{dom})\text{WAKE\_N}}$ ; the time wake up directly via pin SLP\_N must be longer than  $t_{\text{gotonorm}}$ .

Sleep mode is only entered when the pin SLP\_N is low and from normal mode. To enter Sleep mode successfully (INH becomes floating), the sleep command (SLP\_N = 0) must be maintained for at least  $t_{\text{gotosleep}}$ . The pin INH is only floating in sleep mode and going into high in others modes.

**Standby mode:** It is entered whenever a local or remote wake-up occurs while the device is in Sleep mode. Standby mode is signaled through a low level on pin RXD. The pin INH will be set high and activate the external voltage regulator and the microcontroller after the device enters standby mode from sleep mode.

Setting pin SLP\_N high during Standby mode results in the following events:

- (1) An immediate reset of the wake-up source flag; thus releasing the possible strong pull-down at pin TXD before the actual mode change (after  $t_{\text{gotonorm}}$ ) is performed.
- (2) A change into Normal mode if the high level on pin SLP\_N has been maintained for a certain time period ( $t_{\text{gotonorm}}$ ).
- (3) An immediate reset of the wake-up request signal on pin RXD.

**Normal mode:** Only in Normal mode the receiver and transmitter are active and the SIT1021Q is able to transmit and receive data via the LIN bus. The high level of bus represents recessive and low level represents dominant. The receiver detects the data stream on the LIN bus and outputs it to the microcontroller via pin RXD. Normal mode is entered as a high level on pin SLP\_N and maintained for a time of at least  $t_{\text{gotonorm}}$  while the SIT1021Q is in Sleep, Power-up or Standby mode. The Sleep mode is entered by setting pin SLP\_N low for longer than  $t_{\text{gotosleep}}$ .

**Power-on mode:** When SIT1021Q is in Power-on mode: pin RXD is left floating, pin TXD is weakly pulled down, transmitter and receiver are not activated. If the pin SLP\_N is high at power up the device will be powered up in normal mode and if low it will be powered up in Standby mode.

## 6 Wake-up source recognition

In Sleep mode, SIT1021Q can be woken up remotely via the LIN bus or be woken up locally via the pin WAKE\_N. The wake-up source flag can be read by detecting the state of pin TXD in the Standby mode. If an external pull-up resistor on pin TXD to the power supply voltage of the microcontroller has been added, a high level indicates a remote wake-up request (weak pull-down at pin TXD) and a LOW level indicates a local wake-up request (strong pull-down at pin TXD; much stronger than the external pull-up resistor). The

wake-up request flag (signaled on pin RXD) as well as the wake-up source flag (signaled on pin TXD) are reset immediately after the microcontroller sets pin SLP\_N high.

## 7 Wake Up Events

In sleep mode, the device can be woken up by the following three ways:

- (1) Remote wake-up via pin LIN;
- (2) Local wake-up via pin WAKE\_N;
- (3) Wake up directly via pin SLP\_N.

## 8 Remote and local wake-up

Remote wake-up on the pin LIN: When A falling edge at pin LIN followed by a low level maintained longer than  $t_{wake(dom)LIN}$  and a rising edge at pin LIN respectively, the process is regarded as a valid remote wake-up event (see Fig 5).

Local wake-up on the pin WAKE\_N: When A falling edge at pin LIN followed by a low level maintained longer than  $t_{wake(dom)WAKE\_N}$ , the process is regarded as a valid remote wake-up event. The pin WAKE\_N provides an internal pull-up path to VBAT. To prevent EMI issues, it is recommended to connect the unused pin WAKE\_N to VBAT.

When a local or remote wake-up occurs, pin INH is activated (turns to high) and the internal slave termination resistor is turned on. The wake-up request is indicated by a low active wake-up request signal on pin RXD to interrupt the microcontroller.

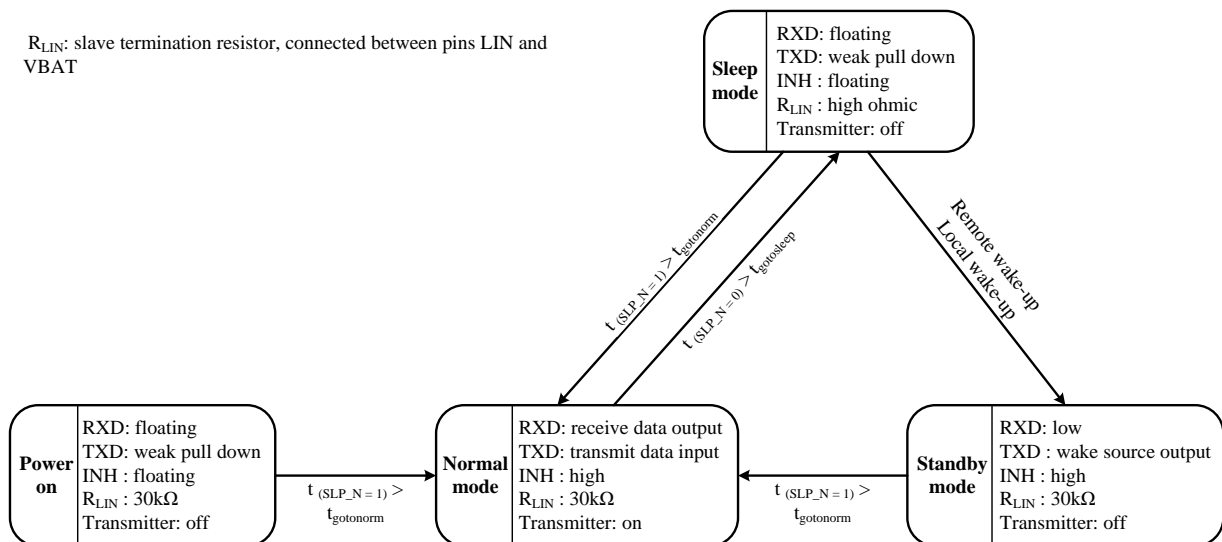


Fig 4. State diagram

Table 2. Operating modes

Mode	SLP_N	TXD	RXD	INH	Transmitter	Remarks
Sleep	low	weak pull-down	floating	floating	off	no wake-up request detected
Standby	low	weak pull-down if remote wake-up; strong pull-down if local wake-up	low	high	off	wake-up request detected; in this mode the microcontroller can read the wake-up source: remote or local wake-up
Normal	high	recessive: high dominant: low	recessive: high dominant: low	high	on	
Power-on	low	weak pull-down	floating	high	off	

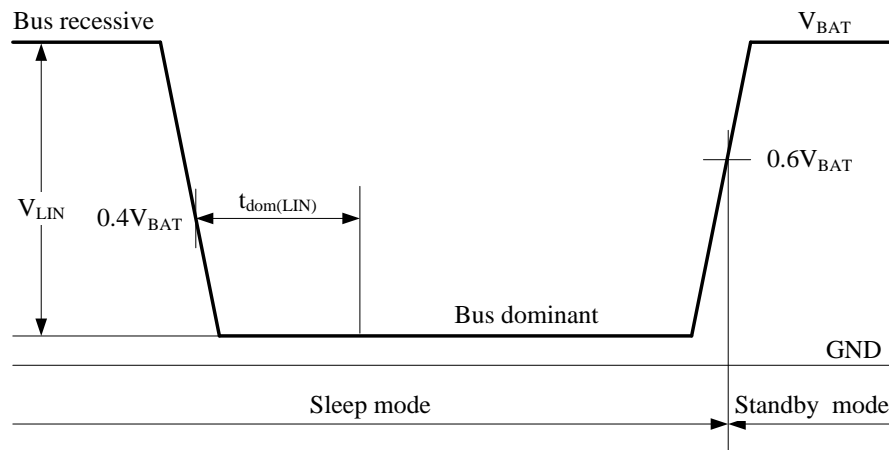


Fig 5. Remote wake-up behavior

**LIMITING VALUES**

Parameter	Symbol	Conditions	Range	Unit
battery supply voltage	V <sub>BAT</sub>	with respect to GND	-0.3 ~ +42	V
voltage on pin TXD	V <sub>TXD</sub>	I <sub>SLP_N</sub> no limitation	-0.3 ~ +6	V
		I <sub>SLP_N</sub> < 500μA	-0.3 ~ +7	
voltage on pin RXD	V <sub>RXD</sub>	I <sub>SLP_N</sub> no limitation	-0.3 ~ +6	V
		I <sub>SLP_N</sub> < 500μA	-0.3 ~ +7	
voltage on pin SLP_N	V <sub>SLP_N</sub>	I <sub>SLP_N</sub> no limitation	-0.3 ~ +6	V
		I <sub>SLP_N</sub> < 500μA	-0.3 ~ +7	
voltage on pin LIN	V <sub>LIN</sub>	with respect to GND	-42 ~ +42	V
voltage on pin WAKE_N	V <sub>WAKE_N</sub>		-0.3 ~ +42	V
voltage on pin INH	V <sub>INH</sub>		-0.3 ~ V <sub>BAT</sub> +0.3	V
virtual junction temperature	T <sub>j</sub>		-40 ~ 150	°C
storage temperature	T <sub>stg</sub>		-55 ~ 150	°C
ESD, human body model	V <sub>ESD</sub>	On pins WAKE_N, LIN, VBAT and INH	-8 ~ +8	kV
		On pins RXD, SLP_N and TXD	-2 ~ +2	kV
All pins		-750 ~ +750	V	
All pins		-200 ~ +200	V	
ESD, IEC61000-4-2		On pins WAKE_N, LIN, VBAT and INH	-4 ~ +4	kV

The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.



**STATIC CHARACTERISTICS**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>Supply</b>						
battery supply current	$I_{BAT}$	Sleep mode; ( $V_{LIN}=V_{BAT}$ ; $V_{WAKE\_N}=V_{BAT}$ ; $V_{TXD}=0V$ ; $V_{SLP\_N}=0V$ )	1	3	15	$\mu A$
		Standby mode; bus recessive ( $V_{INH}=V_{BAT}$ ; $V_{LIN}=V_{BAT}$ ; $V_{WAKE\_N}=V_{BAT}$ ; $V_{TXD}=0V$ ; $V_{SLP\_N}=0V$ )	150	350	800	$\mu A$
		Standby mode; bus dominant ( $V_{BAT}=12V$ ; $V_{INH}=12V$ ; $V_{LIN}=0V$ ; $V_{WAKE\_N}=12V$ ; $V_{TXD}=0V$ ; $V_{SLP\_N}=0V$ )	500	750	1000	$\mu A$
		Normal mode; bus recessive ( $V_{INH}=V_{BAT}$ ; $V_{LIN}=V_{BAT}$ ; $V_{WAKE\_N}=V_{BAT}$ ; $V_{TXD}=5V$ ; $V_{SLP\_N}=5V$ )	200	380	600	$\mu A$
		Normal mode; bus dominant ( $V_{BAT}=12V$ ; $V_{INH}=12V$ ; $V_{WAKE\_N}=12V$ ; $V_{TXD}=0V$ ; $V_{SLP\_N}=5V$ )	0.5	1.4	3	mA
<b>Power-on reset</b>						
low-level $V_{BAT}$ reset threshold voltage	$V_{th}(V_{BATL})L$		3.9	4.4	4.7	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
high-level V <sub>BAT</sub> reset threshold voltage	V <sub>th</sub> (V <sub>BATL</sub> )H		4.2	4.7	5.1	V
V <sub>BAT</sub> reset hysteresis voltage	V <sub>hys</sub> (V <sub>BATL</sub> )		0.05	0.3	1	V
<b>Pin TXD</b>						
high-level input voltage	V <sub>IH</sub>		2		7	V
low-level input voltage	V <sub>IL</sub>		-0.3		+0.8	V
hysteresis voltage	V <sub>hys</sub>		50	200	400	mV
pull-down resistance on pin TXD	R <sub>PD</sub> (TXD)	V <sub>TXD</sub> =5V	140	500	1200	kΩ
low-level input current	I <sub>IL</sub>	V <sub>TXD</sub> =0V	-5		+5	μA
low-level output current	I <sub>OL</sub>	local wake-up request; Standby mode; V <sub>WAKE_N</sub> =0V; V <sub>LIN</sub> =V <sub>BAT</sub> ; V <sub>TXD</sub> =0.4V	1.5			mA
<b>Pin SLP_N</b>						
high-level input voltage	V <sub>IH</sub>		2		7	V
low-level input voltage	V <sub>IL</sub>		-0.3		0.8	V
hysteresis voltage	V <sub>hys</sub>		50	200	400	mV
pull-down resistance on pin SLP_N	R <sub>PD</sub> (SLP_N)	V <sub>SLP_N</sub> =5V	140	500	1200	kΩ
low-level input current	I <sub>IL</sub>	V <sub>SLP_N</sub> =0V	-5		5	μA
<b>Pin RXD</b>						
low-level output current	I <sub>OL</sub>	Normal mode; V <sub>RXD</sub> =0.4V; V <sub>LIN</sub> =0V	1.5			mA
high-level leakage current	I <sub>LH</sub>	Normal mode; V <sub>RXD</sub> =5V; V <sub>LIN</sub> =V <sub>BAT</sub>	-5		5	μA
<b>Pin WAKE_N</b>						

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
high-level input voltage	$V_{IH}$		$V_{BAT}-1$		$V_{BAT}+0.3$	V
low-level input voltage	$V_{IL}$		-0.3		$V_{BAT}-3.3$	V
low-level pull-up current	$I_{pu(L)}$	$V_{WAKE\_N}=0V$ ;	-30	-12	-1	$\mu A$
high-level leakage current	$I_{LH}$	$V_{WAKE\_N}=27V$ ; $V_{BAT}=27V$	-5		5	$\mu A$
<b>Pin INH</b>						
switch-on resistance between pins $V_{BAT}$ and INH	$R_{SW}$	Standby; Normal and Power-on mode; $I_{INH}=-15mA$ ; $V_{BAT}=12V$		20	50	$\Omega$
high-level leakage current	$I_{LH}$	Sleep mode; $V_{INH}=27V$ ; $V_{BAT}=27V$	-5		5	$\mu A$
<b>Pin LIN</b>						
current limitation for driver dominant state	$I_{BUS\_LIM}$	$V_{TXD}=0V$ ; $V_{LIN}=V_{BAT}=18V$	40		100	mA
pull-up resistance	$R_{pu}$	Sleep mode; $V_{SLP\_N}=0V$	50	160	250	k $\Omega$
receiver recessive input leakage current	$I_{BUS\_PAS\_rec}$	$V_{TXD}=5V$ ; $V_{LIN}=27V$ ; $V_{BAT}=5.5V$			10	$\mu A$
receiver dominant input leakage current including pull-up resistor	$I_{BUS\_PAS\_dom}$	Normal mode; $V_{TXD}=5V$ ; $V_{LIN}=0V$ ; $V_{BAT}=12V$	-1000			$\mu A$
loss-of-ground bus current	$I_{BUS\_NO\_GND}$	$V_{BAT}=27V$ ; $V_{LIN}=0V$	-1000		10	$\mu A$
loss-of-battery bus current	$I_{BUS\_NO\_BAT}$	$V_{BAT}=0V$ ; $V_{LIN}=27V$			10	$\mu A$
receiver dominant input voltage	$V_{th(dom)RX}$				$0.4V_{BAT}$	V
receiver recessive input voltage	$V_{th(rec)RX}$		$0.6V_{BAT}$			V
receiver center voltage	$V_{th(RX)cntr}$	$V_{th(RX)cntr} = (V_{th(rec)RX} + V_{th(dom)RX})/2$	$0.475V_{BAT}$	$0.5V_{BAT}$	$0.525V_{BAT}$	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
receiver hysteresis voltage	$V_{th(hys)RX}$	$V_{th(hys)RX} = V_{th(rec)RX} - V_{th(dom)RX}$			$0.175V_{BAT}$	V
slave resistance	$R_{slave}$	connected between pins LIN and $V_{BAT}$ ; $V_{LIN}=0V$ ; $V_{BAT}=12V$ ; $V_{TXD}=V_{SLP\_N}=5V$	20	30	60	k $\Omega$
capacitance on pin LIN	$C_{LIN}$				30	pF
dominant output voltage	$V_{o(dom)}$	Normal mode; $V_{TXD}=0V$ ; $V_{BAT}=7V$			1.4	V
		Normal mode; $V_{TXD}=0V$ ; $V_{BAT}=18V$			2.0	V
<b>Thermal shutdown</b>						
shutdown junction temperature	$T_{j(sd)}$		150	175	200	$^{\circ}C$

(Unless specified otherwise;  $5.5V \leq V_{BAT} \leq 27V$ ,  $-40^{\circ}C \leq T_j \leq 150^{\circ}C$ ; typical in  $V_{BAT}=12V$ ,  $T_j=25^{\circ}C$ .)

**DYNAMIC CHARACTERISTICS**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>Duty cycles</b>						
duty cycle 1	$\delta 1$ <sup>[1][2]</sup>	$V_{th(rec)(max)}=0.744 \times V_{BAT}$ ; $V_{th(dom)(max)}=0.581 \times V_{BAT}$ ; $t_{bit}=50\mu s$ ; $V_{BAT}=7V \sim 18V$ Fig 6	0.396			
		$V_{th(rec)(max)}=0.76 \times V_{BAT}$ ; $V_{th(dom)(max)}=0.593 \times V_{BAT}$ ; $t_{bit}=50\mu s$ ; $V_{BAT}=5.5V \sim 7V$ Fig 6	0.396			
duty cycle 2	$\delta 2$ <sup>[2][3]</sup>	$V_{th(rec)(min)}=0.422 \times V_{BAT}$ ; $V_{th(dom)(min)}=0.284 \times V_{BAT}$ ; $t_{bit}=50\mu s$ ; $V_{BAT}=7.6V \sim 18V$ Fig 6			0.581	
		$V_{th(rec)(min)}=0.41 \times V_{BAT}$ ; $V_{th(dom)(min)}=0.275 \times V_{BAT}$ ; $t_{bit}=50\mu s$ ; $V_{BAT}=6.1V \sim 7.6V$ Fig 6			0.581	
duty cycle 3	$\delta 3$ <sup>[1][2]</sup>	$V_{th(rec)(max)}=0.778 \times V_{BAT}$ ; $V_{th(dom)(max)}=0.616 \times V_{BAT}$ ; $t_{bit}=96\mu s$ ; $V_{BAT}=7V \sim 18V$ Fig 6	0.417			
		$V_{th(rec)(max)}=0.797 \times V_{BAT}$ ; $V_{th(dom)(max)}=0.630 \times V_{BAT}$ ; $t_{bit}=96\mu s$ ; $V_{BAT}=5.5V \sim 7V$ Fig 6	0.417			
duty cycle 4	$\delta 4$ <sup>[2][3]</sup>	$V_{th(rec)(min)}=0.389 \times V_{BAT}$ ; $V_{th(dom)(min)}=0.251 \times V_{BAT}$ ; $t_{bit}=96\mu s$ ; $V_{BAT}=7.6V \sim 18V$ Fig 6			0.590	
		$V_{th(rec)(min)}=0.378 \times V_{BAT}$ ; $V_{th(dom)(min)}=0.242 \times V_{BAT}$ ; $t_{bit}=96\mu s$ ; $V_{BAT}=6.1V \sim 7.6V$ Fig 6			0.590	
<b>Timing characteristics</b>						
receiver propagation delay	$t_{PD(RX)}$ <sup>[4]</sup>				6	$\mu s$
receiver propagation	$t_{PD(RX)sym}$ <sup>[4]</sup>		-2		2	$\mu s$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
delay symmetry						
LIN dominant wake-up time	$t_{\text{wake(dom)LIN}}$	Sleep mode	30	65	150	$\mu\text{s}$
dominant wake-up time on pin WAKE_N	$t_{\text{wake(dom)WAKE\_N}}$	Sleep mode	7	22	50	$\mu\text{s}$
go to normal time	$t_{\text{gotonorm}}$		2	5	10	$\mu\text{s}$
go to sleep time	$t_{\text{gotosleep}}$		2	5	10	$\mu\text{s}$
TXD dominant time-out time	$t_{\text{to(dom)TXD}}$	$V_{\text{TXD}}=0\text{V}$	27	52	90	ms

(Unless specified otherwise;  $5.5\text{V} \leq V_{\text{BAT}} \leq 27\text{V}$ ,  $-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$ ; typical in  $V_{\text{BAT}}=12\text{V}$ ,  $T_j=25^\circ\text{C}$ .)

$$[1] \quad \delta 1, \delta 3 = \frac{t_{\text{bus(rec)(min)}}}{2 \times t_{\text{bit}}}$$

[2] Bus load conditions are: (1)  $C_L=1\text{nF}$ ,  $R_L=1\text{k}\Omega$ ; (2)  $C_L=6.8\text{nF}$ ,  $R_L=660\Omega$ ; (3)  $C_L=10\text{nF}$ ,  $R_L=500\Omega$

$$[3] \quad \delta 2, \delta 4 = \frac{t_{\text{bus(rec)(max)}}}{2 \times t_{\text{bit}}}$$

[4] Load condition pin RXD:  $C_{\text{TXD}}=20\text{pF}$ ,  $R_{\text{RXD}}=2.4\text{k}\Omega$

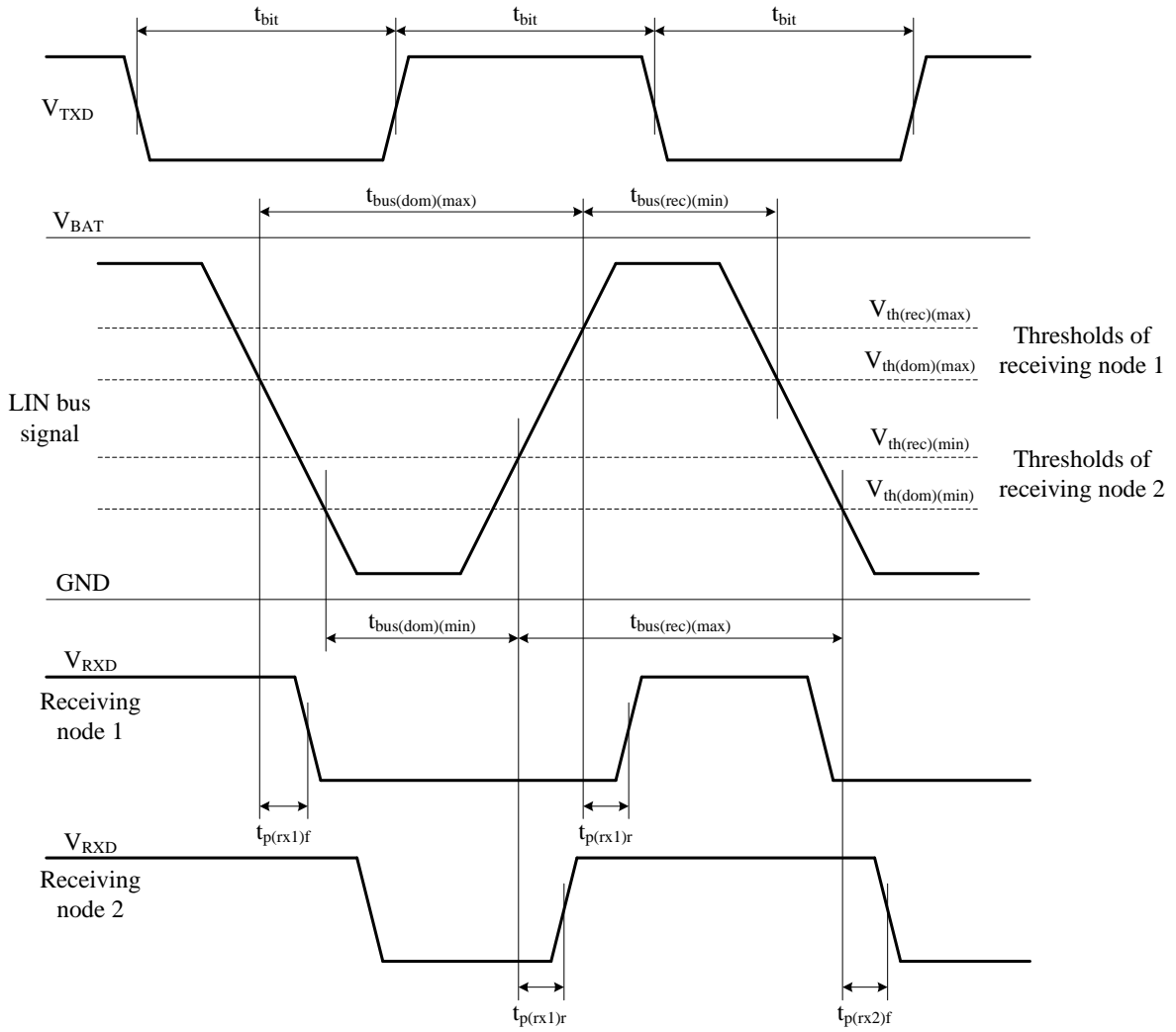


Fig 6. Timing diagram LIN transceiver

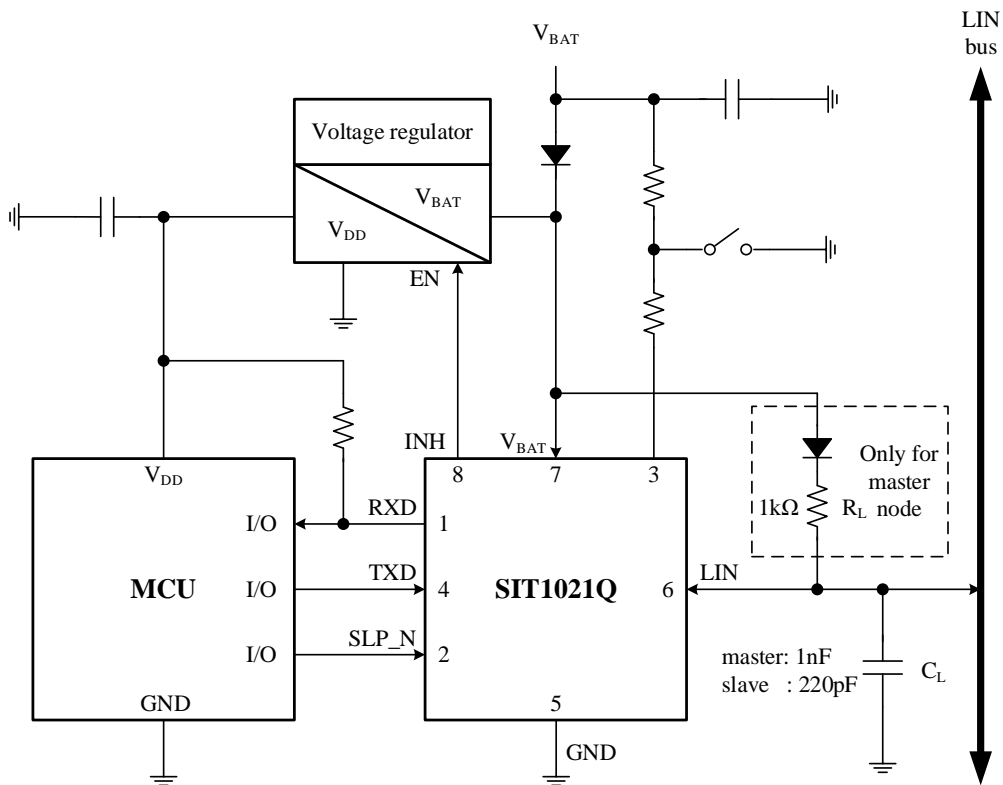
**TYPICAL APPLICATION**


Fig 7. Typical application of the SIT1021Q

 Note: To obtain a slower bus waveform slope, it is recommended to use a  $R_L/C_L$  combination of  $660\Omega/6.8nF$ .

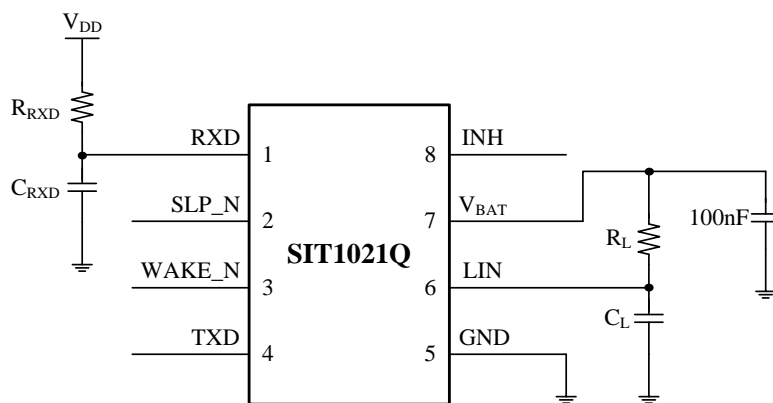
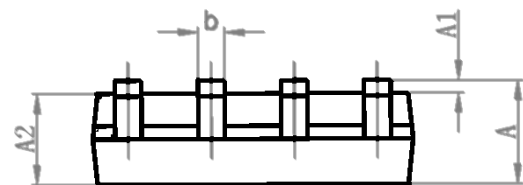
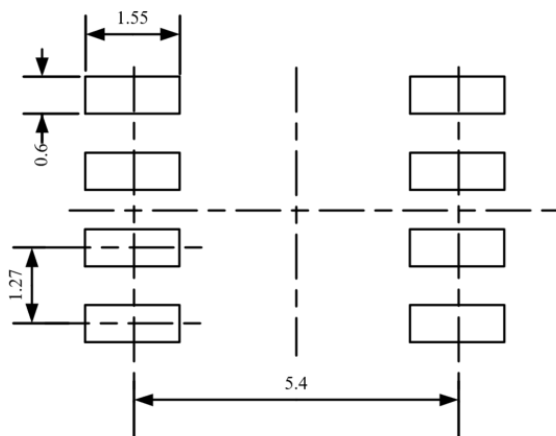
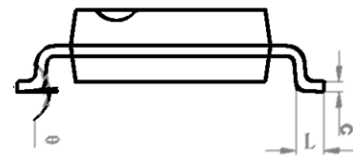
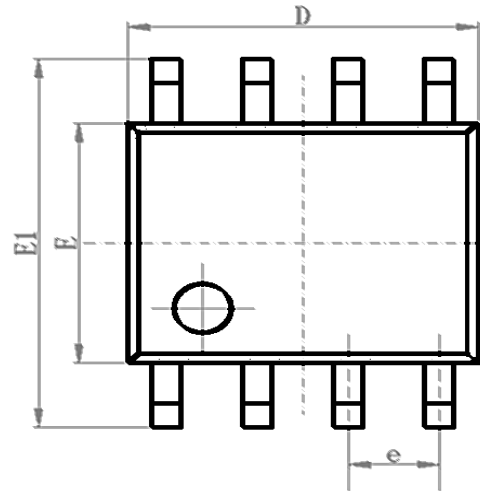
**TIMING TEST CIRCUIT**


Fig 8. Timing test circuit for LIN transceiver



**SOP8 DIMENSIONS**
**PACKAGE SIZE**

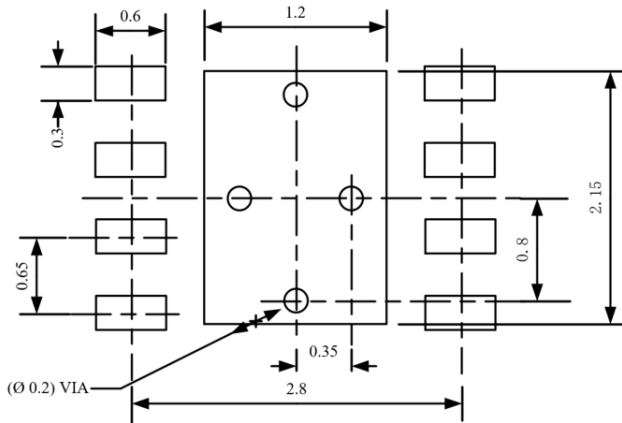
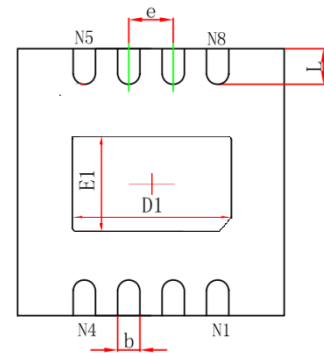
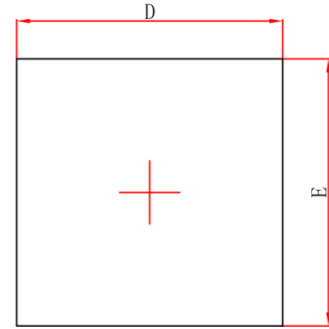
SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	1.40	-	1.80
A1	0.10	-	0.25
A2	1.30	1.40	1.50
b	0.38	-	0.51
D	4.80	4.90	5.00
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
e		1.27BSC	
L	0.40	0.60	0.80
c	0.20	-	0.25
$\theta$	0°	-	8°



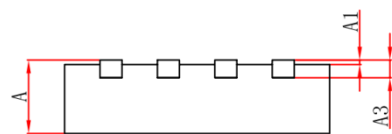
LAND PATTERN EXAMPLE (Unit: mm)

**DFN3\*3-8/HVSON8 DIMENSIONS**
**PACKAGE SIZE**

SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.203 REF		
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D1	2.05	2.15	2.25
E1	1.10	1.20	1.30
b	0.25	0.30	0.35
e	0.65 TYP		
L	0.35	0.4	0.45



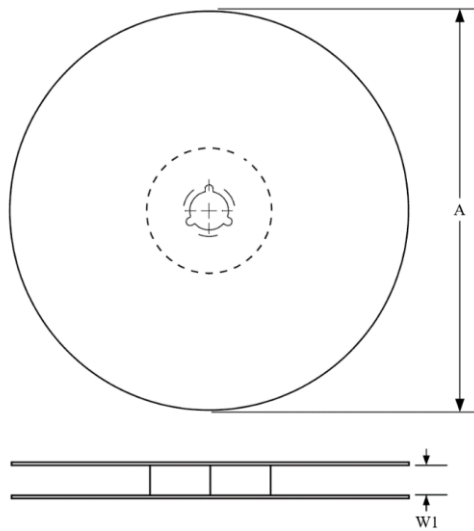
LAND PATTERN EXAMPLE (Unit: mm)



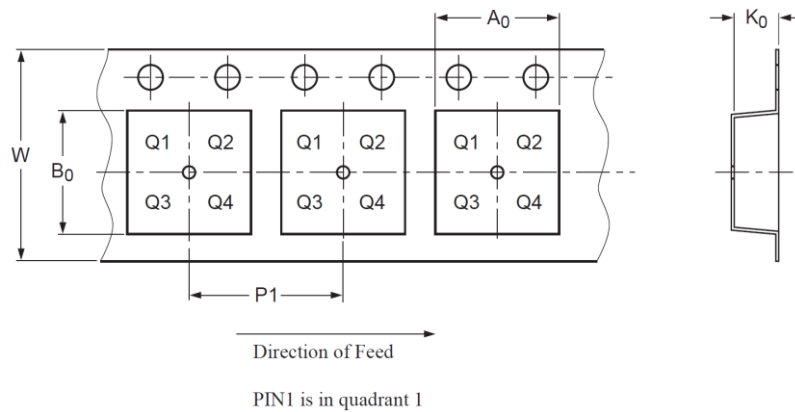
**ORDERING INFORMATION**

TYPE NUMBER	PACKAGE	PACKING
SIT1021QT	SOP8	Tape and reel
SIT1021QTK	DFN3*3-8/HVSON8, Small outline package, no leads	Tape and reel

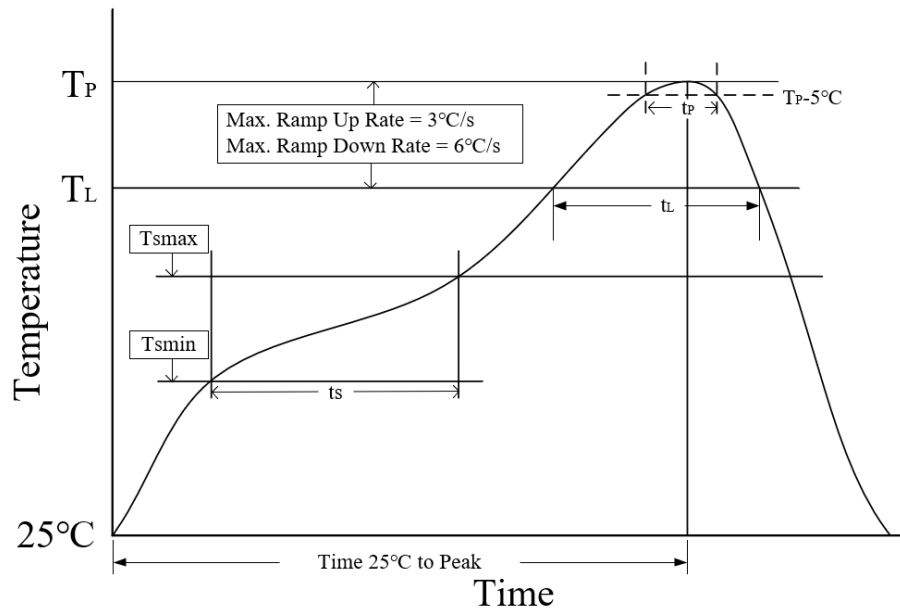
SOP8 is packed with 2500 pieces/disc in braided packaging. Leadless DFN3\*3-8/HVSON8 is packed with 6000 pieces/disc in braided packaging.

**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Package type	Reel diameter A (mm)	Tape width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
SOP8	330±1	12.4	6.60±0.1	5.30±0.10	1.90±0.1	8.00±0.1	12.00±0.1
DFN3*3-8	329±1	12.4	3.30±0.1	3.30±0.1	1.10±0.1	8.00±0.1	12.00±0.3

**REFLOW SOLDERING**


Parameter	Lead-free soldering conditions
Ave ramp up rate ( $T_L$ to $T_P$ )	3 °C/second max
Preheat time $t_s$ ( $T_{smin}=150\text{ °C}$ to $T_{smax}=200\text{ °C}$ )	60-120 seconds
Melting time $t_L$ ( $T_L=217\text{ °C}$ )	60-150 seconds
Peak temp $T_P$	260-265 °C
5°C below peak temperature $t_p$	30 seconds
Ave cooling rate ( $T_P$ to $T_L$ )	6 °C/second max
Normal temperature 25°C to peak temperature $T_P$ time	8 minutes max

**Important statement**

SIT reserves the right to change the above-mentioned information without prior notice.

**REVISION HISTORY**

Version number	Data sheet status	Revision Date
V1.0	Initial version	April 2022
V1.1	Add AEC-Q100 qualified; Add ESD limiting parameters.	September 2022