



1N65Q-TA

Power MOSFET

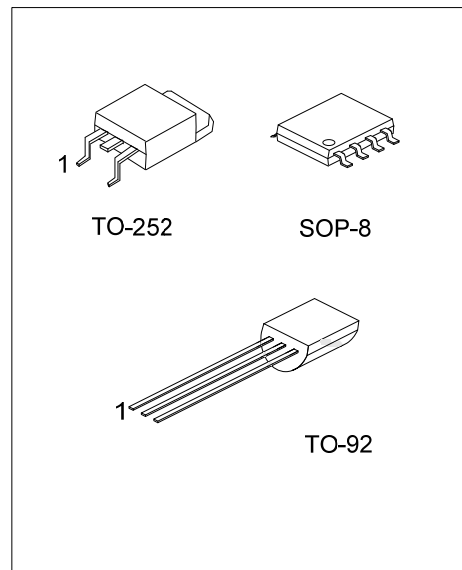
1.0A, 650V N-CHANNEL POWER MOSFET

DESCRIPTION

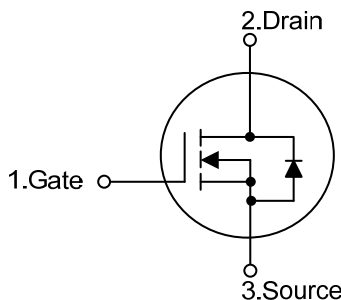
The UTC **1N65Q-TA** is a high voltage MOSFET and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and have a high rugged avalanche characteristics. This power MOSFET is usually used at high speed switching applications in power supplies, PWM motor controls, high efficient AC to DC converters and bridge circuits.

FEATURES

- * $R_{DS(ON)} \leq 9.5 \Omega @ V_{GS}=10V, I_D=0.5A$
- * Fast switching capability
- * Avalanche energy specified
- * Improved dv/dt capability, high ruggedness



SYMBOL



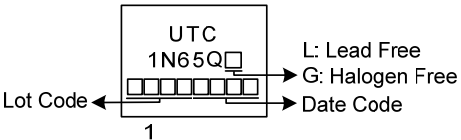
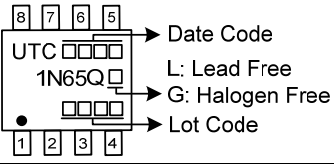
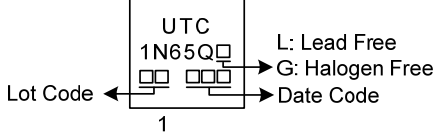
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
1N65QL-TN3-R	1N65QG-TN3-R	TO-252	G	D	S	Tape Reel
1N65QL-S08-R	1N65QG-S08-R	SOP-8	G	D	S	Tape Reel
1N65QL-T92-B	1N65QG-T92-B	TO-92	G	D	S	Tape Box
1N65QL-T92-K	1N65QG-T92-K	TO-92	G	D	S	Bulk

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>1N65QG-TN3-R</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) R: Tape Reel, B: Tape Box, K: Bulk</p> <p>(2) TN3: TO-252, S08: SOP-8, T92: TO-92</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ MARKING

PACKAGE	MARKING
TO-252	 <p>The diagram shows a TO-252 package with the following marking layout: <ul style="list-style-type: none"> Top: UTC Below UTC: 1N65Q□ Below 1N65Q□: Lot Code (indicated by an arrow pointing left) Below Lot Code: 1 Bottom right: Date Code (indicated by an arrow pointing right) Far right: L: Lead Free (indicated by an arrow pointing right) Below L: G: Halogen Free (indicated by an arrow pointing right) </p>
SOP-8	 <p>The diagram shows an SOP-8 package with the following marking layout: <ul style="list-style-type: none"> Top: UTC Below UTC: □□□□ (Date Code, indicated by arrows pointing right to positions 8, 7, 6, 5) Below Date Code: 1N65Q□ Below 1N65Q□: L: Lead Free (indicated by an arrow pointing right) Below L: G: Halogen Free (indicated by an arrow pointing right) Bottom right: Lot Code (indicated by an arrow pointing right) Bottom: □□□□ (Lot Code, indicated by an arrow pointing right to positions 1, 2, 3, 4) </p>
TO-92	 <p>The diagram shows a TO-92 package with the following marking layout: <ul style="list-style-type: none"> Top: UTC Below UTC: 1N65Q□ Below 1N65Q□: Lot Code (indicated by an arrow pointing left) Below Lot Code: 1 Bottom right: Date Code (indicated by an arrow pointing right) Far right: L: Lead Free (indicated by an arrow pointing right) Below L: G: Halogen Free (indicated by an arrow pointing right) </p>

■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	650	V
Gate-Source Voltage		V_{GSS}	± 30	V
Continuous Drain Current	Continuous	I_D	1.0	A
Pulsed Drain Current (Note 2)	Pulsed (Note 2)	I_{DM}	4.0	A
Avalanche Current (Note 2)		I_{AR}	1.0	A
Avalanche Energy (Note 3)	Single Pulsed	E_{AS}	50	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	4.1	V/ns
Power Dissipation	TO-252	P_D	26	W
	SOP-8		2.1	W
	TO-92		1.42	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L=100\text{mH}$, $I_{AS}=1.0\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\ \Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD}\leq 1.0\text{A}$, $di/dt\leq 200\text{A}/\mu\text{s}$, $V_{DD}\leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL CHARACTERISTICS

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-252	θ_{JA}	110	$^\circ\text{C}/\text{W}$
	SOP-8		90 (Note)	$^\circ\text{C}/\text{W}$
	TO-92		160 (Note)	$^\circ\text{C}/\text{W}$
Junction to Case	TO-252	θ_{JC}	4.8 (Note)	$^\circ\text{C}/\text{W}$
	SOP-8		59.5 (Note)	$^\circ\text{C}/\text{W}$
	TO-92		88 (Note)	$^\circ\text{C}/\text{W}$

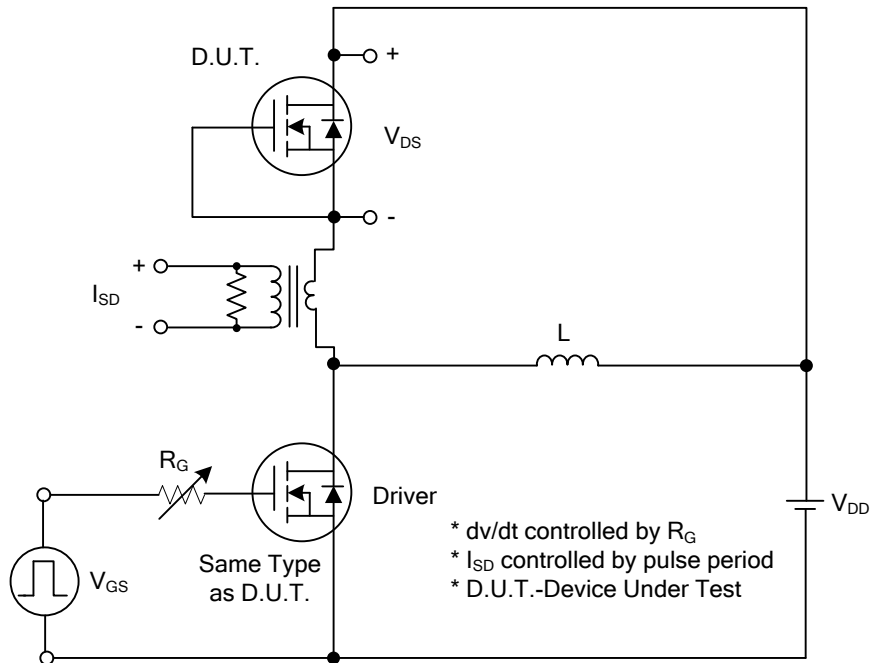
Note: The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

■ ELECTRICAL CHARACTERISTICS (T_C=25°C, unless otherwise specified)

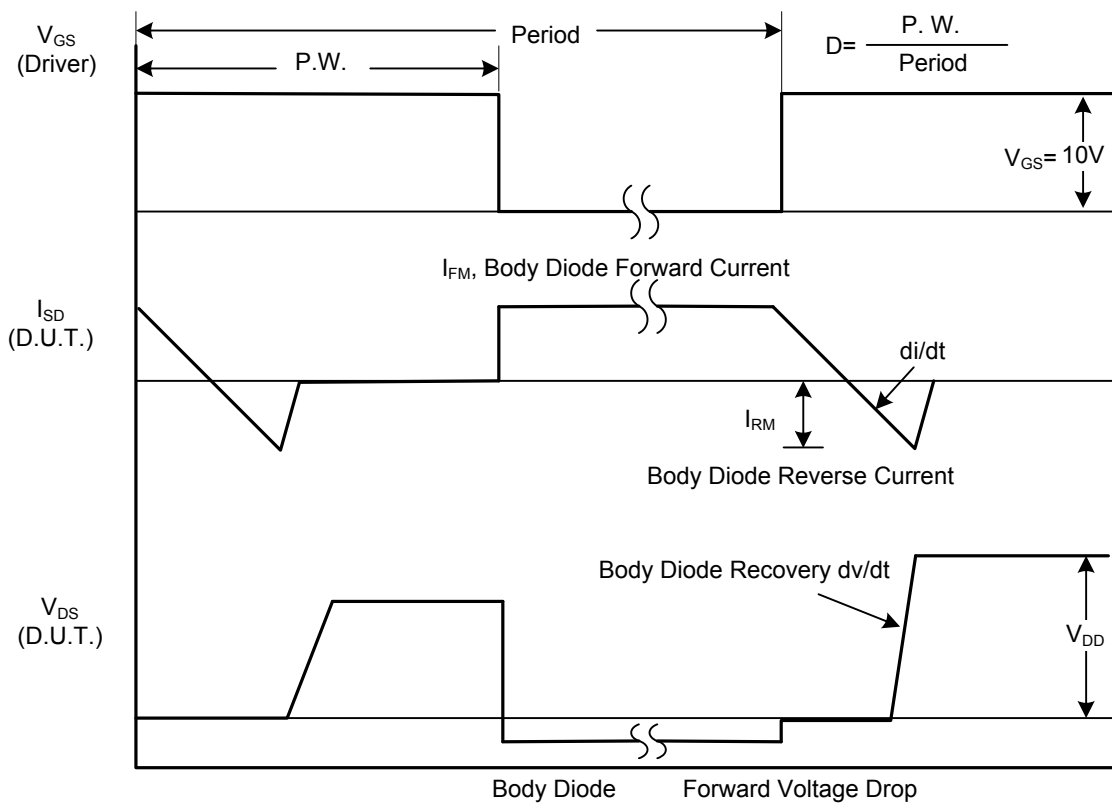
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250μA	650			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} = 650V, V _{GS} = 0V			10	μA
Gate-Source Leakage Current	Forward	I _{GSS}			100	nA
	Reverse				V _{GS} = 30V, V _{DS} = 0V	
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = 250μA	2.0		4.0	V
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 0.5A			9.5	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz		153		pF
Output Capacitance	C _{OSS}			20		pF
Reverse Transfer Capacitance	C _{RSS}			3.5		pF
SWITCHING CHARACTERISTICS						
Total Gate Charge	Q _G	V _{DS} = 50V, V _{GS} = 10V, I _D = 1.3A, I _G = 100μA (Note 1, 2)		14		nC
Gate-Source Charge	Q _{GS}			1.5		nC
Gate-Drain Charge	Q _{GD}			1		nC
Turn-On Delay Time	t _{D(ON)}	V _{DD} = 30V, V _{GS} = 10V, I _D = 0.5A, R _G = 25Ω (Note 1, 2)		23		ns
Turn-On Rise Time	t _R			25		ns
Turn-Off Delay Time	t _{D(OFF)}			60		ns
Turn-Off Fall Time	t _F			28		ns
DRAIN-SOURCE DIODE CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I _S				1	A
Maximum Body-Diode Pulsed Current	I _{SM}				4	A
Drain-Source Diode Forward Voltage	V _{SD}	V _{GS} = 0V, I _{SD} = 1.0A			1.4	V
Reverse Recovery Time	t _{rr}	I _F = 1.0A, V _{DD} = 100V		210		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs		460		nC

Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%
 2. Essentially independent of operating temperature

TEST CIRCUITS AND WAVEFORMS

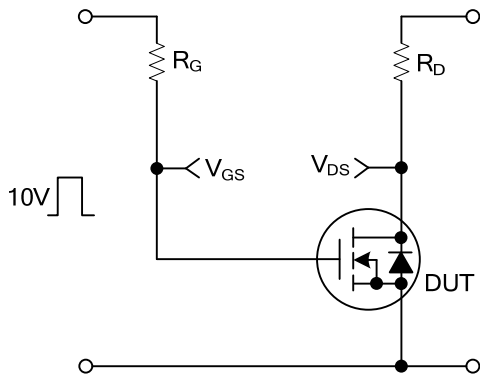


Peak Diode Recovery dv/dt Test Circuit

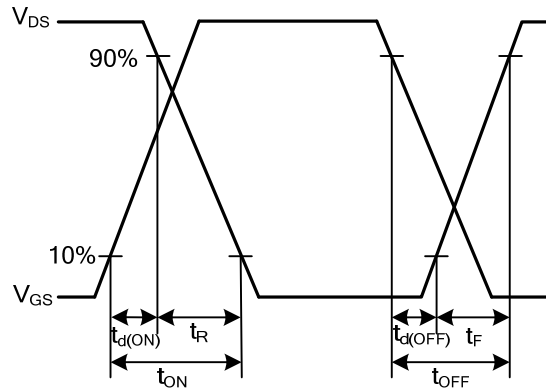


Peak Diode Recovery dv/dt Waveforms

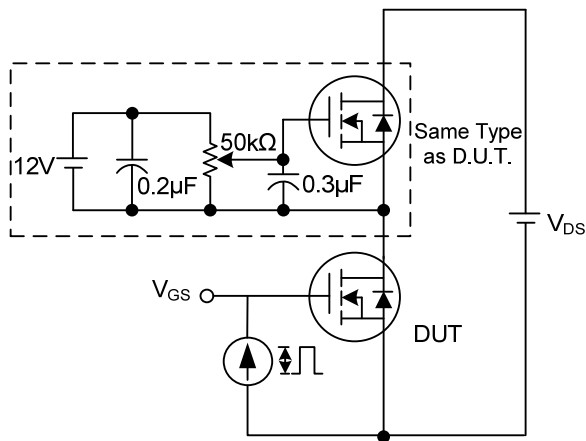
TEST CIRCUITS AND WAVEFORMS



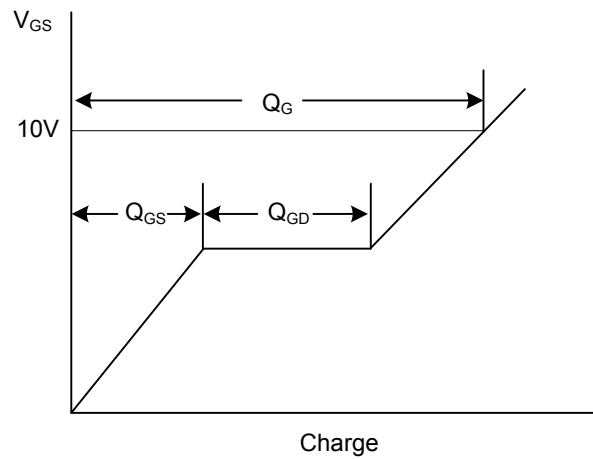
Switching Test Circuit



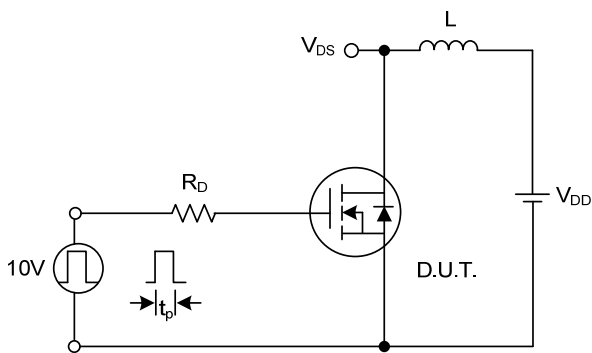
Switching Waveforms



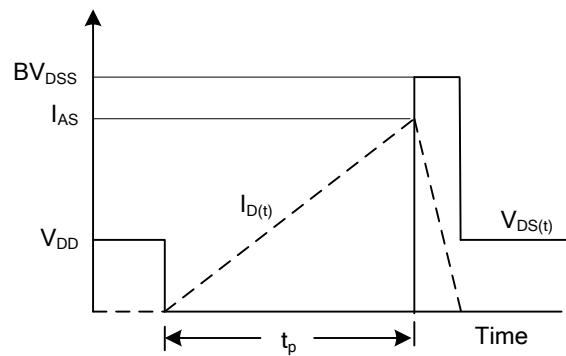
Gate Charge Test Circuit



Gate Charge Waveform

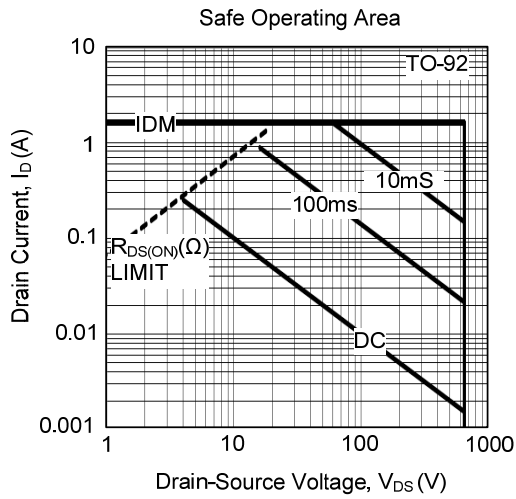


Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

■ TYPICAL CHARACTERISTICS



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