SPECIFICATION

PART NO. : OEL9M1018-Y-E

3.08 inch OLED
20x2 characters
with 6x8 dots

This specification maybe changed without any notice in order to improve performance or quality etc.
Please contact TRULY Semiconductors LTD. OLED R&D department for update specification and product status before design for this product or release the order.

PRODUCT CONTENTS

TRULY®信利		Customer	
Written by	Mi Chaofeng	Approved by	
Checked by	Yang Xueyu		
Approved by	Zhang Weicang		

REVISION HISTORY

Rev.	Contents	Date
1.0	first release	2014-04-02

n PHYSICAL DATA

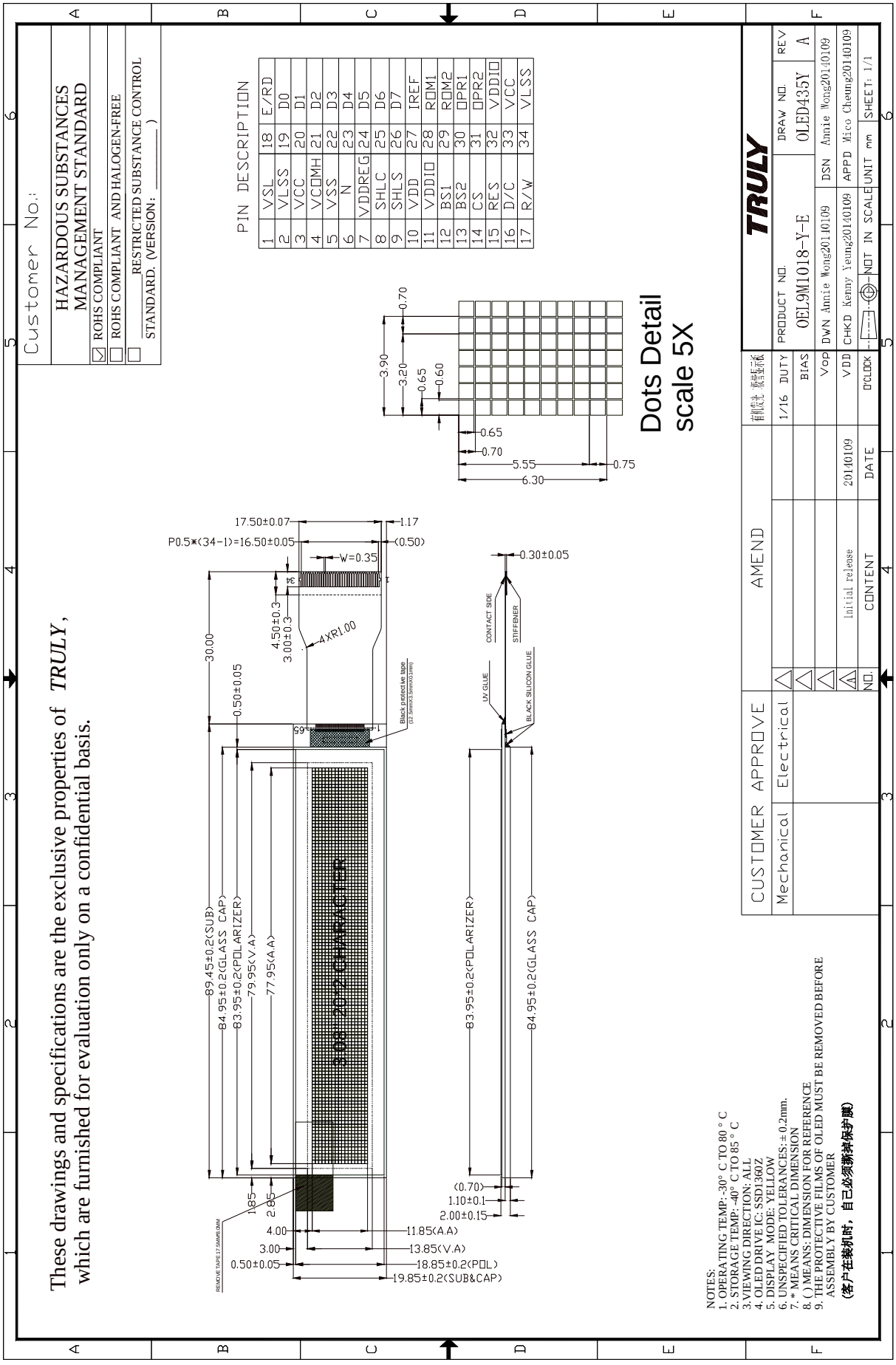
No.	Items:	Specification:	Unit
1	Diagonal Size	3.08	Inch
2	Resolution	20x2	characters
3	Active Area	77.95 (W) x 11.85(H)	mm^2
4	Outline Dimension (Panel)	89.45(W) x 19.85(H)	mm^2
5	Pixel Pitch	0.65(W) x 0.70(H)	mm^2
6	Pixel Size	0.60(W) x 0.65(H)	mm^2
7	Driver IC	SSD1360Z	-
8	Display Color	Yellow	-
8	Grayscale	1	Bit
9	Interface	Parallel / SPI / I2C	-
10	IC package type	COG	-
11	Thickness	2.0±0. 1	mm
12	Weight	TBD	g
13	Duty	1/16	-

n MAXIMUM RATINGS

Voltage Referenced to VSS

Symbol	Parameter	Value	Unit
V_{DDIO}	Supply Voltage	-0.3 to +6	V
V_{DD}		-0.3 to 3.6	V
V_{CC}		0 to 16	V
V_{SEG}	SEG output voltage	0 to V_{CC}	V
V_{COM}	COM output voltage	0 to 0.9*V_{CC}	V
V_{in}	Input voltage	V_{SS}-0.3 to V_{DD}+0.3	V
T_A	Operating Temperature	-40 to +85	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

n EXTERNAL DIMENSIONS



nELECTRICAL CHARACTERISTICS

◆DC Characteristics

Condition(Unless otherwise specified)

Voltage reference to Vss, V_{DDIO} =2.4V to 3.6V ,4.4V to 5.5V

(Ta = 25℃)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{CC}	Operating Voltage	-		8	-	15	V
V_{DDIO}	Low voltage power supply, power supply for I/O pins	Low Voltage I/O Application		2.4	-	3.6	V
		5V I/O Application (V_{DD} as output)		4.4	-	5.5	V
V_{OH}	High Logic Output Level	I_{OUT} = 100uA, 3.3MHz		0.9x V_{DDIO}	-	-	V
V_{OL}	Low Logic Output Level	I_{OUT} = 100uA, 3.3MHz		-	-	0.1x V_{DDIO}	V
V_{IH}	High Logic Input Level	-		0.8x V_{DDIO}	-	-	V
V_{IL}	Low Logic Input Level	-		-	-	0.2x V_{DDIO}	V
I_{SLP_VDD}	V_{DD} Sleep mode Current	V_{DDIO} = 3.3V, V_{CC} = OFF V_{DD} (external: LV I/O mode) = 3.3V, Display OFF, No panel attached		-	-	10	uA
$I_{SLP\ VDDIO}$	V_{DDIO} Sleep mode Current	V_{DDIO} = 3.3V, V_{CC} =OFF Display OFF, No panel attached	Ext V_{DD} = 3.3V	-	-	10	uA
		V_{DDIO} = 5V, V_{CC} =OFF Display OFF, No panel attached	Enable Internal V_{DD} during Sleep mode (at 5V I/O mode)	-	55	70	uA
			Disable Internal V_{DD} during Sleep mode (Deep Sleep mode)	-	-	10	uA
I_{SLP_VCC}	V_{CC} Sleep mode Current	V_{CC} = 8~15V V_{DDIO} = 3.3V, V_{DD} (external) = 3.3V, or V_{DDIO} = 5V, V_{DD} (internal) Display OFF, No panel attached		-	-	10	uA
I_{CC}	V_{CC} Supply Current V_{DDIO} = VDD = 3.3V, VCC =12V, Contrast = FFh, I_{REF} =15uA, No loading, Display ON, All ON, ICON ON			-	1000	1200	uA
I_{DDIO}	V_{DDIO} Supply Current V_{CC} = 12V, Contrast = FFh, I_{REF} = 15uA , No loading, Display ON, All ON, ICON ON	V_{DDIO} = V_{DD} = 3.3V (Low Voltage I/O Application)		-	0.5	5	uA
		V_{DDIO} = 5V (Internal V_{DD}) (5V I/O Application)		-	240	290	uA

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{DD}	V_{DD} Supply Current $V_{DDIO} = V_{DD} = 3.3V$ (Low Voltage I/O Application), $V_{CC} = 12V$, Contrast = FFh, $I_{REF} = 15uA$, No loading, Display ON, All ON, ICON ON		-	200	240	uA
I_{SEG}	Segment Output Current, $V_{DDIO} = V_{DD} = 3.3V$ (LV I/O) or $V_{DDIO} = 5V$ (5V I/O), $V_{CC} = 12V$, $I_{REF} = 15uA$, Display ON	Contrast=FFh	-	600	-	uA
		Contrast=7Fh	-	300	-	
		Contrast=3Fh	-	150	-	
Dev	Segment output current uniformity	$Dev = (I_{SEG} - I_{MID})/I_{MID}$ $I_{MID} = (I_{MAX} + I_{MIN})/2$ $I_{SEG}[0:99]$ = Segment current at contrast setting = FFh	-3	-	3	%
Adj. Dev	Adjacent pin output current uniformity (contrast setting = FFh)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])	-2	-	2	%
$Icon_{SEG}$	Icon Segment Output Current, $V_{DDIO} = V_{DD} = 3.3V$ (LV I/O) or $V_{DDIO} = 5V$ (5V I/O), $V_{CC} = 12V$, $I_{REF} = 15uA$, Display ON	Contrast=7Fh	-	600	-	uA
		Contrast=3Fh	-	300	-	

◆ AC Characteristics

Conditions:

Voltage referenced to V_{SS}

V_{DDIO} = 2.4 to 3.6V (Low Voltage I/O Application) or V_{DDIO} = 4.4V to 5.5V (5V I/O Application)

T_A = 25°C

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
F_{OSC} (1)	Oscillation Frequency of Display Timing Generator	$V_{DD} = 3.3V$ or Internal V_{DD}	268	298	328	kHz
F_{FRM}	Frame Frequency for 16 MUX Mode	2-line Character Display Mode, Display ON, Internal Oscillator Enabled	-	$F_{OSC} * 1 / (D * K * 16)$ (2)	-	Hz
t_{RES}	Reset low pulse width (RES#)	-	2000	-	-	ns

Note

(1) F_{OSC} stands for the frequency value of the internal oscillator and the value is measured when OLED command D5h A[7:4] is in default value.

(2) D: Divide ratio

K: Phase 1 period + Phase 2 period + K_o , where K_o = 170

Default K is 8 + 4 + 170 = 182

Use 8080/6800-Series MPU Parallel Interface or Serial Interface

1. 6800 Series MPU Parallel Interface

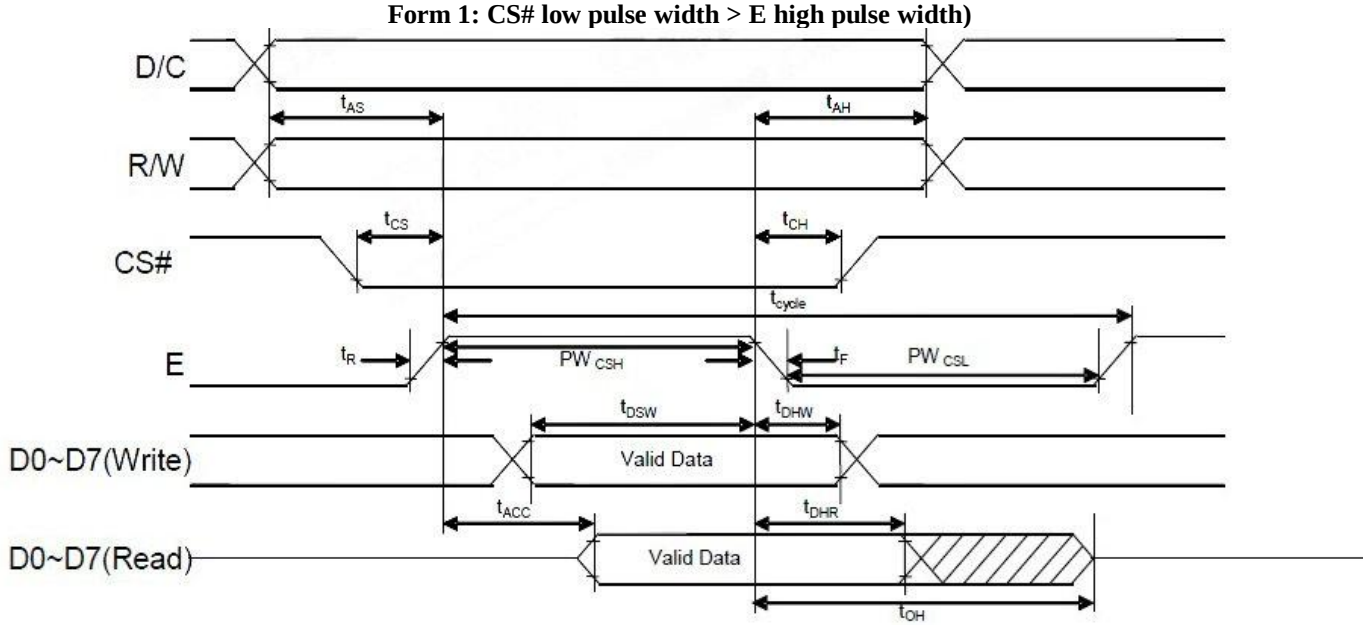
(T_A = 25 °C , V_{DDIO} = 2.4-3.6 / 4.4-5.5V, V_{SS} =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	400	-	-	ns
t_{AS}	Address Setup Time	13	-	-	ns
t_{AH}	Address Hold Time	17	-	-	ns
t_{CS}	Chip Select Time	0	-	-	ns
t_{CH}	Chip Select Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	35	-	-	ns
t_{DHW}	Write Data Hold Time	18	-	-	ns
t_{DHR}	Read Data Hold Time	13	-	-	ns
t_{OH}	Output Disable Time	-	-	90	ns
t_{ACC}	Access Time (RAM) Access Time (command)	-	-	200	ns ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) Chip Select Low Pulse Width (read Command) Chip Select Low Pulse Width (write)	250 250 50	- - -	- - -	ns ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	155 150	- -	- -	ns ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

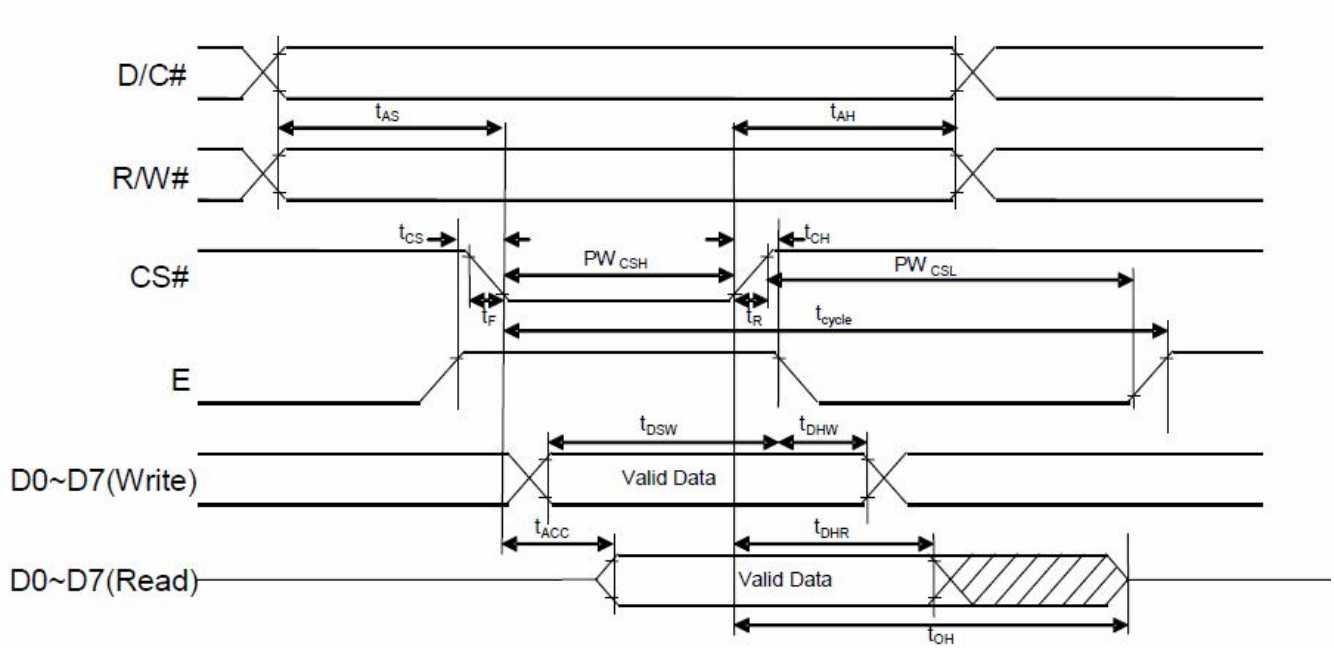
Note

(1) All timings are based on 20% to 80% of V_{DDIO}-V_{SS}

Form 1: CS# low pulse width > E high pulse width)



Form 2: CS# low pulse width < E high pulse width)



2. 8080 Series MPU Parallel Interface

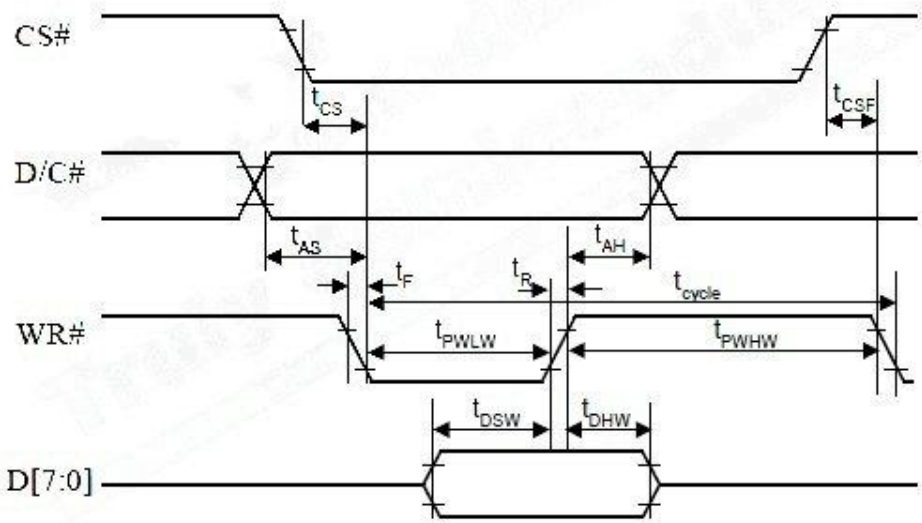
8080-Series MCU Parallel Interface Timing Characteristics

(T_A = 25°C, V_{DDIO} = 2.4-3.6 / 4.4-5.5V, V_{SS} =0V)

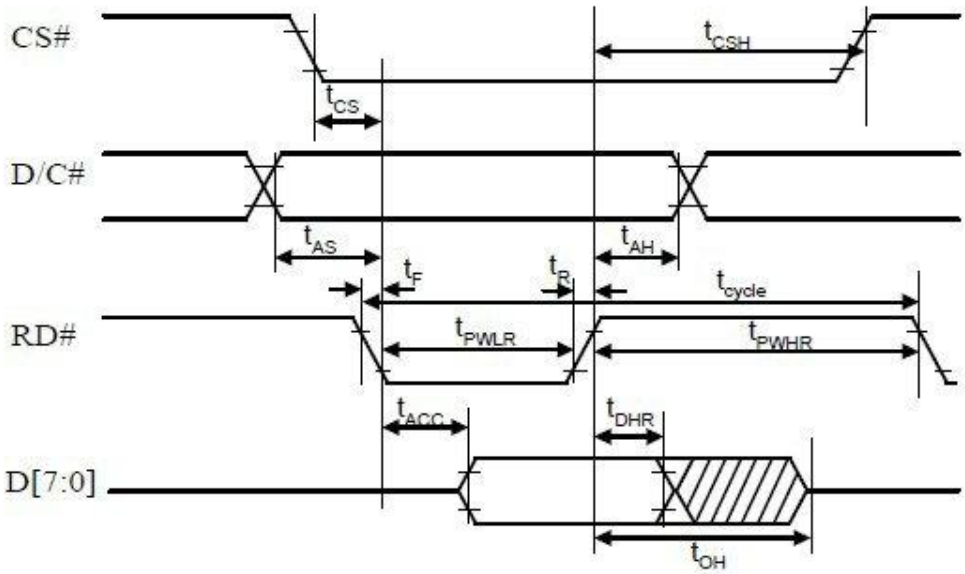
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	400	-	-	ns
t_{AS}	Address Setup Time	13	-	-	ns
t_{AH}	Address Hold Time	17	-	-	ns
t_{CS}	Chip Select Time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	0	-	-	ns
t_{DSW}	Write Data Setup Time	35	-	-	ns
t_{DHW}	Write Data Hold Time	18	-	-	ns
t_{DHR}	Read Data Hold Time	13	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time (RAM) Access Time (command)	-	-	200	ns ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) - t_{PWLR} Chip Select Low Pulse Width (read Command) - t_{PWLR} Chip Select Low Pulse Width (write) - t_{PWLW}	250 250 50	- - -	- - -	ns ns ns
PW_{CSH}	Chip Select High Pulse Width (read) - t_{PWHR} Chip Select High Pulse Width (write) - t_{PWHW}	155 150	- -	- -	ns ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

8080-series parallel interface characteristics

Write cycle



Read Cycle



3. Serial Interface

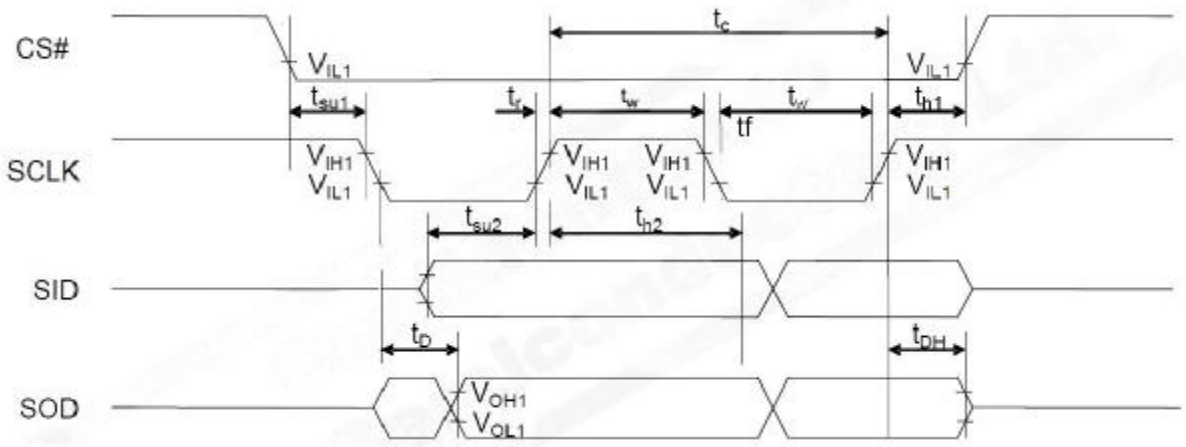
Serial Timing Characteristics

(T_A = 25°C, V_{DDIO} = 2.4-3.6 / 4.4-5.5V, V_{SS} =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_c	Serial clock cycle time	1	-	20	us
t_r, t_f	Serial clock rise/fall time	-	-	15	ns
t_w	Serial clock width (high, low)	400	-	-	ns
t_{su1}	Chip select setup time	60	-	-	ns
t_{h1}	Chip select hold time	20	-	-	ns
t_{su2}	Serial input data setup time	200	-	-	ns
t_{h2}	Serial input data hold time	20	-	-	ns
t_D	Serial output data delay time	200	-	-	ns
t_{DH}	Serial output data hold time	10	-	-	ns

Note: All timings are based on 20% to 80% of V_{DDIO}-V_{SS}

Serial Timing Characteristics



4. I²C Timing Characteristics

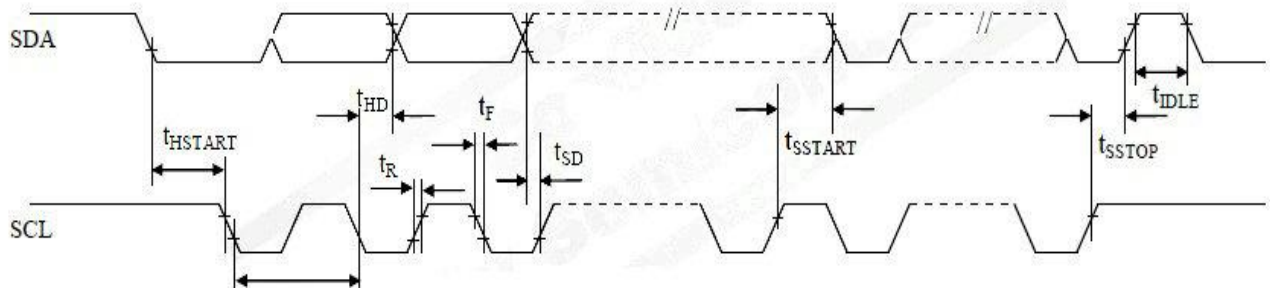
I2C Timing Characteristics

(T_A = 25°C, V_{DDIO} = 2.4-3.6 / 4.4-5.5V, V_{SS} =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	5	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	460	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

Note: All timings are based on 20% to 80% of V_{DDIO}-V_{SS}

Figure 12-5 : I2C Timing Characteristics



n TIMING OF POWER SUPPLY

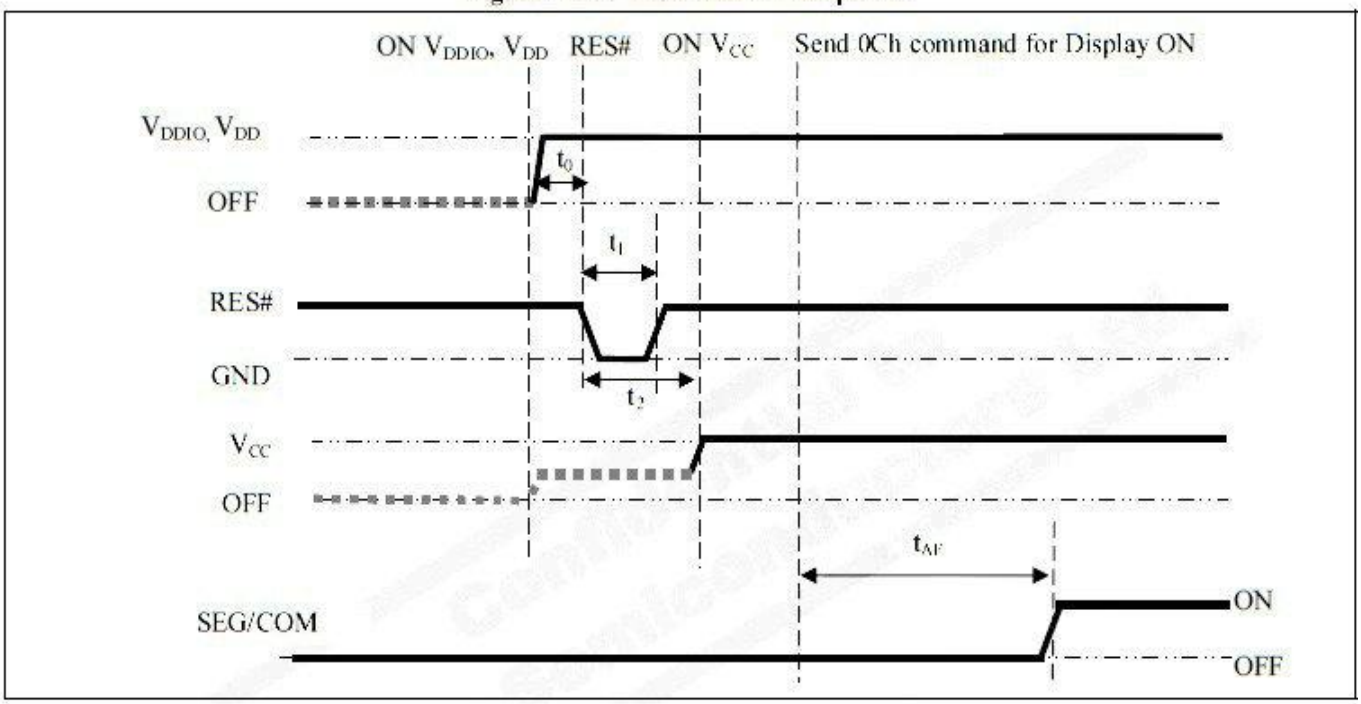
The following figures illustrate the recommended power ON and power OFF sequence of SSD1360 :

When LV I/O mode is chosen:

Power ON sequence:

1. Power ON V_{DDIO}, V_{DD}
2. After V_{DDIO}, V_{DD} become stable, wait at least 20ms (t_0), set RES# pin LOW (logic low) for at least 3us (t_1) [4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC} [1]
4. After V_{CC} become stable, send fundamental command 0Ch (for RE=0b, SD=0b) for display ON. SEG/COM will be ON after 100ms (t_{AF}).

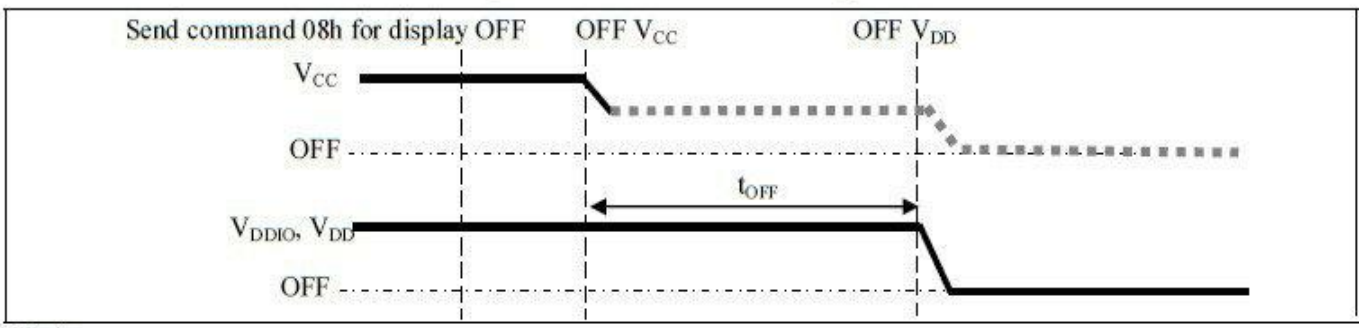
Figure 7-14 : The Power ON sequence



Power OFF sequence:

1. Send fundamental command 08h (for RE=0b, SD=0b) for display OFF.
2. Power OFF V_{CC} [1], [2], [3]
3. Power OFF V_{DDIO}, V_{DD} after t_{OFF}. (where Minimum t_{OFF}=0ms [5], Typical t_{OFF}=100ms)

Figure 7-15 : The Power OFF sequence



Note:

[1] Since an ESD protection circuit is connected between V_{DDIO}, V_{DD} and V_{CC}, V_{CC} becomes lower than V_{DDIO}, V_{DD} whenever V_{DDIO}, V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 7-14 and Figure 7-15.

[2] V_{CC} should be kept float (i.e. disable) when it is OFF.

[3] Power Pins (V_{DDIO}, V_{DD} , V_{CC}) can never be pulled to ground under any circumstance.

[4] The register values are reset after t_1.

[5] V_{DDIO}, V_{DD} should not be Power OFF before V_{CC} Power OFF.

n ELECTRO-OPTICAL CHARACTERISTICS (Ta=25℃)

Items		Symbol	Min.	Typ.	Max.	Unit	Remark
Operating Luminance		L	120	150*	-	cd /m^2	Yellow
Power Consumption		P	-	105	120	mW	30% pixels ON L=150cd/m^2
Frame Frequency		Fr	-	100	-	Hz	-
Color Coordinate	Yellow	CIE x	0.42	0.46	0.50	CIE1931	Darkroom
		CIE y	0.47	0.52	0.55		
Response Time	Rise	Tr	-	-	0.02	ms	-
	Decay	Td	-	-	0.02	ms	-
Contrast Ratio*		Cr	10000:1	-	-	-	Darkroom
Viewing Angle		△ θ	160	-	-	Degree	-
Operating Life Time*		Top	40,000	-	-	Hours	L=150cd/m^2

Note:

1. **150cd/m^2** is base on V_{DD}=3.0V, V_{CC}=12.0V, contrast command setting 0x5F;
2. **Contrast ratio** is defined as follows:

$$\text{Contrast ratio} = \frac{\text{Photo – detector output with OLED being “white”}}{\text{Photo – detector output with OLED being “black”}}$$

3. **Life Time** is defined when the Luminance has decayed to less than 50% of the initial Luminance specification. (Odd and even chess board alternately displayed)
(The initial value should be closed to the typical value after adjusting.)

n INTERFACE PIN CONNECTIONS

<table>
<tr><th>No</th><th>Symbol</th><th>Description</th></tr>
<tr><td>1</td><td>VSL</td><td>This is segment voltage (output low level) reference pin. When external VSL is not used, this pin should be left</td></tr>
<tr><td>2</td><td>VLSS</td><td>Analog system ground pin. It must be connected to external ground.</td></tr>
<tr><td>3</td><td>VCC</td><td>Power supply for panel driving voltage. This is also the most positive power voltage supply pin. It is supplied by external high voltage source.</td></tr>
<tr><td>4</td><td>VCOMH</td><td>COM signal deselected voltage level.
A capacitor should be connected between this pin and VSS.
No external power supply is allowed to connect to this</td></tr>
<tr><td>5</td><td>VSS</td><td>Ground pin. It must be connected to external ground.</td></tr>
<tr><td>6</td><td>N</td><td>Select number of display line during power ON reset
When this pin is pulled HIGH, 2-line is selected as display line .When this pin is pulled LOW, 1-line is selected as display line.</td></tr>
<tr><td>7</td><td>VDDREG</td><td>Internal VDD regulator selection pin in 5V I/O application mode.
When this pin is pulled HIGH, internal VDD regulator is enabled (5V I/O application).
When this pin is pulled LOW, internal VDD regulator is disabled (Low voltage I/O application).
Under 5V I/O application mode, internal VDD regulator can also be disabled by extended command 71h “Function Selection A” for power saving;.</td></tr>
<tr><td>8</td><td>SHLC</td><td>This pin is used to determine the Common output scanning direction.
<table>
<tr><td>SHLC</td><td>COM scan direction</td></tr>
<tr><td>1</td><td>COM0 to COM16 (Normal)</td></tr>
<tr><td>0</td><td>COM16 to COM0 (Reverse)</td></tr>
</table></td></tr>
<tr><td>9</td><td>SHLS</td><td>This pin is used to change the mapping between the display data column address and the Segment driver.
<table>
<tr><td>SHLS</td><td>SEG direction</td></tr>
<tr><td>1</td><td>SEG0 to SEG119 (Normal)</td></tr>
<tr><td>0</td><td>SEG119 to SEG0 (Reverse)</td></tr>
</table></td></tr>
</table>

10	VDD	Power supply for core logic operation. VDD can be supplied externally or regulated internally. In LV IO application (internal VDD is disabled), this is a power input pin. In 5V IO application (internal VDD is enabled), VDD is regulated internally from VDDIO. A capacitor should be connected between VDD and VSS under all circumstances.
11	VDDIO	Low voltage power supply and power supply for interface logic level in both Low Voltage I/O and 5V I/O application. It should match with the MCU interface voltage level and must be connected to external source.
12	BS1	MCU bus interface selection pins.
13	BS2	
14	CS#	This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW (active LOW). In I2C mode, this pin must be connected to VSS.
15	RES#	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed.
16	D/C#	This pin is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data at D[7:0] will be interpreted as data. When the pin is pulled LOW, the data at D[7:0] will be transferred to a command register. In I2C mode, this pin acts as SA0 for slave address selection.
17	R/W#	This pin is read / write control input pin connecting to the MCU interface. When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I2C interface is selected, this pin must be connected to VSS.

<table>
<tr><td>18</td><td>E/RD#</td><td>This pin is MCU interface input.
When 6800 interface mode is selected, this pin will be used as the Enable (E) signal.
Read/write operation is initiated when this pin is pulled HIGH and the chip is selected.
When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected.
When serial or I2C interface is selected, this pin must be connected to VSS.</td></tr>
<tr><td>19~26</td><td>D0~D7</td><td>These pins are bi-directional data bus connecting to the MCU data bus.
Unused pins are recommended to tie LOW.
When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SID and D2 will be the serial data output: SOD.
When I2C mode is selected, D2, D1 should be tied together and serve as SDA out , SDA in application and D0 is the serial clock input, SCL.</td></tr>
<tr><td>27</td><td>IREF</td><td>This pin is the segment output current reference pin.
IREF is supplied externally.
A resistor should be connected between this pin and VSS to maintain current of around 15uA .</td></tr>
<tr><td>28~29</td><td>ROM1~ROM2</td><td>These pins are used to select Character ROM; select appropriate logic setting as described in the following table. ROM1 and ROM0 are pin select as shown in below table:
<table>
<tr><td>ROM1</td><td>ROM0</td><td>ROM</td></tr>
<tr><td>0</td><td>0</td><td>A</td></tr>
<tr><td>0</td><td>1</td><td>B</td></tr>
<tr><td>1</td><td>0</td><td>C</td></tr>
<tr><td>1</td><td>1</td><td>S/W selectable</td></tr>
</table>
S/W selectable by extended command 72h “Function Selection B”;</td></tr>
<tr><td>30~31</td><td>OPR1~ OPR2</td><td>This pin is used to select the character number of character generator.
<table>
<tr><td>OPR1</td><td>OPR0</td><td>CGROM</td><td>CGRAM</td></tr>
<tr><td>1</td><td>1</td><td>256</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>248</td><td>8</td></tr>
<tr><td>1</td><td>0</td><td>250</td><td>6</td></tr>
<tr><td>0</td><td>0</td><td>240</td><td>8</td></tr>
</table></td></tr>
<tr><td>32</td><td>VDDIO</td><td>Same as pin 11</td></tr>
</table>

33	VCC	Same as pin 3.
34	VLSS	Same as pin 2.

MCU Bus Interface Pin Selection

Pin name	8080-parallel(8bit)	6800-parallel(8bit)	Serial Interface	I2C Interface
BS1	1	0	0	1
BS2	1	1	0	0

Note: 0 is connected to Vss
1 is connected to VDD.

n COMMAND TABLE

1. Fundamental Command TableSet													
Command	RE	SD	Instruction Code										Description
			D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0	
Clear Display	X	0	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC.
Return Home	0	0	0	0	0	0	0	0	0	0	1	*	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.
Entry Mode Set	0	0	0	0	0	0	0	0	0	1	I/D	S	Assign cursor / blink moving direction with DDRAM address. I/D = "1": cursor/ blink moves to right and DDRAM address is increased by 1 (POR) I/D = "0": cursor/ blink moves to left and DDRAM address is decreased by 1 Assign display shift with DDRAM address. S = "1": make display shift of the enabled lines by the DS2 to DS1 bits in the shift enable instruction. Left/ right direction depends on I/D bit selection. S = "0": display shift disable (POR)
	1	0	0	0	0	0	0	0	0	1	BDC	BDS	Common bi-direction function. BDC = "0": COM16 -> COM0 BDC = "1": COM0 -> COM16 Segment bi-direction function. BDS = "0": SEG119 -> SEG0, BDS = "1": SEG0 -> SEG119
Display ON / OFFControl	0	0	0	0	0	0	0	0	1	D	C	B	Set display/cursor/blink ON/OFF D = "1": display ON, D = "0": display OFF (POR), C = "1": cursor ON, C = "0": cursor OFF (POR), B = "1": blink ON, B = "0": blink OFF (POR). Note: It is recommended to turn off the cursor and blinking effects when updating internal RAM contents for better visual performance; refer to Section 9.1.4 for details

1. Fundamental Command TableSet

Command	RE	SD	Instruction Code										Description
			D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0	
Function Set	0	0	0	0	0	0	1	DL	N	RE (0)	BR1	BR0	Parallel bus width, DL when DL= " 1" (POR): 8-bit, when DL = "0": 4-bit Numbers of display line, N when N = "1" (POR): 2-line, when N = "0": 1-line Extension register, RE ("0") Brightness ratio, BR[1:0] (% setting of different contrast level) 00: 100%, 01: 75%, 10: 50%, 11: 25%
	1	0	0	0	0	0	1	DL	N	RE (1)	BE	REV	Extension register, RE ("1") CGRAM blink enable BE = 1b: CGRAM blink enable BE = 0b: CGRAM blink disable (POR) Reverse bit REV = "1": reverse display, REV = "0": normal display (POR)
Set CGRAM address	0	0	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter. (POR=00 0000)
Set DDRAM Address	0	0	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter. (POR=000 0000)
Set Scroll Quantity	1	0	0	0	1	*	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	Set the quantity of horizontal dot scroll. (POR=00 0000) Valid up to SQ[5:0] = 110000b
Read Busy Flag and Address/ Part ID	X	0	0	1	BF	AC6 / ID6	AC5 / ID5	AC4 / ID4	AC3 / ID3	AC2 / ID2	AC1 / ID1	AC0 / ID0	Can be known whether during internal operation or not by reading BF. The contents of address counter or the part ID can also be read. When it is read the first time, the address counter can be read. When it is read the second time, the part ID can be read. BF = "1": busy state BF = "0": ready state
Write data	X	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM / CGRAM).
Read data	X	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM / CGRAM).

*Notes
(1) POR stands for Power On Reset Values.POR stands for Power On Reset Values.
(2) "*" and "X" stand for "Don't care".

2. Extended Command Set

Command	RE	SD	Instruction Code											Description
			D/C#	R/W# (WR#)	Hex	D7	D6	D5	D4	D3	D2	D1	D0	
Function Selection A	1	0	0	0	71	0	1	1	1	0	0	0	1	A[7:0] = 00h, Disable internal V_{DD} regulator at 5V I/O application mode A[7:0] = 5Ch, Enable internal V_{DD} regulator at 5V I/O application mode (POR)
	1	0	1	0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
Function Selection B	1	0	0	0	72	0	1	1	1	0	0	1	0	OP[1:0]: Select the character no. of character generator OP[1:0] / CGROM / CGRAM 00b / 240 / 8 01b / 248 / 8 10b / 250 / 6 11b / 256 / 0 RO[1:0]: Select character ROM RO[1:0] / ROM 00b / A 01b / B 10b / C 11b / Invalid **Note**: It is recommended to turn off the disply (cmd 08h) before setting no. of CGRAM and defining character ROM, while clear display (cmd 01h) is recommended to sent afterwards
	1	0	1	0		*	*	*	*	RO1	RO0	OP1	OP0	
OLED Characterization	1	X	0	0	78 / 79	0	1	1	1	1	0	0	SD	Extension register, SD SD = 0b: OLED command set is disabled (POR) SD = 1b: OLED command set is enabled Details refer to Table 8-3, Table and Table 8-5.

Notes
(1) POR stands for Power On Reset Values.
(2) "*" and "X" stand for "Don't care".

3. OLED Command Set

Command	RE	SD	Instruction Code											Description
			D/C#	R/W# (WR#)	Hex	D7	D6	D5	D4	D3	D2	D1	D0	
Set Contrast Control	1	1	0	0	81	1	0	0	0	0	0	0	1	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 7Fh)
	1	1	0	0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
Set Display Clock Divide Ratio/Oscillator Frequency	1	1	0	0	D5	1	1	0	1	0	1	0	1	A[3:0] : Define the divide ratio (D) of the display clocks (DCLK): Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1) A[7:4] : Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 0100b Range:0000b~1111b Frequency increases as setting value increases.
	1	1	0	0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
Set Pre-charge Period	1	1	0	0	D9	1	1	0	1	1	0	0	1	A[3:0] : Phase 1 period of up to 15 DCLK clocks 0 is invalid entry (RESET= 8h) A[7:4] : Phase 2 period of up to 15 DCLK clocks 0 is invalid entry (RESET=4h)
	1	1	0	0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
Set COM Pins Hardware Configuration	1	1	0	0	DA	1	1	0	1	1	0	1	0	A[4]=0b, Sequential SEG pin configuration A[4]=1b(RESET), Alternative SEG pin configuration A[5]=0b(RESET), Disable SEG Left/Right remap A[5]=1b, Enable SEG Left/Right remap
	1	1	0	0	A[7:0]	0	0	A_5	A_4	0	0	1	0	
Set V_{COMH} Deselect Level	1	1	0	0	DB	1	1	0	1	1	0	1	1	A[5:4] / Hex code / V_{COMH} deselect level 00b / 00h / ~0.65 x V_{CC} 10b / 20h / ~0.77 x V_{CC} (RESET) 11b / 30h / ~0.83 x V_{CC}
	1	1	0	0	A[7:0]	0	0	A_5	A_4	0	0	0	0	

3. OLED Command Set

Command	RE	SD	Instruction Code										Description
			D/C#	R/W# (WR#)	Hex	D7	D6	D5	D4	D3	D2	D1	D0	
GPIO Function	1	1	0	0	DC	1	1	0	1	1	1	0	0	Set GPIO:
	1	1	0	0	A[7:0]	0	0	0	0	0	0	A_1	A_0	A[1:0] = 00b represents GPIO pin HiZ, input disabled (always read as low) A[1:0] = 01b represents GPIO pin HiZ, input enabled A[1:0] = 10b represents GPIO pin output Low (RESET) A[1:0] = 11b represents GPIO pin output High
VSL Setting	1	1	0	0	F2	1	1	1	1	0	0	1	0	A[1] = 0b: Enable external VSL A[1] = 1b: Internal VSL (RESET) Note (a) Refer to Table 6-1 for VSL pin details
	1	1	0	0	A[1]	0	0	0	0	0	0	A_1	0	

Note

(1) POR stands for Power On Reset Values.

(2) "*" and "X" stand for "Don't care".

(3) The locked OLED driver IC MCU interface prohibits all commands access except logic bit SD is set to 1b.

(4) Refer to Table 8-1 and Table 8-2 and for the details of logic bits RE and SD.

4. Graphic Command Set

Command	RE	SD	Instruction Code											Description
			D/C#	R/W# (WR#)	Hex	D7	D6	D5	D4	D3	D2	D1	D0	
Character Mode or Graphic Mode Selection	1 1	1 1	0 0	0 0	F0 A[7:0]	1 *	1 *	1 *	1 *	0 *	0 *	0 *	0 A_0	A[0]=0b, Graphic mode A[0]=1b (RESET), Character mode
Set Lower Column Start Address for Page Addressing Mode	1	1	0	0	00~0F	0	0	0	0	X_3	X_2	X_1	X_0	Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. **Note** (2) This command is only for page addressing mode
Set Higher Column Start Address for Page Addressing Mode	1	1	0	0	10~17	0	0	0	1	0	X_2	X_1	X_0	Set the higher nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. **Note** (3) This command is only for page addressing mode
Set Memory Addressing Mode	1 1	1 1	0 0	0 0	20 A[7:0]	0 *	0 *	1 *	0 *	0 *	0 *	0 A_1	0 A_0	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode (RESET) A[1:0] = 11b, Invalid
Set Column Address	1 1 1	1 1 1	0 0 0	0 0 0	21 A[7:0] B[7:0]	0 * *	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Setup column start and end address A[6:0] : Column start address, range : 0-119d, (RESET=0d) B[6:0]: Column end address, range : 0-119d, (RESET =119d) **Note** (1) This command is only for horizontal or vertical addressing mode.
Set Page Address	1 1 1	1 1 1	0 0 0	0 0 0	22 A[7:0] B[7:0]	0 * *	0 * *	1 * *	0 * *	0 * *	0 * *	1 * *	0 A_0 B_0	Setup page start and end address A[2:0] : Page start Address, range : 0-1d, (RESET = 0d) B[2:0] : Page end Address, range : 0-1d, (RESET = 1d) **Note** (1) This command is only for horizontal or vertical addressing mode.

4. Graphic Command Set

Command	RE	SD	Instruction Code											Description
			D/C#	R/W# (WR#)	Hex	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display Start Line	1	1	0	0	40~4F	0	1	0	0	X_3	X_2	X_1	X_0	Set display RAM display start line register from 0-15 using $X_3X_2X_1X_0$. Display start line register is reset to 0000b during RESET. **Note** (1) The scroll offset value should be less than the vertical scroll area set by OLED command A3h.
Set Vertical Scroll Area	1	1	0	0	A3	1	0	1	0	0	0	1	1	A[3:0] : Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0).[RESET = 0] B[4:0] : Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 16] **Note** (1) A[3:0]+B[4:0] <= MUX ratio (2) B[4:0] <= MUX ratio (3a) Vertical scrolling offset (E[3:0] in 29h/2Ah) < B[4:0] (3b) Set Display Start Line ($X_3X_2X_1X_0$ of 40h~4Fh) < B[4:0] (4) The last row of the scroll area shifts to the first row of the scroll area. (5) For 16d MUX display A[3:0] = 0, B[4:0]=16 : whole area scrolls A[3:0]= 0, B[4:0] < 16 : top area scrolls A[3:0] + B[4:0] < 16 : central area scrolls A[3:0] + B[4:0] = 16 : bottom area scrolls
	1	1	0	0	A[7:0]	*	*	*	*	B_4	B_3	B_2	B_1	B_0
Entire Display ON	1	1	0	0	A4/A5	1	0	1	0	0	1	0	X_0	A4h, X0=0b: Resume to RAM content display (RESET) Output follows RAM content A5h, X0=1b: Entire display ON Output ignores RAM content
	1	1	0	0	A[7:0]	*	*	*	*	A_3	A_2	A_1	A_0	
Set Page Start Address for Page Addressing Mode	1	1	0	0	B0~B1	1	0	1	1	0	0	0	X_0	Set GDDRAM Page Start Address (PAGE0~PAGE1) for Page Addressing Mode using X[0]. **Note** (1) This command is only for page addressing mode
Set Display Offset	1	1	0	0	D3	1	1	0	1	0	0	1	1	Set vertical shift by COM from 0d~15d The value is reset to 0000b after RESET.
	1	1	0	0	A[7:0]	*	*	*	*	A_3	A_2	A_1	A_0	

4. Graphic Command Set

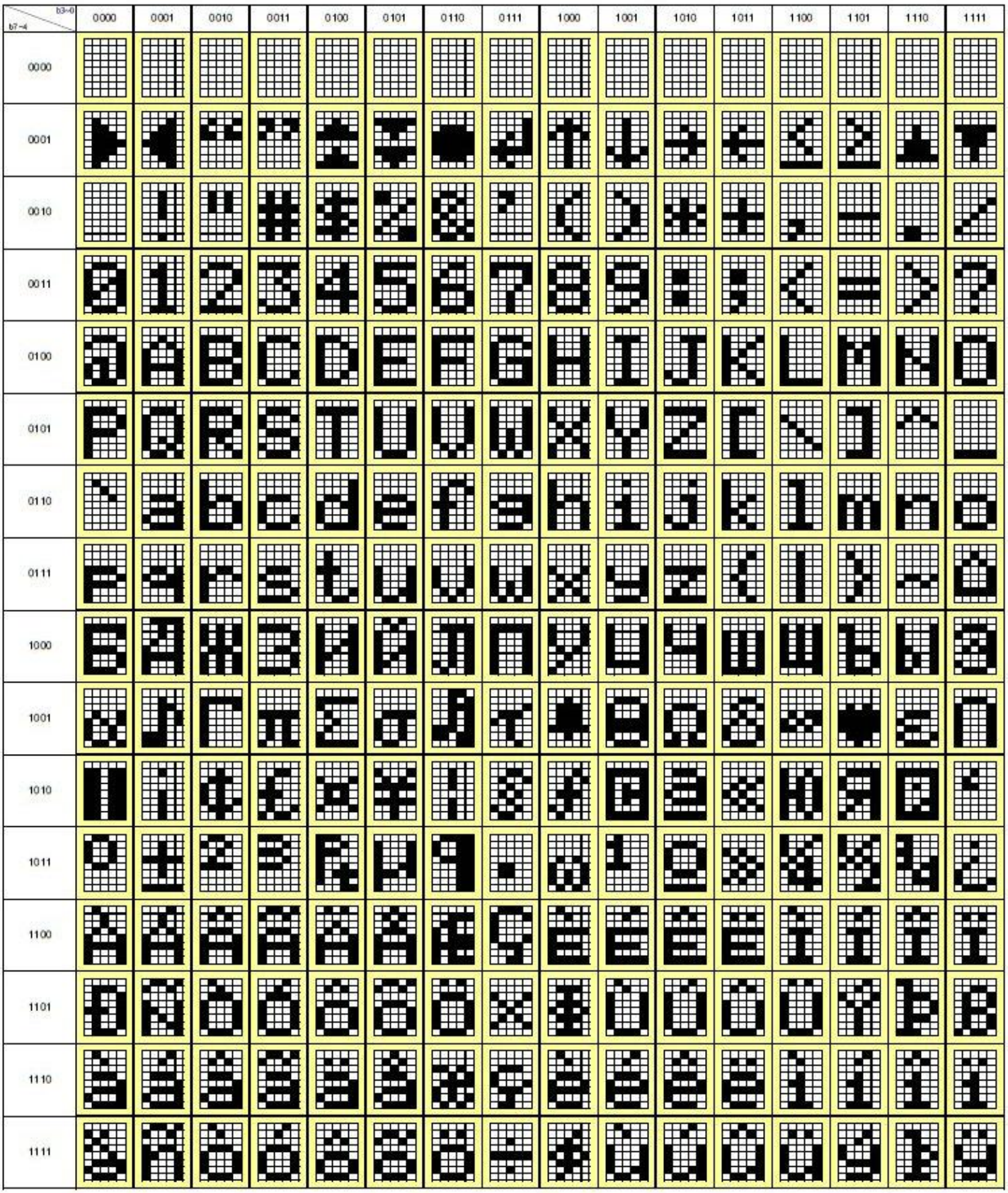
Command	RE	SD	Instruction Code D/C#	R/W# (WR#)	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Description
Continuous Horizontal Scroll Setup	1	1	0	0	26/27	0	0	1	0	0	1	1	X_0	26h, X[0]=0, Right Horizontal Scroll 27h, X[0]=1, Left Horizontal Scroll (Horizontal scroll by 1 column) A[7:0] : Dummy byte (Set as 00h) B[0] : Define start page address 0b – PAGE0 | 1b – PAGE1 C[2:0] : Set time interval between each scroll step in terms of frame frequency 000b – 6frames | 100b – 3frames 001b – 32frames | 101b – 4frames 010b – 64frames | 110b – 5frames 011b – 128frames | 111b – 2frames D[0] : Define end page address 0b – PAGE0 | 1b – PAGE1 The value of D[0] must be larger or equal to B[0] E[7:0] : Dummy byte (Set as 00h) F[6:0] : Define start column address (00d-119d) G[6:0] : Define end column address (00d-119d) The value of G[6:0] must be larger or equal to F[6:0]
	1	1	0	0	A[7:0]	0	0	0	0	0	0	0	0	
	1	1	0	0	B[7:0]	*	*	*	*	*	*	*	B_0	
	1	1	0	0	C[7:0]	*	*	*	*	*	C_2	C_1	C_0	
	1	1	0	0	D[7:0]	*	*	*	*	*	*	*	D_0	
	1	1	0	0	E[7:0]	0	0	0	0	0	0	0	0	
	1	1	0	0	F[7:0]	*	F_6	F_5	F_4	F_3	F_2	F_1	F_0	
	1	1	0	0	G[7:0]	*	G_6	G_5	G_4	G_3	G_2	G_1	G_0	
Continuous Vertical and Horizontal Scroll Setup	1	1	0	0	29/2A	0	0	1	0	1	0	X_1	X_0	29h, X_1X_0=01b : Vertical and Right Horizontal Scroll 2Ah, X_1X_0=10b : Vertical and Left Horizontal Scroll A[0] : Horizontal scrolling offset A[0] = 0, no offset A[0] = 1, scroll by 1 column
	1	1	0	0	A[7:0]	*	*	*	*	*	*	*	A_0	
	1	1	0	0	B[7:0]	*	*	*	*	*	*	*	B_0	
	1	1	0	0	C[7:0]	*	*	*	*	*	C_2	C_1	C_0	
	1	1	0	0	D[7:0]	*	*	*	*	*	*	*	D_0	
	1	1	0	0	E[7:0]	*	*	*	*	E_3	E_2	E_1	E_0	
	1	1	0	0	F[7:0]	*	F_6	F_5	F_4	F_3	F_2	F_1	F_0	
	1	1	0	0	G[7:0]	*	G_6	G_5	G_4	G_3	G_2	G_1	G_0	

4. Graphic Command Set

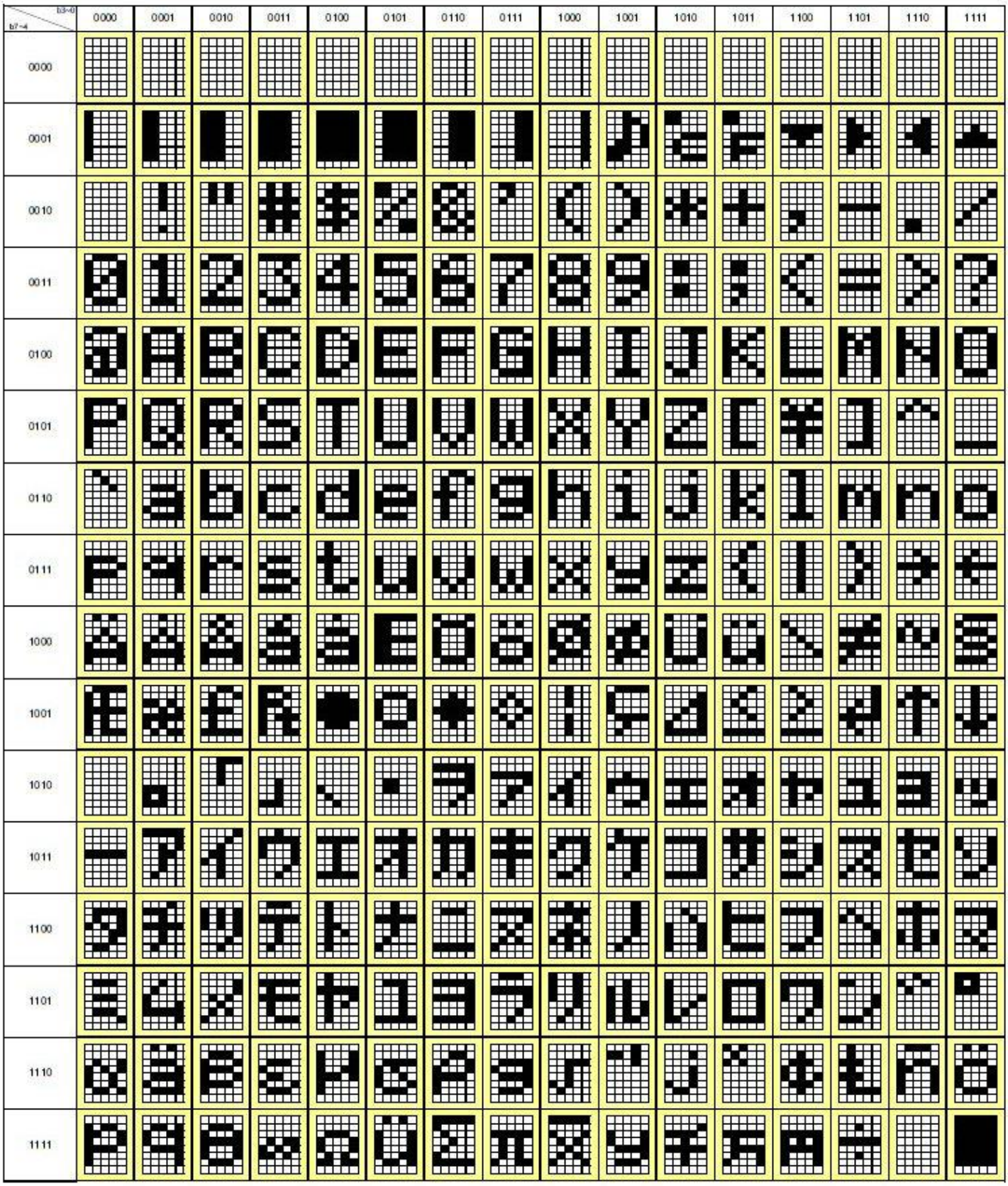
Command	RE	SD	Instruction Code											Description
			D/C#	R/W# (WR#)	Hex	D7	D6	D5	D4	D3	D2	D1	D0	
Content Scroll Setup	1	1	0	0	2C/2D	0	0	1	0	1	1	0	X_0	2Ch, X[0]=0, Right Horizontal Scroll by one column 2Dh, X[0]=1, Left Horizontal Scroll by one column A[7:0] : Dummy byte (Set as 00h) B[0] : Define start page address 0b – PAGE0 | 1b – PAGE1
	1	1	0	0	A[7:0]	0	0	0	0	0	0	0	0	
	1	1	0	0	B[7:0]	*	*	*	*	*	*	*	B_0	
	1	1	0	0	C[7:0]	0	0	0	0	0	0	0	1	
	1	1	0	0	D[7:0]	*	*	*	*	*	*	*	D_0	
	1	1	0	0	E[7:0]	0	0	0	0	0	0	0	0	
	1	1	0	0	F[7:0]	*	F_6	F_5	F_4	F_3	F_2	F_1	F_0	
	1	1	0	0	G[7:0]	*	G_6	G_5	G_4	G_3	G_2	G_1	G_0	

n CHARACTER GENERATION ROM

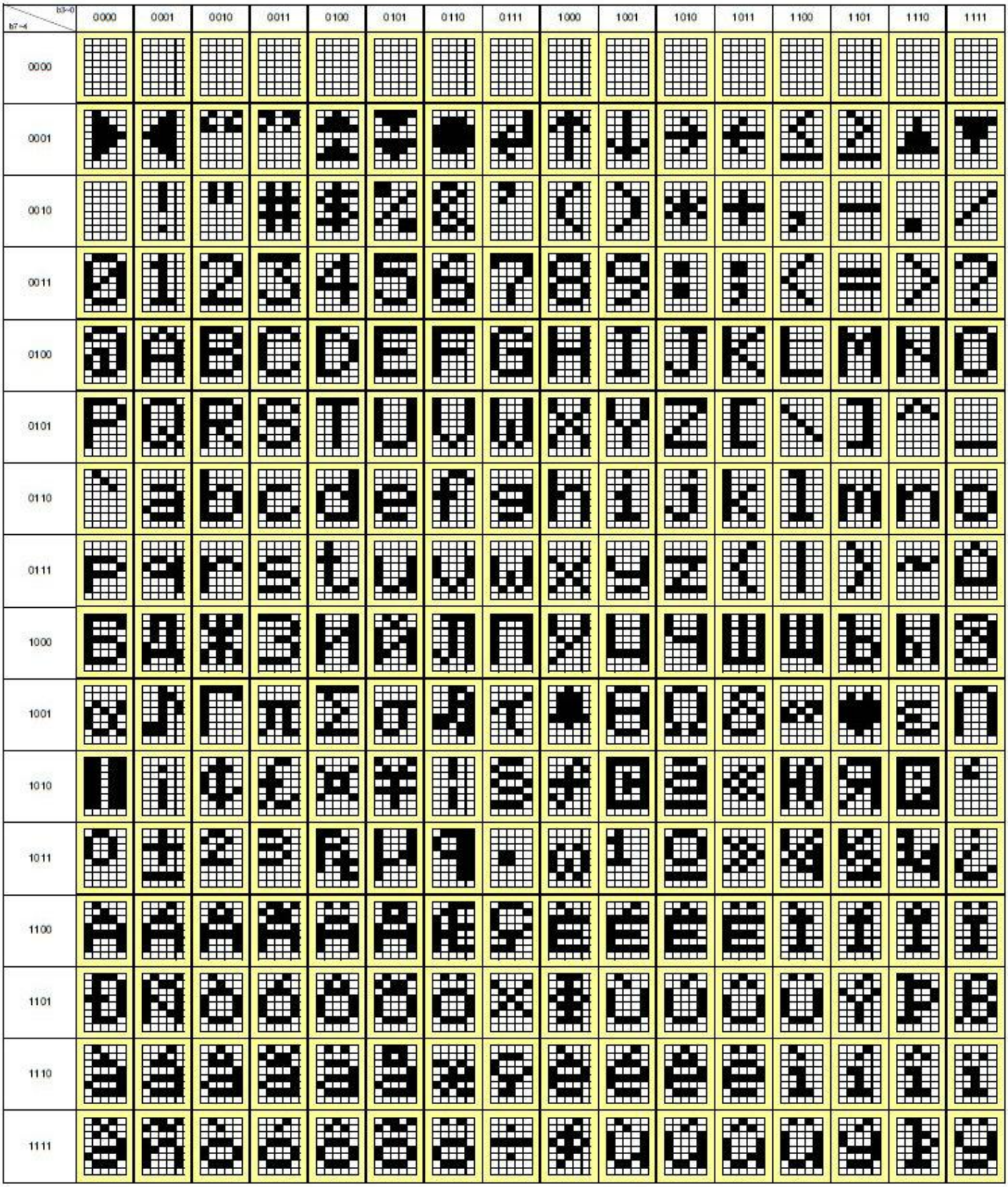
ROM A



ROM B


b3~0
b7~4
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111

ROM C


b3~0
b7~4
0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111

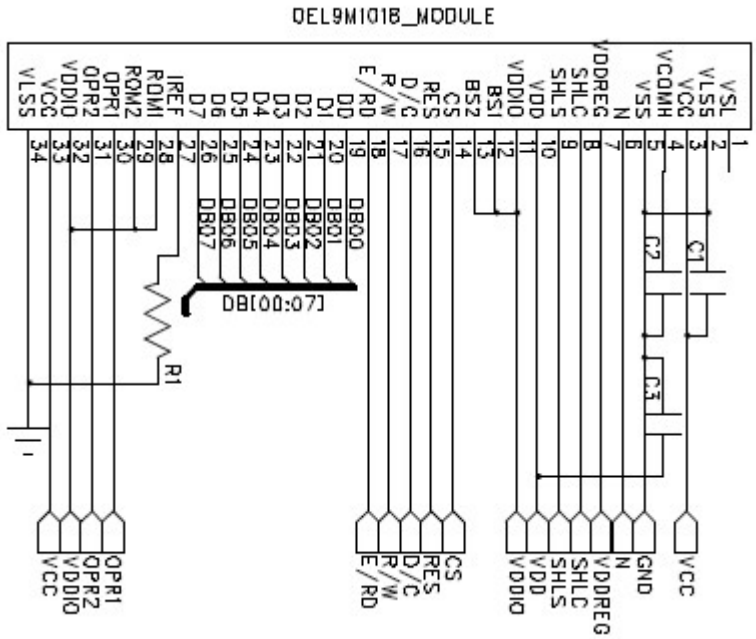
n INITIALIZATION CODE

```
void InitOLED_MASTER_SSD1360(void)
{
  MainOLED_WCom(0x38);

   //display off,blink off ,cursor off
   MainOLED_WCom(0X08);

  MainOLED_WCom(0x3C);//3CH:RE=1,38H:RE=0
  //Entry Mode Set
  MainOLED_WCom(0x05);

  //OLED command set is enabled
  MainOLED_WCom(0x79);

  //Set Contrast Control
  MainOLED_WCom(0x81);
  MainOLED_WCom(CONTRAST);

  //Set Display Clock Divide Ratio/Oscillator Frequency
  MainOLED_WCom(0xD5);
  MainOLED_WCom(0x40);

  //Set Pre-charge Period
  MainOLED_WCom(0xD9);
  MainOLED_WCom(0x48);

  //Set SEG Pins Hardware Configuration
  MainOLED_WCom(0xDA);
  MainOLED_WCom(0x12);

  //Set VCOMH
  MainOLED_WCom(0xDB);
  MainOLED_WCom(0x20);

  //GPIO Function
  MainOLED_WCom(0xDC);
  MainOLED_WCom(0x00);

  //VSL Setting
  MainOLED_WCom(0xF2);
  MainOLED_WCom(0x02);

  //Character Mode or Graphic Mode Selection(0b Graphic mode;1b Character mode)
```

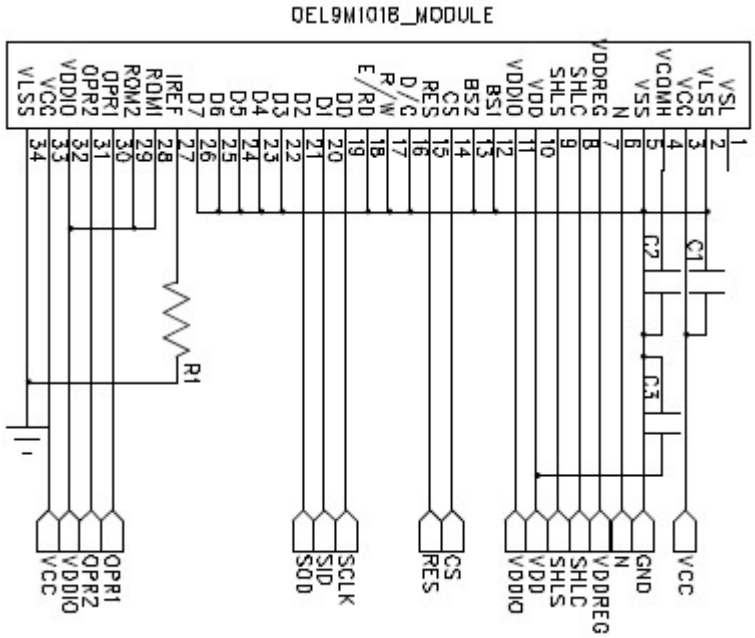
```
  MainOLED_WCom(0xF0);
  MainOLED_WCom(0x00);

  //Set Memory Addressing Mode
  MainOLED_WCom(0x20);
  MainOLED_WCom(0x02);//Page Addressing Mode
  //Set Lower Column Start Address
  MainOLED_WCom(0x00);
  //Set Higher Column Start Address
  MainOLED_WCom(0x10);

  //Set Display Start Line
  MainOLED_WCom(0x40);

  //Entire Display ON
  MainOLED_WCom(0xA4);//Output follows RAM content

  //Set Display Offset
  MainOLED_WCom(0xD3);
  MainOLED_WCom(0x00);

  //Set Fade Out and Fade in/out
  MainOLED_WCom(0x23);
  MainOLED_WCom(0x00);

  //Set Icon All OFF
  MainOLED_WCom(0x90);
  MainOLED_WCom(0x42);

   MainOLED_WCom(0X78);//SD=0
   MainOLED_WCom(0X38);//RE=0
   MainOLED_WCom(0X0C);//display on

}
```

n SCHEMATIC EXAMPLE

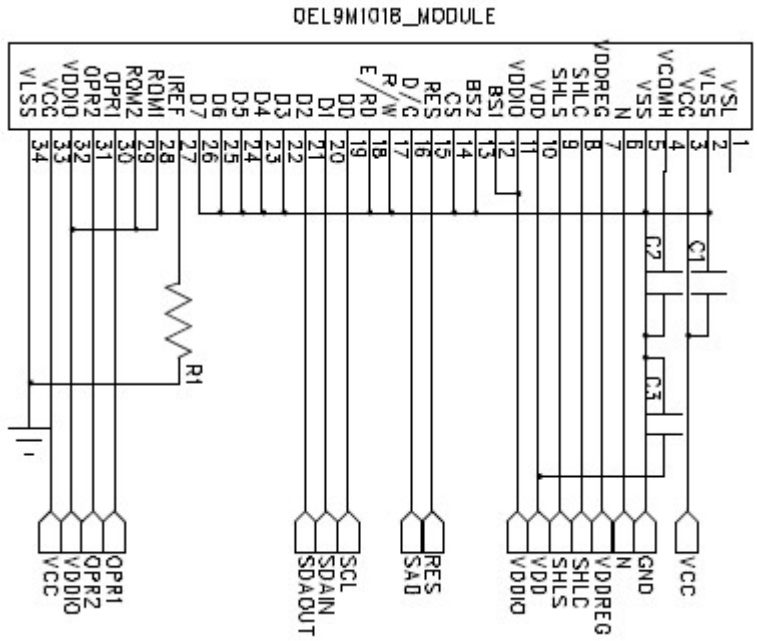
◆8080 parallel Interface Application Circuit:



◆Serial Interface Application Circuit:



◆ IIC Interface Application Circuit:



Note:

1. R1=(V_{CC}-3)V/15uA=(12-3)V/15uA≈667KΩ,C1=C2= 4.7uF, C3=1.0uF;
2. The V_{CC} should connect an external voltage;

n RELIABILITY TESTS

Item		Condition	Criterion
High Temperature Storage (HTS)		85±2℃, 200 hours	1. After testing, the function test is ok. 2. After testing, no addition to the defect. 3. After testing, the change of luminance should be within +/- 50% of initial value. 4. After testing, the change for the mono and area color must be within (+/-0.02, +/- 0.02) and for the full color it must be within (+/-0.04, +/-0.04) of initial value based on 1931 CIE coordinates. 5. After testing, the change of total current consumption should be within +/- 50% of initial value.
High Temperature Operating (HTO)		80±2℃, 96 hours	
Low Temperature Storage (LTS)		-40±2℃, 200 hours	
Low Temperature Operating (LTO)		-30±2℃, 96 hours	
High Temperature / High Humidity Storage (HTHHS)		50±3℃, 90%±3%RH, 120 hours	
Thermal Shock (Non-operation) (TS)		-20±2℃ ~ 25℃ ~ 70±2℃ (30min) (5min) (30min) 10cycles	
Vibration (Packing)	10~55~10Hz,amplitude 1.5mm, 1 hour for each direction x, y, z	1. One box for each test. 2. No addition to the cosmetic and the electrical defects.	
Drop (Packing)	Height : 1 m, each time for 6 sides, 3 edges, 1 angle		
ESD (finished product housing)	±4kV (R: 330Ω C: 150pF , 10times, air discharge)	1. After testing, cosmetic and electrical defects should not happen. 2. In case of malfunction or defect caused by ESD damage, it would be judged as a good part if it would be recovered to normal state after resetting.	

Note： 1) For each reliability test, the sample quantity is 3, and only for one test item.
2) The HTHHS test is requested the Pure Water(Resistance＞10MΩ).
3) The test should be done after 2 hours of recovery time in normal environment.

n OUTGOING QUALITY CONTROL SPECIFICATION

◆Standard

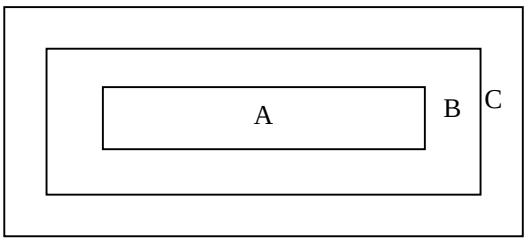
According to GB/T2828.1-2003/ISO 2859-1： 1999 and ANSI/ASQC Z1.4-1993, General Inspection Level II.

◆Definition

1 Major defect : The defect that greatly affect the usability of product.

2 Minor defect : The other defects, such as cosmetic defects, etc.

3 Definition of inspection zone:



Zone A: Active Area

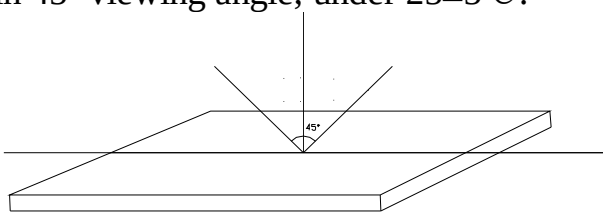
Zone B: Viewing Area except Zone A

Zone C: Outside Viewing Area

Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble of quality and assembly to customer's product.

◆Inspection Methods

1 The general inspection : under 20W x 2 or 40W fluorescent light, about 30cm viewing distance, within 45º viewing angle, under 25±5℃.



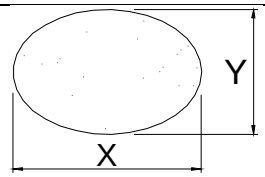
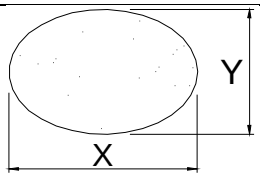
2 The luminance and color coordinate inspection : By PR705 or BM-7 or the equal equipments, in the dark room, under 25±5℃.

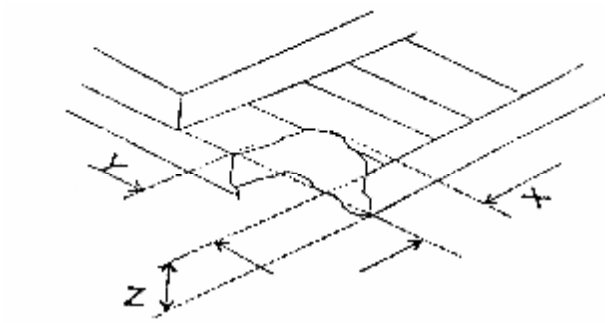
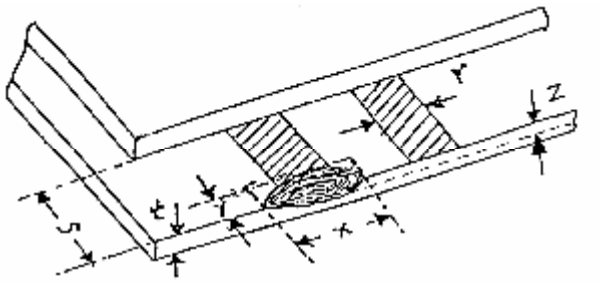
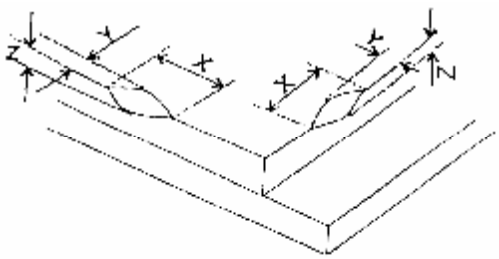
◆Inspection Criteria

1 Major defect : AQL= 0.65

Item	Criterion
Function Defect	1. No display or abnormal display is not accepted
	2. Open or short is not accepted.
	3. Power consumption exceeding the spec is not accepted.
Outline Dimension	Outline dimension exceeding the spec is not accepted.
Glass Crack	Glass crack tends to enlarge is not accepted.

2 Minor Defect : AQL= 1.5

<table>
<tr><td>Item</td><td colspan="4">Criterion</td></tr>
<tr><td rowspan="5">Spot Defect (dimming and lighting spot)</td><td colspan="2">Size (mm)</td><td colspan="2">Accepted Qty</td></tr>
<tr><td colspan="2"></td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="3">  </td><td>Φ≦0.07</td><td colspan="2">Ignored</td></tr>
<tr><td>0.07＜Φ≦0.10</td><td>3</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.10＜Φ≦0. 15</td><td>1</td></tr>
<tr><td colspan="4">Note : Φ= (x + y) / 2</td><td>0.15＜Φ</td><td>0</td></tr>
<tr><td rowspan="5">Line Defect (dimming and lighting line)</td><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.02</td><td colspan="2">Ignored</td></tr>
<tr><td>L≦3.0</td><td>0.02＜W≦0.03</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>L≦2.0</td><td>0.03＜W≦0.05</td><td>1</td></tr>
<tr><td>/</td><td>0.05＜W</td><td>As spot defect</td></tr>
<tr><td colspan="5">Remarks: The total of spot defect and line defect shall not exceed 4 pcs. The distance between two lines defects must exceed 1 mm</td></tr>
<tr><td>Polarizer Stain</td><td colspan="4">Stain which can be wiped off lightly with a soft cloth or similar cleaning is accepted, otherwise, according to the Spot Defect and the Line Defect.</td></tr>
<tr><td rowspan="7">Polarizer Scratch</td><td colspan="4">1. If scratch can be seen during operation, according to the criterions of the Spot Defect and the Line Defect.</td></tr>
<tr><td colspan="4">2. If scratch can be seen only under non-operation or some special angle, the criterion is as below :</td></tr>
<tr><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.02</td><td colspan="2">Ignore</td></tr>
<tr><td>3.0＜L≦5.0</td><td>0.02＜W≦0.04</td><td>2</td><td rowspan="3">Ignore</td></tr>
<tr><td>L≦3.0</td><td>0.04＜W≦0.06</td><td>1</td></tr>
<tr><td>/</td><td>0.06＜W</td><td>0</td></tr>
<tr><td rowspan="5">Polarizer Air Bubble</td><td colspan="2">Size</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="3">  </td><td>Φ≦0.20</td><td colspan="2">Ignored</td></tr>
<tr><td>0.20＜Φ≦0.30</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.30＜Φ≦0.50</td><td>1</td></tr>
<tr><td></td><td>0.50＜Φ</td><td>0</td></tr>
</table>

<table>
<tr><td rowspan="4">Glass Defect (Glass Chiped)</td><td>1. On the corner
 
(mm)
<table><tr><td>x</td><td>≤ 1.5</td></tr><tr><td>y</td><td>≤ 1.5</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>2. On the bonding edge
 
(mm)
<table><tr><td>x</td><td>≤ a / 4</td></tr><tr><td>y</td><td>≤ s / 3 &≤0.7</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>3. On the other edges
 
(mm)
<table><tr><td>x</td><td>≤ a / 8</td></tr><tr><td>y</td><td>≤ 0.7</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>Note: t: glass thickness ; s: pad width ; a: the length of the edge</td></tr>
<tr><td>TCP Defect</td><td>Crack, deep fold and deep pressure mark on the TCP are not accepted</td></tr>
<tr><td>Pixel Size</td><td>The tolerance of display pixel dimension should be within ±20% of the spec</td></tr>
<tr><td>Luminance</td><td>Refer to the spec or the reference sample</td></tr>
<tr><td>Color</td><td>Refer to the spec or the reference sample</td></tr>
</table>

n CAUTIONS IN USING OLED MODULE

◆Precautions For Handling OLED Module:

1. OLED module consists of glass and polarizer. Pay attention to the following items when handling:
   i. Avoid drop from high, avoid excessive impact and pressure.
   ii. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead.
   iii. If the surface becomes dirty, breathe on the surface and gently wipe it off with a soft dry cloth. If it is terrible dirty, moisten the soft cloth with Isopropyl alcohol or Ethyl alcohol. Other solvents may damage the polarizer. Especially water, Ketone and Aromatic solvents.
   iv. Wipe off saliva or water drops immediately, contact the polarizer with water over a long period of time may cause deformation.
   v. Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peeling-off may occur with high temperature and high humidity.
   vi. Condensation on the surface and the terminals due to cold or anything will damage, stain or dirty the polarizer, so make it clean as the way of iii.
2. Do not attempt to disassemble or process the OLED Module.
3. Make sure the TCP or the FPC of the Module is free of twisting, warping and distortion, do not pull or bend them forcefully, especially the soldering pins. On the other side, the SLIT part of the TCP is made to bend in the necessary case.
4. When assembling the module into other equipment, give the glass enough space to avoid excessive pressure on the glass, especially the glass cover which is much more fragile.
5. Be sure to keep the air pressure under 120 kPa, otherwise the glass cover is to be cracked.
6. Be careful to prevent damage by static electricity:
   i. Be sure to ground the body when handling the OLED Modules.
   ii. All machines and tools required for assembling, such as soldering irons, must be properly grounded.
   iii. Do not assemble and do no other work under dry conditions to reduce the amount of static electricity generated. A relative humidity of 50%-60% is recommended.
   iv. Peel off the protective film slowly to avoid the amount of static electricity generated.
   v. Avoid to touch the circuit, the soldering pins and the IC on the Module by the body.
   vi. Be sure to use anti-static package.
7. Contamination on terminals can cause an electrochemical reaction and corrade the terminal circuit, so make it clean anytime.
8. All terminals should be open, do not attach any conductor or semiconductor on the terminals.
9. When the logic circuit power is off, do not apply the input signals.
10. Power on sequence: $V_{DD} \rightarrow V_{CC}$, and power off sequence: $V_{CC} \rightarrow V_{DD}$.
11. Be sure to keep temperature, humidity and voltage within the ranges of the spec, otherwise shorten Module’ s life time, even make it damaged.
12. Be sure to drive the OLED Module following the Specification and datasheet of IC controller, otherwise something wrong may be seen.

13.When displaying images, keep them rolling, and avoid one fixed image displaying more than 30 seconds, otherwise the residue image is to be seen. This is the speciality of OLED.

◆Precautions For Soldering OLED Module:

1. Soldering temperature : 260°C ± 10°C.
2. Soldering time : 3-4 sec.
3. Repeating time : no more than 3 times.
4. If soldering flux is used, be sure to remove any remaining flux after finishing soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended to protect the surface with a cover during soldering to prevent any damage due to flux spatters.

◆ Precautions For Storing OLED Module:

1. Be sure to store the OLED Module in the vacuum bag with dessicant.
2. If the Module can not be used up in 1 month after the bag being opened, make sure to seal the Module in the vacuum bag with dessicant again.
3. Store the Module in a dark place, do not expose to sunlight or fluorescent light.
4. The polarizer surface should not touch any other objects. It is recommended to store the Module in the shipping container.
5. It is recommended to keep the temperature between 0°C and 30°C , the relative humidity not over 60%.

◆ Limited Warranty

Unless relevant quality agreements signed with customer and law enforcement, for a period of 12 months from date of production, all products (except automotive products) TRULY will replace or repair any of its OLED modules which are found to be functional defect when inspected in accordance with TRULY OLED acceptance standards (copies available upon request). Cosmetic/visual defects must be returned to TRULY within 90 days of shipment. Confirmation of such date should be based on freight documents. The warranty liability of TRULY is limited to repair and/or replacement on the terms above. TRULY will not be responsible for any subsequent or consequential events.

◆Return OLED Module Under Warranty:

1. No warranty in the case that the precautions are disregarded.
2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects.

◆PRIOR CONSULT MATTER

1. For TRULY standard products , we keep the right to change material ,process … for improving the product property without any notice on our customer.
2. If you have special requirement about reliability condition, please let us know before you start the test on our samples.