

SPDT SWITCH GaAs MMIC

■ FEATURES

- AEC-Q100 grade 1 qualified
- Control voltage V_{CTL(H)} = 3.0 V typ.
- Low insertion loss

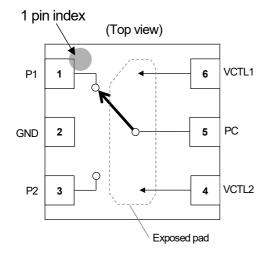
0.35 dB typ. @ f = 0.3 to 2.5 GHz 0.45 dB typ. @ f = 4.9 to 5.9 GHz 0.60 dB typ. @ f = 8.5 GHz

- High isolation
 28 dB typ. @ f = 0.3 to 2.5 GHz
 27 dB typ. @ f = 4.9 to 5.9 GHz
 18 dB typ. @ f = 8.5 GHz
- P-1dB = +31 dBm typ. @ f = 0.3 GHz, 2.5 GHz, 5.9 GHz
- Wide operating temperature -40 to +125°C
- Package with wettable flank ESON6-GC (1.6 x 1.6 x 0.78 mm typ., pin pitch 0.5 mm)
- RoHS compliant and Halogen Free, MSL1

■ APPLICATION

- 802.11 a/b/g/n/ac/ax and BT networks applications
- UWB (ultra-wide band) applications
- RKE applications
- General purpose switching applications

BLOCK DIAGRAM (ESON6-GC)



■ GENERAL DESCRIPTION

The NJG1801BKGC-A is an ultra-wide band SPDT switch for automotive suited for WiFi, Bluetooth, UWB applications and so on.

This switch features low insertion loss and high isolation covering up to 8.5 GHz.

ESON6-GC package with wettable flank structure corresponds to Automated Optical Inspection (AOI) which has strong demands from automotive customers.

TRUTH TABLE

"H" = $V_{CTL(H)}$, "L" = $V_{CTL(L)}$

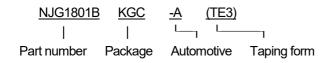
VCTL1	VCTL2	ON Path
L	Н	PC-P1
Н	L	PC-P2

■ PIN CONFIGURATION

PIN NO.	SYMBOL	DESCRIPTION
1	P1	RF input/output
2	GND	Ground terminal
3	P2	RF input/output
4	VCTL2	Control signal input
4	VUILZ	terminal
5	PC	RF input/output
6	VCTL1	Control signal input
0	VOILI	terminal
Exposed	GND	Ground terminal
pad		

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PRODUCT NAME INFORMATION



ORDERING INFORMATION

PART NUMBER	PACKAGE OUTLINE	RoHS	HALOGEN- FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs.)
NJG1801BKGC-A	ESON6-GC	Yes	Yes	SnBi	1801B A	5.4	3,000

ABSOLUTE MAXIMUM RATINGS

(General conditions: $T_a = +25^{\circ}C$, $Z_s = Z_l$				
PARAMETER	SYMBOL	RATINGS	UNIT	
RF Input Power	PIN	+31 ⁽¹⁾	dBm	
Control Voltage	Vctl	6.0	V	
Power Dissipation ⁽²⁾	PD	1100	mW	
Operating Temperature	T _{opr}	-40 to +125	°C	
Storage Temperature	T _{stg}	-55 to +150	°C	

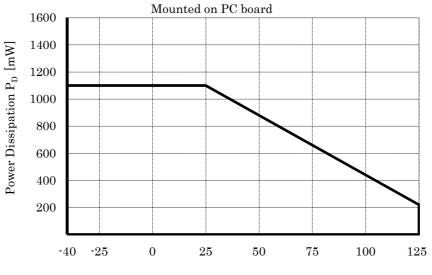
(1): $V_{CTL(L)} = 0 V$, $V_{CTL(H)} = 3.0 V$, on state port

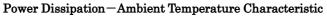
(2): 4-layer FR4 PCB with through-hole (101.5 x 114.5 mm), Tj = 150°C

■ POWER DISSIPATION VS.AMBIENT TEMPERATURE

Please, refer to the following Power Dissipation and Ambient Temperature.

(Please note the surface mount package has a small maximum rating of Power Dissipation [P_D], a special attention should be paid in designing of thermal radiation.)





Ambient Temperature $Ta[^{\circ}C]$

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■ ELECTRICAL CHARACTERISTICS 1 (DC CHARACTERISTICS)

		(General conditions:	$I_a = +25$	°C, with a	applicatic	on circuit)
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Control Voltage (HIGH)	Vctl(H)		1.8	3.0	5.0	V
Control Voltage (LOW)	Vctl(L)		-0.2	-	0.2	V
Control Current	Іст∟		-	5	10	μA

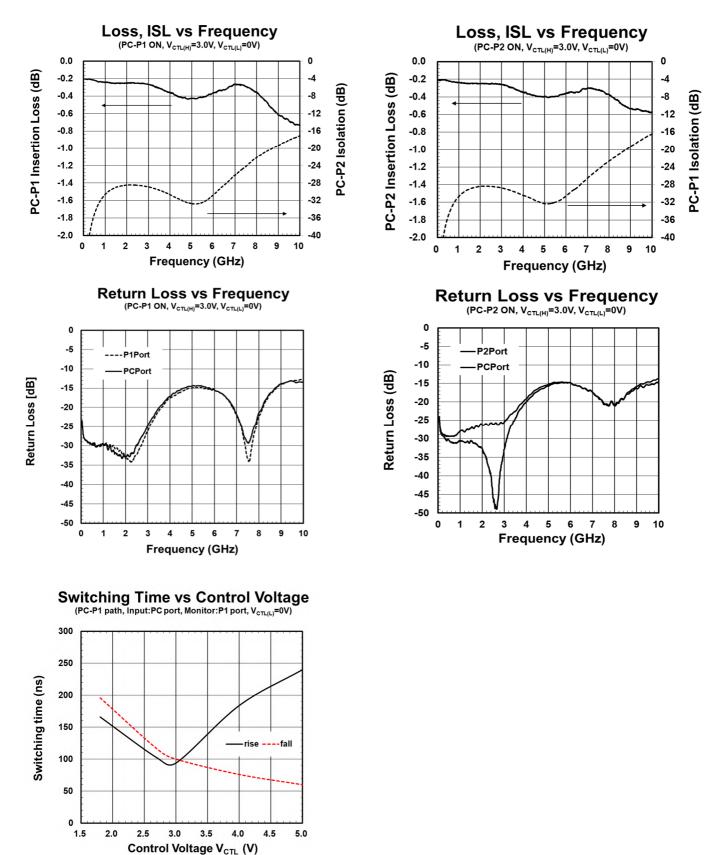
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■ ELECTRICAL CHARACTERISTICS 2 (RF CHARACTERISTICS)

(Gene	(General conditions: $V_{CTL(H)} = 3.0 \text{ V}$, $V_{CTL(L)} = 0 \text{ V}$, $T_a = +25^{\circ}\text{C}$, $Z_S = Z_I = 50 \Omega$, with application circuit)					
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Insertion loss1	LOSS1	f = 0.3 to 2.5 GHz	-	0.35	0.55	dB
Insertion loss2	LOSS2	f = 4.9 to 5.9 GHz	-	0.45	0.70	dB
Insertion loss3	LOSS3	f = 8.5 GHz	-	0.60	0.80	dB
Isolation1	ISL1	f = 0.3 to 2.5 GHz	25	28	-	dB
Isolation2	ISL2	f = 4.9 to 5.9 GHz	24	27	-	dB
Isolation3	ISL3	f = 8.5 GHz	16	18	-	dB
Return loss1	RL1	f = 0.3 to 2.5 GHz	18	28	-	dB
Return loss2	RL2	f = 4.9 to 5.9 GHz	10	15	-	dB
Return loss3	RL3	f = 8.5 GHz	10	14	-	dB
Input power at 1dB compression point1	P-1dB1	f = 0.3 to 2.5 GHz	+29	+31	-	dBm
Input power at 1dB compression point2	P-1dB2	f = 4.9 to 5.9 GHz	+28	+31	-	dBm
Input power at 1dB compression point3	P-1dB3	f = 8.5 GHz	+11	-	-	dBm
Switching time	Tsw	50% V _{CTL} to 10%/90% RF	-	100	300	ns

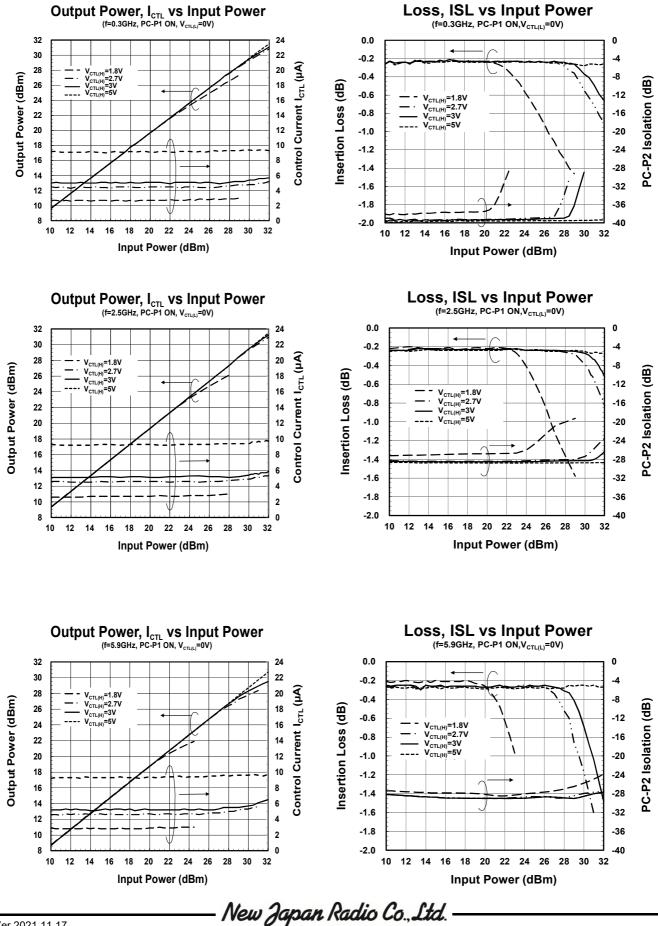
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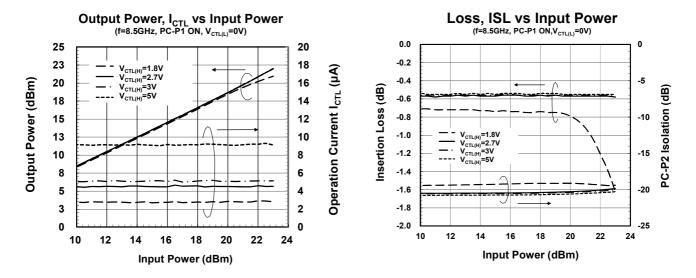
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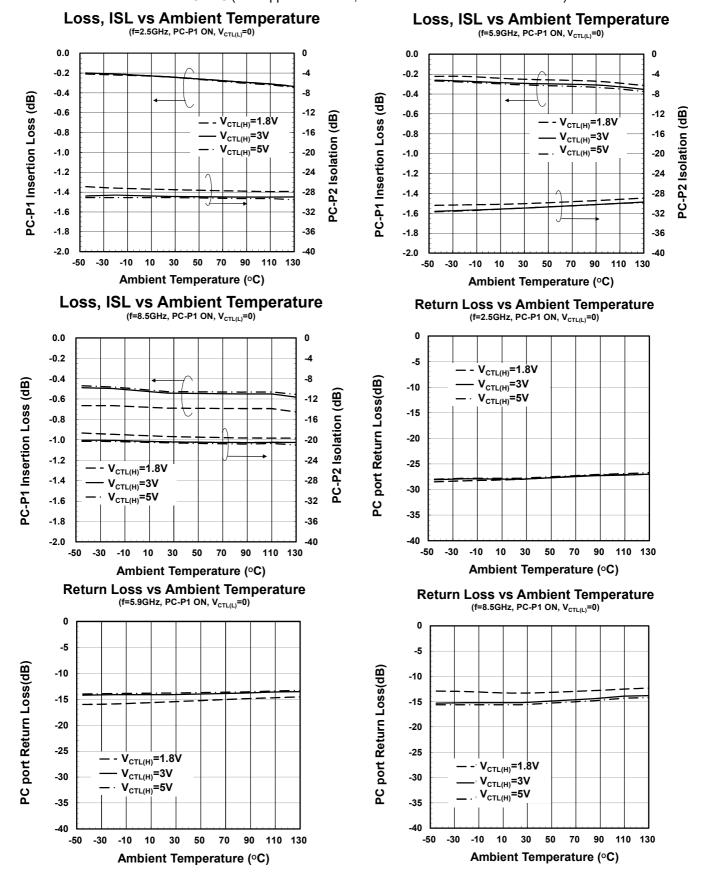
http://www.njr.com/





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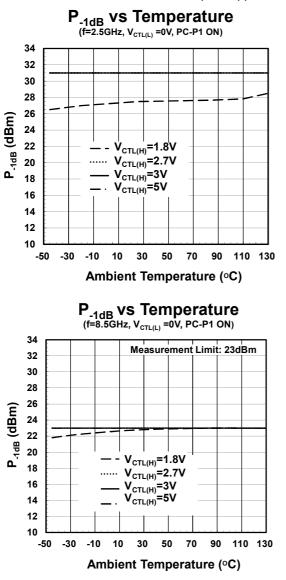


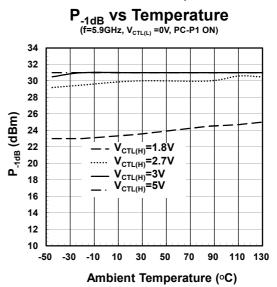


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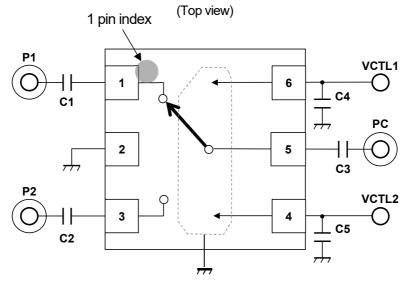




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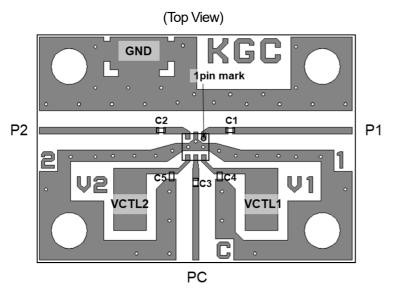
■ APPLICATION CIRCUIT



PARTS LIST

Part ID	Value	Notes
C1 to C3	1000 pF	GRM0335C1E102GA01D
C4 to C5	10 pF	GRM0335C1E100GA01D

RECOMMENDED PCB DESIGN



PCB (FR-4): t = 0.2 mm MICROSTRIP LINE WIDTH = 0.4 mm (Z_0 = 50 Ω) PCB SIZE = 19.4 x 14.0 mm

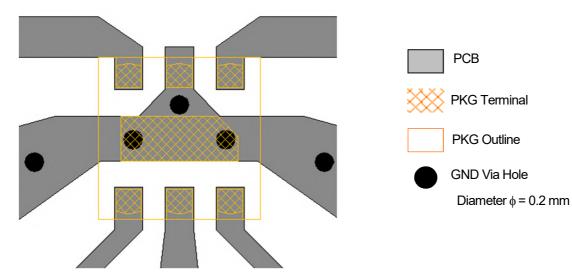
Losses of PCB, capacitors and connectors, Ta = +25°C

Frequency [GHz]	Loss [dB]
0.3	0.14
2.4	0.38
2.5	0.39
4.9	0.59
5.9	0.73
8.5	0.91

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<PCB LAYOUT GUIDELINE>



PRECAUTIONS

- [1] The DC blocking capacitors (C1, C2, C3) should be placed at RF terminals. Please choose appropriate capacitance value at the application frequency.
- [2] For avoiding the degradation of RF performance, the bypass capacitors (C4, C5) should be placed as close as possible to VCTL terminals.
- [3] For good RF performance, GND terminal must be connected to PCB ground plane of substrate, and through -holes should be placed near the IC.
- [4] For good RF performance, exposed pad should be connected to PCB ground plane of substrate, and through -holes should be placed near the IC.

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■ HANDLING PRECAUTIONS

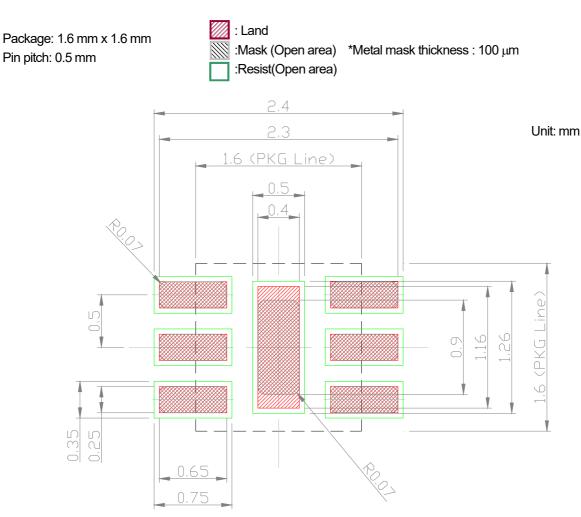
	PIN NO. SYMBOL		ESD RATINGS			
PIN NO.	STIVIDUL	Human Bo	Human Body Model ⁽¹⁾			
Commo	n terminal	Ground	I/O	Device		
Common	I terminai	Ground		Model ⁽²⁾		
1	P1	Class 1C	Class 2	Class C6		
2	GND	COM.	-	Class C6		
3	P2	Class 1C	Class 2	Class C6		
4	VCTL2	Class 0B	Class 0B	Class C6		
5	PC	Class 2	Class 2	Class C6		
6	VCTL1	Class 0B	Class 0B	Class C6		

(1): According to JEDEC JS-001

(2): According to JEDEC JS-002

CAUTION: This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.

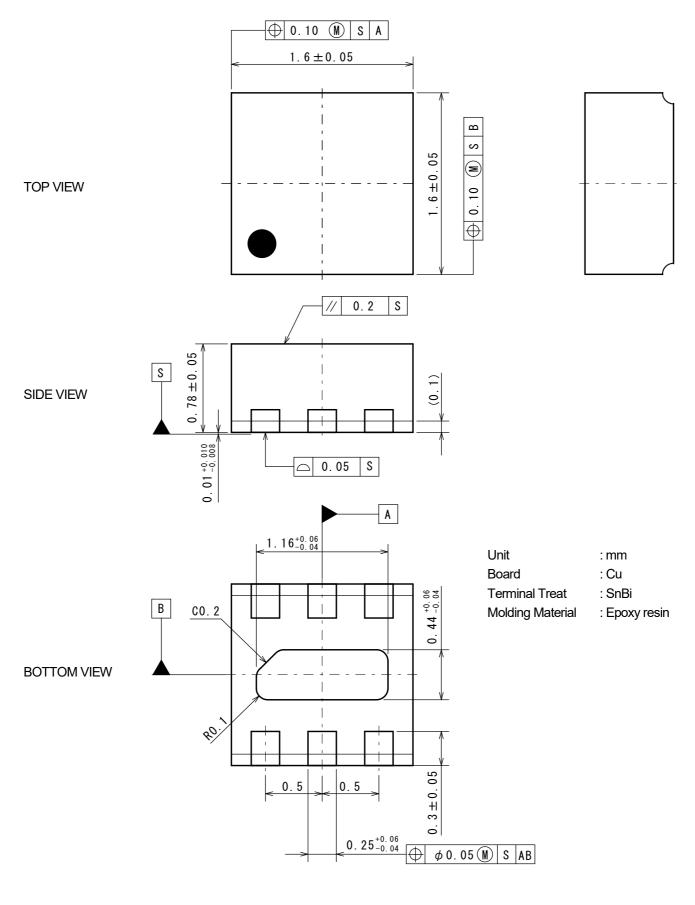
■ RECOMMENDED FOOTPRINT PATTERN (ESON6-GC PACKAGE) <Reference>



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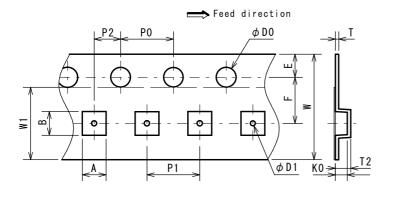
■ PACKAGE OUTLINE (ESON6-GC)



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■ PACKING SPECIFICATION (ESON6-GC)

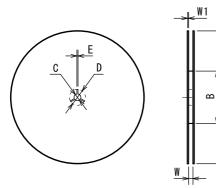
TAPING DIMENSIONS



SYMBOL	DIMENSION	REMARKS
A	1.80±0.05	BOTTOM DIMENSION
В	1.80±0.05	BOTTOM DIMENSION
DO	1.5 ^{+0.1}	
D1	0. 5 ^{+0. 1}	
E	1.75±0.1	
F	3.5±0.05	
P0	4.0±0.1	
P1	4.0±0.1	
P2	2.0±0.05	
T	0.25±0.05	
T2	1.28±0.07	
KO	0.93±0.05	
W	8.0 ^{+0.3} -0.1	
W1	5.5	THICKNESS 0.1max

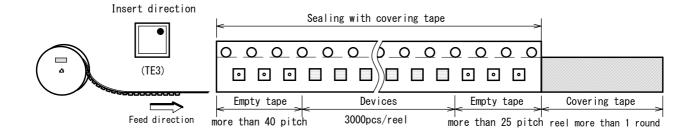
UNIT: mm

REEL DIMENSIONS

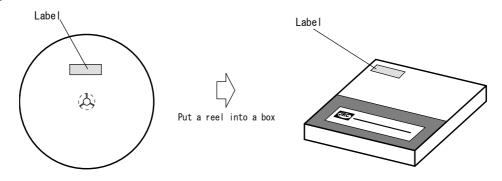


SYMBOL	DIMENSION
A	ϕ 180 $_{-1.5}^{0}$
В	ϕ 60 $^{+1}_{0}$
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	9 ^{+0.3}
W1	1.2

TAPING STATE



PACKING STATE



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■ REVISION HISTORY

Date	Revision	Changes		
17.Nov.2021 Ver.1.3		Revised ELECTRICAL CHARACTERISTICS 1		
		Revised RECOMMENDED PCB DESIGN		
5.Nov.2021	Ver.1.2 Revised RECOMMENDED FOOTPRINT PATTERN			
22.Dec.2020	Ver.1.1	Revised GENERAL DESCRIPTION		
22.Dec.2020 Ver.1.1		Revised POWER DISSIPATION VS.AMBIENT TEMPERATURE (derating curve)		
20.Aug.2020	Ver.1.0	New Release		

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