Serial Input Parallel Output 8-channel Sink Driver

■FEATURES

- ●8-channel SIPO
- ●Cascade Connection
- ●Supply Voltage V_{DD}=3.0 to 5.5V
- ●Output Voltage V_{DS}=up to 40V (45V Rating)
- ●Output Current 300mA(Peak) / ch.
- ●Built-in Noise Filter (CLRb Pin)
- ●Protection Circuit OCP, TSD
- ●Output Slew Rate Control
- ●Operating Temperature Topr=-40 to 125°C
- ●Package Outline HTSSOP24-P1

■GENERAL DESCRIPTION

The NJW4829 is 8-channel sink driver with 300mA output.

The input section corresponds to 8 bit serial communication and cascade connection is also possible.

The CLRb input has built-in filter for noise immunity.

Supply voltage and input voltage correspond to 5V logic, maximum rating of output voltage is 45V.

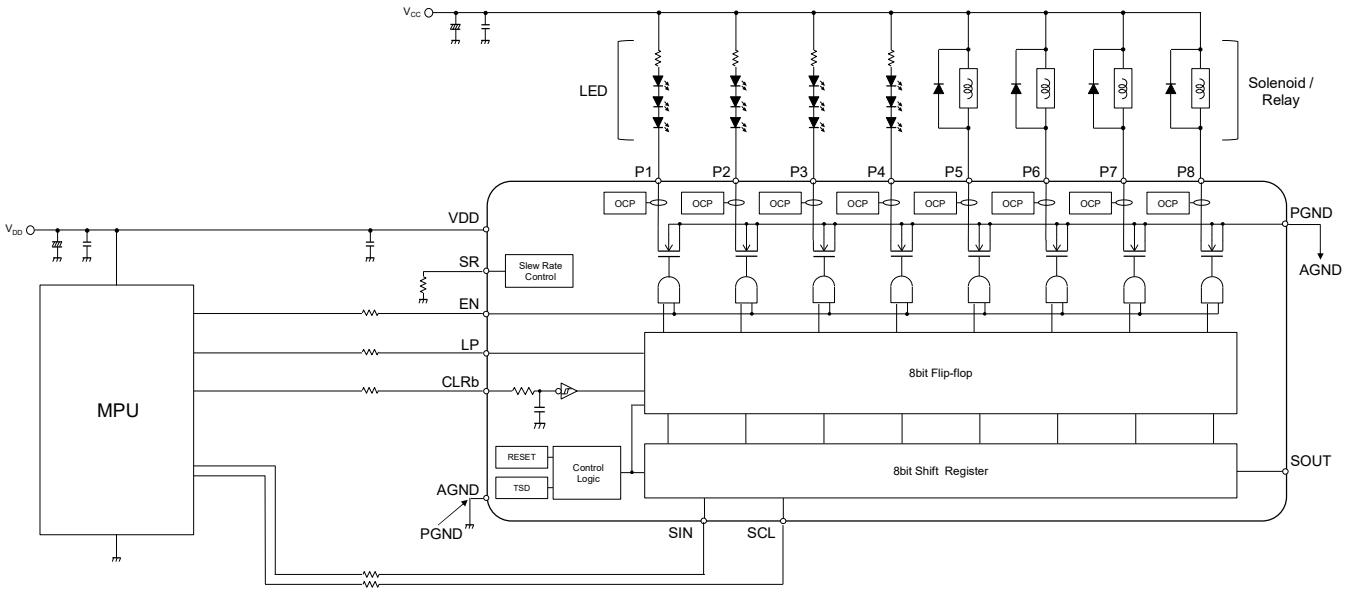
The protection circuits have over current protection (OCP) and thermal shutdown (TSD).

Moreover, because it has built-in output slew rate adjustment function, it can be applied as EMI countermeasure.

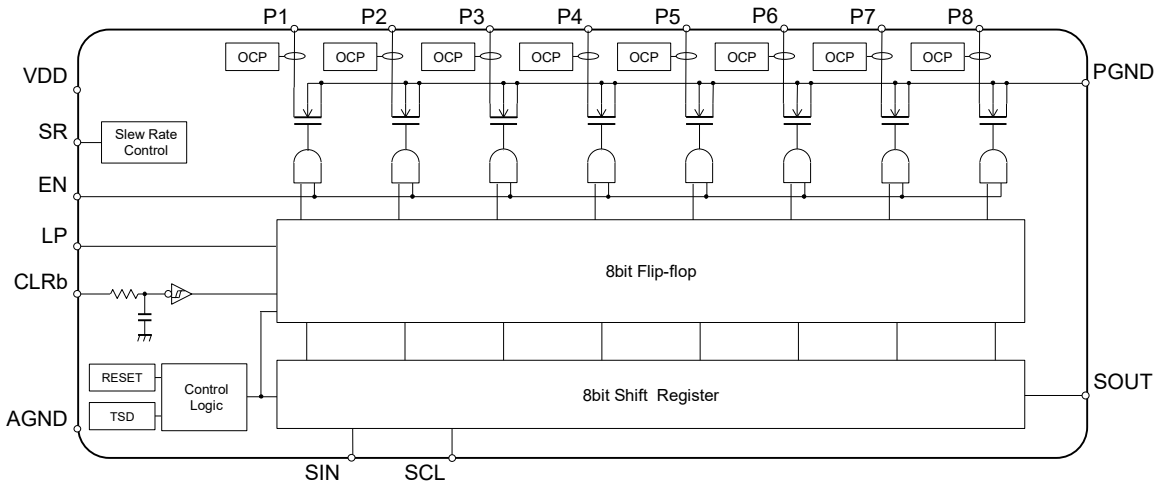
■APPLICATION

LED, Relay and Solenoid applications
for industrial equipment and home appliance

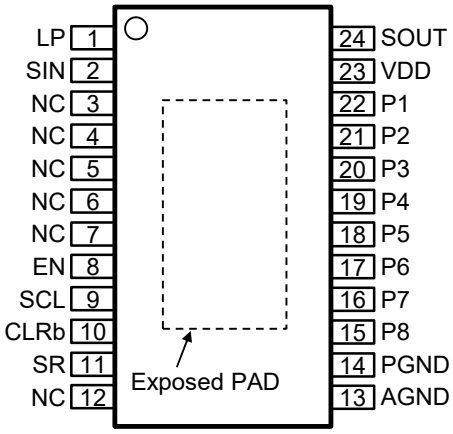
■TYPICAL APPLICATION



■BLOCK DIAGRAM

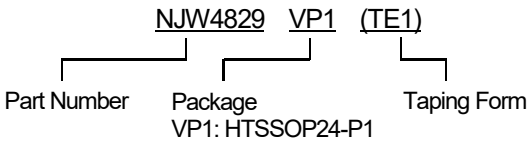


■PIN CONFIGURATION



PIN NO.	SYMBOL	I/O	DESCRIPTION
1	LP	I	Latch Signal Input Pin
2	SIN	I	Serial Data Input Pin
3	NC	-	Not Internally Connected
4			
5			
6			
7			
8	EN	I	Output Enable Signal Input Pin
9	SCL	I	Shift Clock Input Pin
10	CLRb	I	Clear Signal Input Pin
11	SR	-	Output Slew Rate Setting Pin
12	NC	-	Not Internally Connected
13	AGND	-	Control Block Ground Pin
14	PGND	-	Output Block Ground Pin
15	P8	O	Parallel Output Pin
16	P7	O	
17	P6	O	
18	P5	O	
19	P4	O	
20	P3	O	
21	P2	O	
22	P1	O	
23	VDD	-	Power Supply Pin
24	SOUT	O	Serial Data Output Pin
-	Exposed PAD	-	Back Side Thermal PAD It must be set to open or connected to AGND

■PRODUCT NAME INFORMATION



■ORDERING INFORMATION

PRODUCT NAME	PACKAGE OUTLINE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ(pcs)
NJW4829VP1(TE1)	HTSSOP24-P1	yes	yes	Ni/Pd/Au	4829	83	2500

■ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT	NOTE
Supply Voltage	V_{DD}	-0.3 to +7	V	VDD Pin
Output Pin Voltage 1	V_{DS}	-0.3 to +45	V	P1 to P8 Pin
Output Pin Voltage 2	V_O	-0.3 to V_{DD}	V	SOUT Pin
Input Pin Voltage	V_{IN}	-0.3 to V_{DD}	V	SIN, EN, SCL, LP, CLRb Pin
Output Current	I_{DS}	300	mA	P1 to P8 Pin
Power Dissipation (Ta=25°C) HTSSOP24-P1	P_D	1200(1)	mW	
		1600(2)		
		3200(3)		
Junction Temperature	Tj	-40 to +150	°C	
Operating Temperature	Topr	-40 to +125	°C	
Storage Temperature	Tstg	-50 to +150	°C	

(1): Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 2Layers FR-4, applied Exposed Pad)

(2): Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, not applied Exposed Pad)
(For 4Layers: Applying 99.5×99.5mm inner Cu area to a board based on JEDEC standard JESD51-5)

(3): Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, applied Exposed Pad)
(For 4Layers: Applying 99.5×99.5mm inner Cu area and thermal via holes to a board based on JEDEC standard JESD51-5)

■RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	3.0 to 5.5	V
Output Pin Voltage	V_{DS}	0 to 40	V
Output Current(4)	I_{DS}	0 to 300	mA

(4): Caution that the total power consumption of P1 to P8 does not exceed the power dissipation of rating.

■**ELECTRICAL CHARACTERISTICS (DC Parameter)** (Unless otherwise noted, V_{DD}=5V, R_{SR}=500kΩ, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent Current 1	I_{Q1}	All outputs OFF	-	1.4	2.8	mA
Quiescent Current 2	I_{Q2}	All outputs ON	-	1.6	3.2	mA
H level Input Voltage 1	V_{IH1}	SIN, EN, SCL, LP, CLRb Pin	$0.7V_{DD}$	-	V_{DD}	V
H level Input Voltage 2	V_{IH2}	V_{DD}=3V, SIN, EN, SCL, LP, CLRb Pin	$0.7V_{DD}$	-	V_{DD}	V
L level Input Voltage 1	V_{IL1}	SIN, EN, SCL, LP, CLRb Pin	0	-	$0.3V_{DD}$	V
L level Input Voltage 2	V_{IL2}	V_{DD}=3V, SIN, EN, SCL, LP, CLRb Pin	0	-	$0.3V_{DD}$	V
H level Input Current	I_{IH}	V_{DD}=5.5V, V_{IN}=5.5V, SIN, EN, SCL, LP, CLRb Pin	-	-	1	μA
L level Input Current	I_{IL}	V_{DD}=5.5V, V_{IN}=0V, SIN, EN, SCL, LP, CLRb Pin	-	-	1	μA
Output ON Resistance 1	R_{ON1_P}	V_{SR}=0V, I_{DS}=100mA, P1 to P8 Pin	-	0.9	2.7	Ω
Output ON Resistance 2	R_{ON2_P}	V_{DD}=3V, V_{SR}=0V, I_{DS}=100mA, P1 to P8 Pin	-	1	3	Ω
Maximum Output Current	I_{DMAX_P}	V_{SR}=0V, P1 to P8 Pin	300	-	-	mA
Output Leak Current	I_{LEAK_P}	V_{DS}=40V, P1 to P8 Pin	-	-	1	μA
Thermal Shutdown Operating Temperature	T_{TSD_DET}		-	170	-	°C
Thermal Shutdown Recovery Temperature	T_{TSD_REV}		-	150	-	°C
SOUT Pin “L” Output Voltage	V_{OL_SOUT}	I_{SOUT}=4mA	-	0.2	0.4	V
SOUT Pin “H” Output Voltage	V_{OH_SOUT}	I_{SOUT}=-4mA	4.6	4.8	-	V

■**ELECTRICAL CHARACTERISTICS (Switching Parameter)**

(Unless otherwise noted, V_{DD}=5V, V_{CC}=24V, CL=30pF(P-PGND), R_L=240Ω(P-V_{CC}), Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output "H-L" Transition Time	t_{THL}	R_{SR}=500kΩ	-	2.5	-	μs
Output "L-H" Transition Time	t_{TLH}	R_{SR}=500kΩ	-	1.8	-	μs
Output "H-L" Propagation Delay Time (LP-P)	t_{pdHL_LP}	V_{SR}=0V	-	0.2	-	μs
Output "L-H" Propagation Delay Time (LP-P)	t_{pdLH_LP}	V_{SR}=0V	-	0.9	-	μs
LP "H" Pulse Width	t_{W_LP}		90	-	-	ns
CLRb "L" Pulse Width	t_{W_CLRb}		5	-	-	μs
SIN Setup Time for SCL	t_{SU_SIN}		40	-	-	ns
SIN Hold Time for SCL	t_{HD_SIN}		40	-	-	ns
SCL "H" Pulse Width	t_{W_SCL}		50	-	-	ns
SCL Maximum Operating Frequency	f_{MAX_SCL}		10	-	-	MHz
SCL Setup Time for LP	t_{SU_SCL}		30	-	-	ns
LP Setup Time for SCL	t_{SU_LP}		30	-	-	ns
SOUT Output Delay Time (SCL-SOUT)	t_{pd_SOUT}		-	-	50	ns
Output "H-L" Propagation Delay Time (EN-P)	t_{pdHL_EN}	V_{SR}=0V	-	0.2	-	μs
Output "L-H" Propagation Delay Time (EN-P)	t_{pdLH_EN}	V_{SR}=0V	-	0.9	-	μs

■THERMAL CHARACTERISTICS

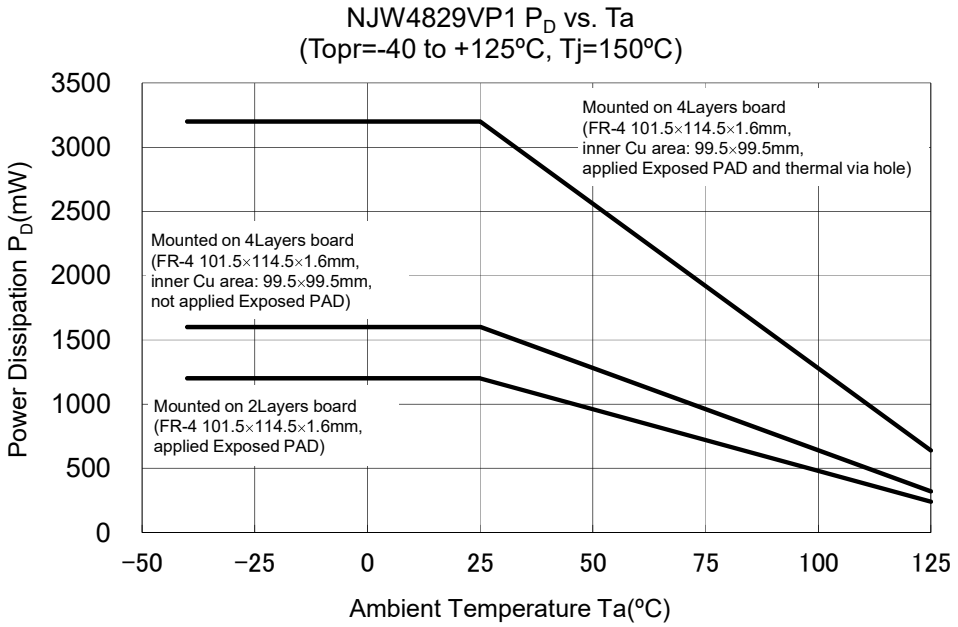
PARAMETER	SYMBOL	VALUE	UNIT
Junction to ambient thermal resistance	θja	103(5) 78(6) 39(7)	°C/W
Junction to top of package characterization parameter	ψjt	13(5) 13(6) 6(7)	°C/W

(5): Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 2Layers FR-4, applied Exposed Pad)

(6): Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, not applied Exposed Pad)
(For 4Layers: Applying 99.5×99.5mm inner Cu area to a board based on JEDEC standard JESD51-5)

(7): Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, applied Exposed Pad)
(For 4Layers: Applying 99.5×99.5mm inner Cu area and thermal via holes to a board based on JEDEC standard JESD51-5)

■POWER DISSIPATION vs. AMBIENT TEMPERATURE



■APPLICATION NOTE / GLOSSARY

●Truth Table

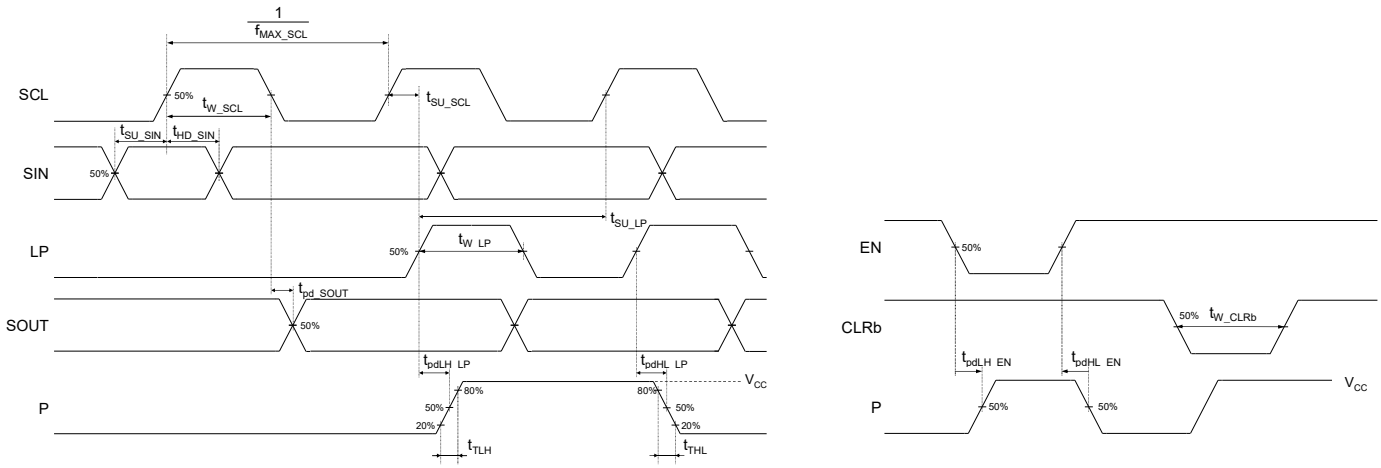
INPUT				P OUTPUT (with pull-up resistor)	OPERATION
CLRb	EN	SCL	LP		
L	X	X	X	All OFF (H)	Reset all latch circuit and protection circuit, and P OUTPUT becomes all OFF. The data of shift register does not change.
X	L	X	X	All OFF (H)	P OUTPUT becomes all OFF. The data of shift register and latch circuit does not change
H	H	↑	X	P0	The logic state of the SIN pin is taken into the shift register. The data of latch circuit and P OUTPUT do not change
		X	↑	P	The all data P of shift register are transferred to the latch circuit and reflected on P OUTPUT
		↓	X	P0	No change
		X	↓		

↑ : Change from "L" to "H"　　H : High Level　　X : Don't Care

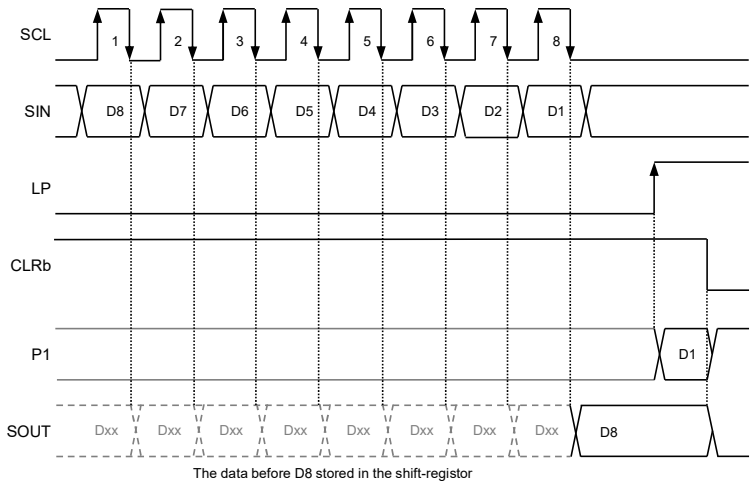
↓ : Change from "H" to "L"　　L : Low Level

P0 : The P output level just before input condition in the above table

●Timing Chart / Timing Definition



●Serial Data Output Timig



The data before D8 stored in the shift-registor

●Serial Data Input (SIN Pin)
The logic state of the SIN pin is taken into the 8-bit shift register as MSB first every rising edge of the shift clock.
The data D1 (LSB) to D8 (MSB) of the shift register and latch circuit in the IC correspond to the output logic of P1 to P8.

●Shift Clock Input (SCL Pin)
When the rising edge is input to the SCL pin, the logic state of the SIN pin is taken into the shift register.
When the falling edge is input to the SCL pin, the MSB data stored in the shift register is output from SOUT.
The data of latch circuit and P OUTPUT do not change.

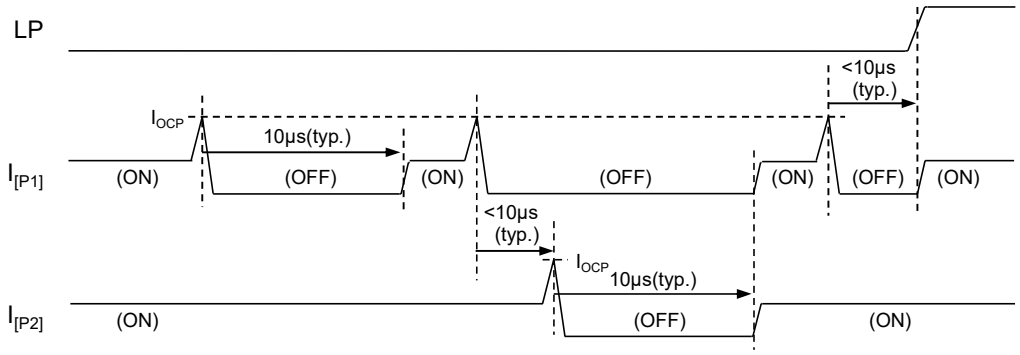
●Latch Signal Input (LP Pin)
When the rising edge is input to the LP pin, the all data of shift register are transferred to the latch circuit and reflected on P output.

●Clear Signal Input (CLRb Pin)
When the CLRb pin is "L", all latch circuits and protection circuits are reset, and all P outputs are turned OFF.
The data of shift register does not change.

●Output Enable Signal Input (EN pin)
When the EN pin is "L", all P outputs are turned OFF.
The data of shift register and latch circuit does not change
It is also possible to directly PWM control the P output in the ON state by inputting the PWM signal.

●Serial Data Output (SOUT pin)
It is used for cascade connection.
The SOUT pin outputs serial data stored in the shift register at the falling edge of SCL pin without being affected by the CLRb, EN, and LP pins.

●Over Current Protection Circuit (OCP)
Overcurrent detection operates for each P1 - P8 output.
When overcurrent is detected, the corresponding P output is turned OFF.
After overcurrent is detected, when data is reset or passage of internal recovery time(10µs typ.), it returns to normal operation.
In the condition of the P output is already overcurrent detected and turned off, if another P output is detected continuously, all the recovery timing of the corresponding P outputs will be all taken over.



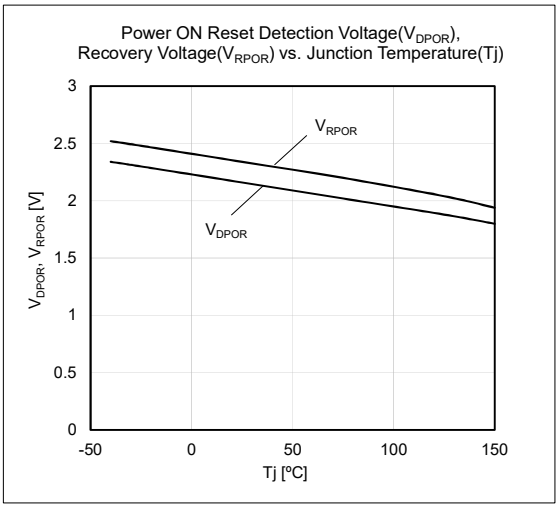
●Thermal Shutdown Circuit (TSD)
When the junction temperature inside the IC exceeds T_{TSD_DET}, all P outputs are turned OFF.
When the internal junction temperature drops to T_{TSD_REV} or less, it returns to normal operation state.
Even if TSD operates, reception of each input signal and serial data output are performed.
However, even if data is updated by the latch signal (LP) while TSD operating, this data will be reflected to the output at time of returning to the normal operation state.

●Power ON Reset Function

The power supply pin has built-in power on reset function.
When the V_{DD} voltage below V_{DPOR} (typ.), all outputs are turned off and all internal states (shift register, latch circuit and protection circuit) are initialized.

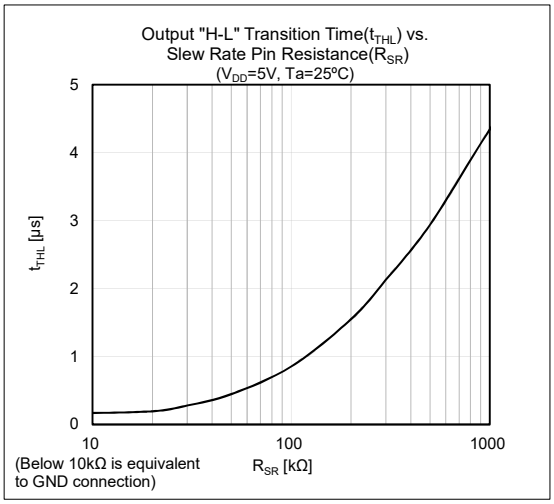
Therefore, when POR release such as the power-on, the data (D1 to D8) stored in the shift register and latch circuit are all L level.

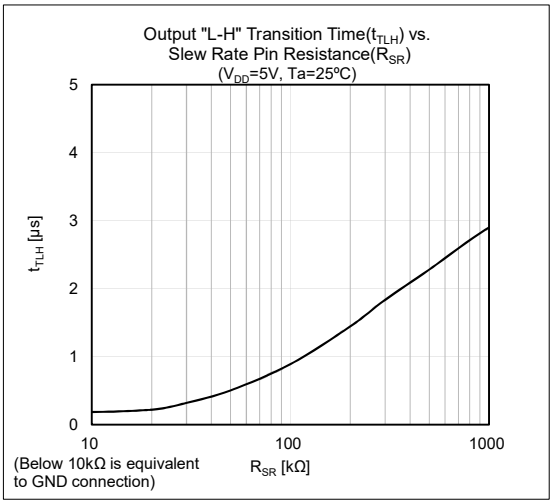
When the V_{DD} voltage exceeds V_{RPOR} (typ.), it operates normally, but the V_{DD} voltage should be used within the recommended operating voltage range (V_{DD}=3.0V to 5.5V)



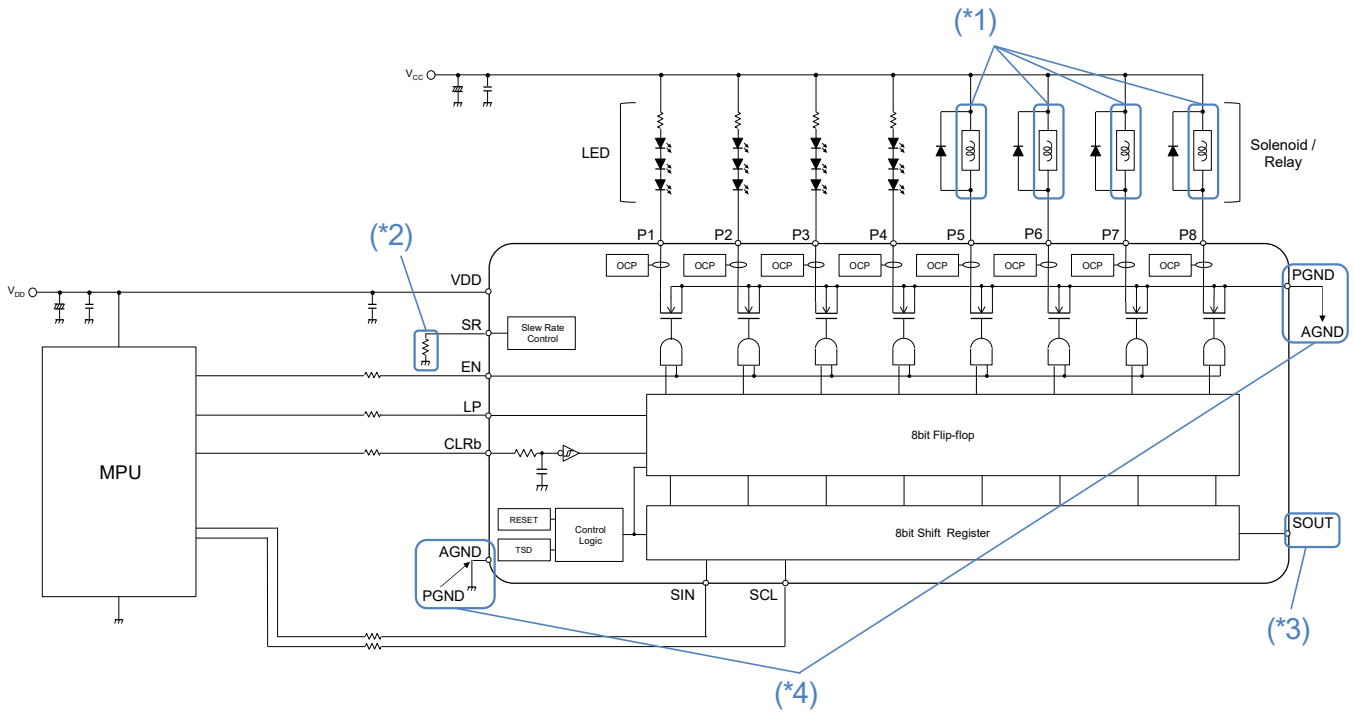
●Output Slew Rate Setting Function (SR Pin)

The SR function can set the rise time and fall time of the gate voltage of the output FETs by connecting a pull-down resistor to the SR pin.
The pull-down resistance can be set from 0 Ω (connected to AGND) to 1M Ω. It should not be open.
When this function is not used, connect the SR pin to AGND.





■TYPICAL APPLICATION 1



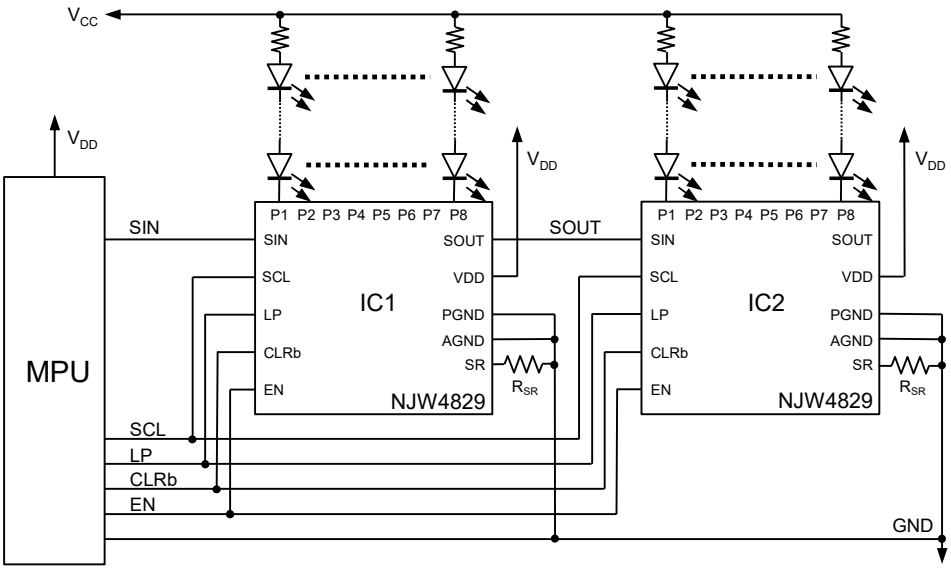
(*1): The output pins don't have clamp circuits.
Therefore, when driving inductive loads such as solenoids and relays, connect a diode to the outside and secure path of recirculation current at turn-off.

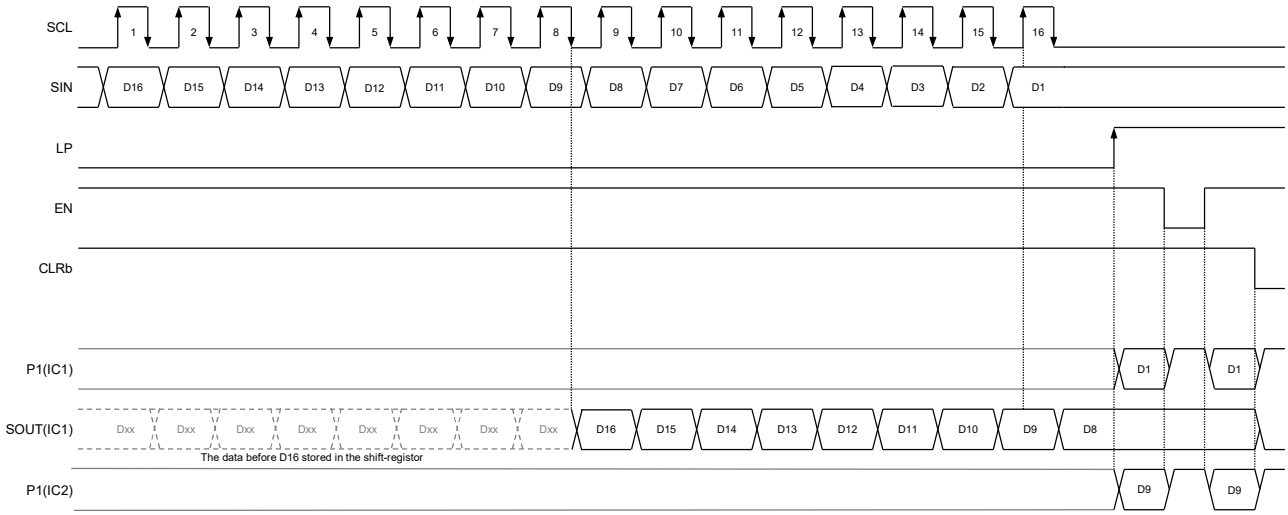
(*2): When SR function is not used, connect the SR pin to AGND and it should not be open.

(*3): When SOUT pin is not used, make it open, or connect with high resistance to AGND or VDD.

(*4): It should be wired the board so that there is no potential difference between AGND and PGND.

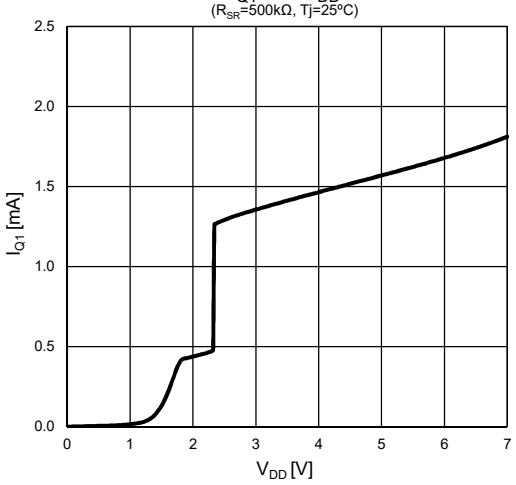
■TYPICAL APPLICATION 2 (Cascade Connection)



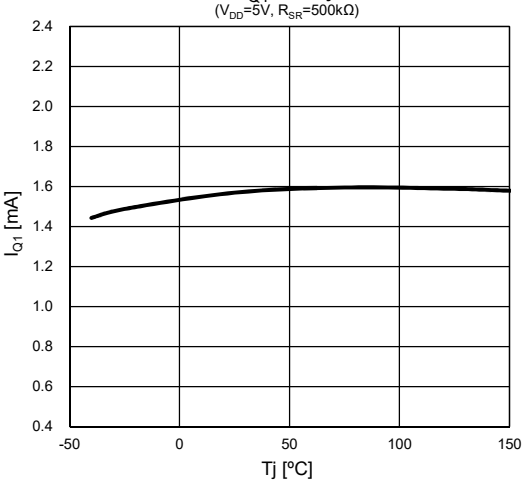


■TYPICAL CHARACTERISTICS

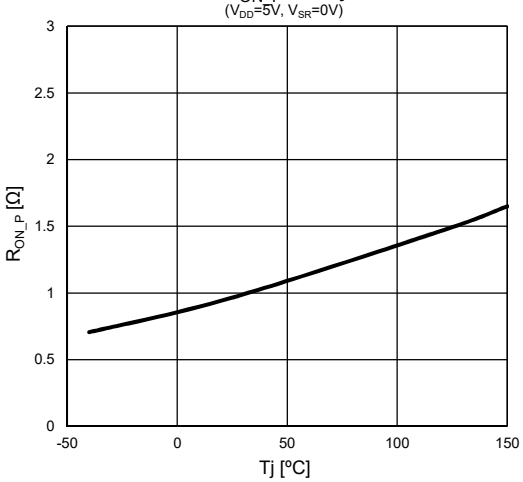
I_{Q1} vs. V_{DD}
(R_{SR}=500kΩ, Tj=25°C)



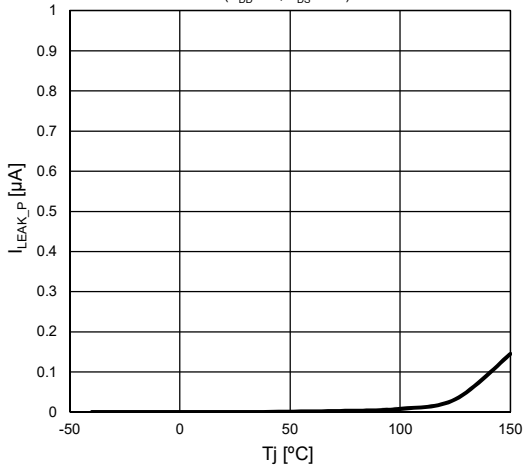
I_{Q1} vs. Tj
(V_{DD}=5V, R_{SR}=500kΩ)



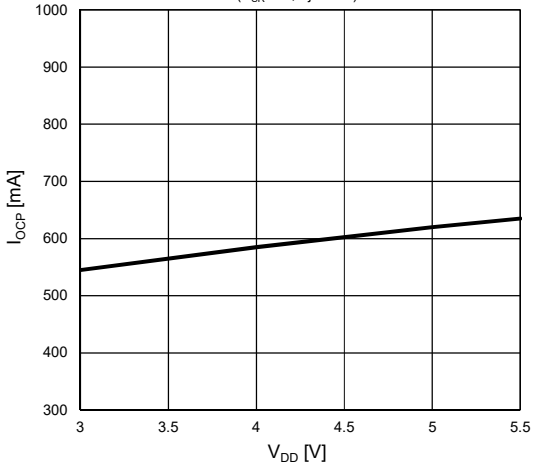
R_{ON_P} vs. Tj
(V_{DD}=5V, V_{SR}=0V)



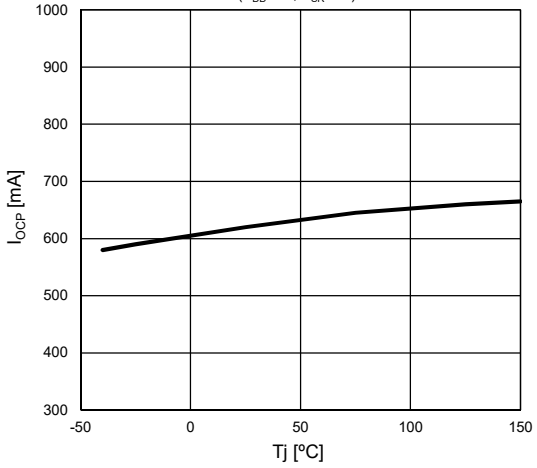
I_{LEAK_P} vs. Tj
(V_{DD}=5V, V_{DS}=40V)



I_{OCP} vs. V_{DD}
(V_{SR}=0V, Tj=25°C)



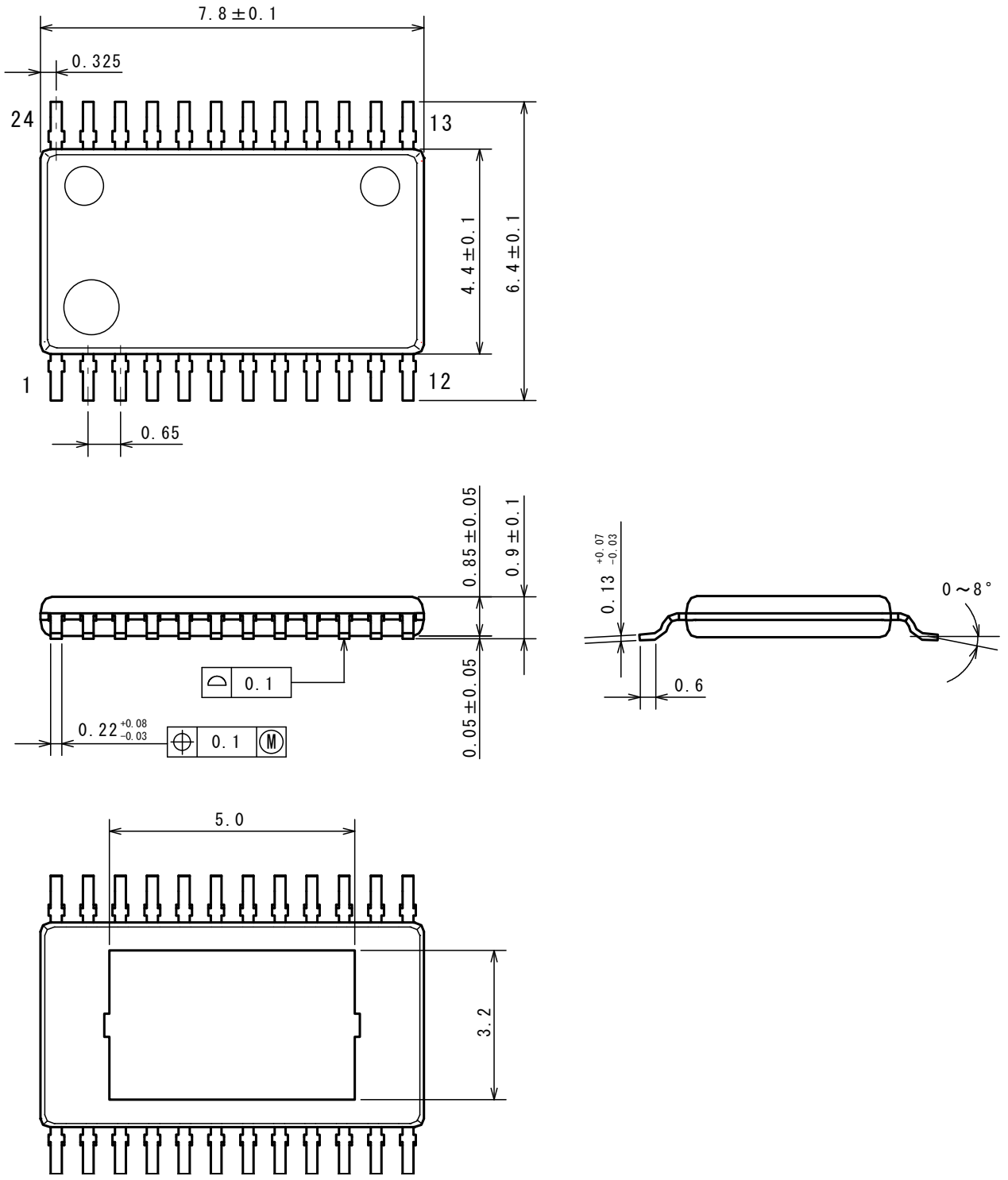
I_{OCP} vs. Tj
(V_{DD}=5V, V_{SR}=0V)



HTSSOP24-P1

Unit: mm

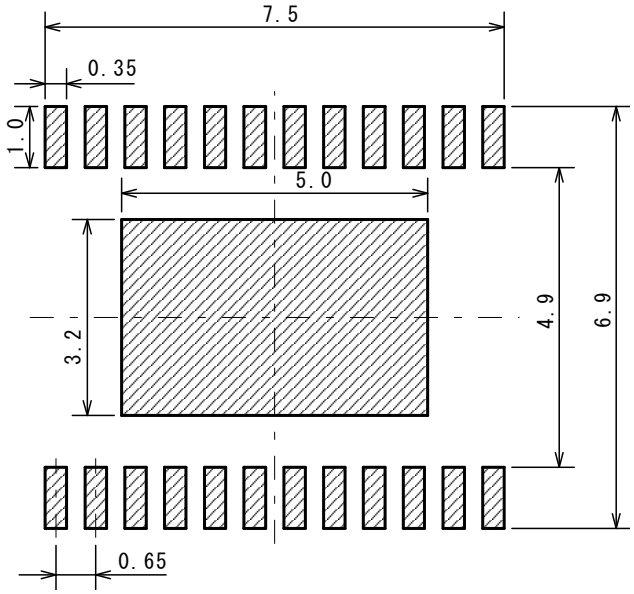
■PACKAGE DIMENSIONS



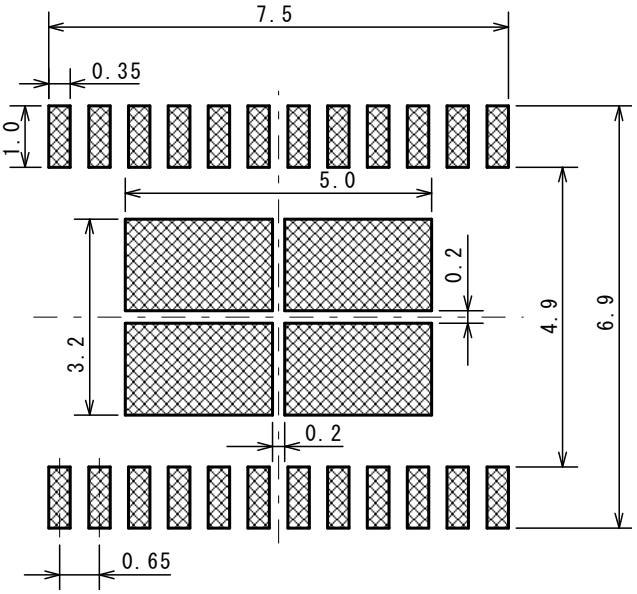
HTSSOP24-P1

Unit: mm

■EXAMPLE OF SOLDER PADS DIMENSIONS



<Solder pattern>



<Metal mask>

＜Instructions for mounting＞

Please note the following points when you mount HTSSOP24-P1 package IC because there is a backside electrode.

(1) Temperature profile of lead and backside electrode.

It is necessary that both re-flow temperature profile of lead and backside electrode are higher than preset temperature.

When solder wet temperature is lower than lead/backside electrode temperature, there is possibility of defect mounting.

(2) Design of foot pattern / metal mask

Metal mask thickness of solder pattern print is more than 0.13mm.

(3) Solder paste

The mounting was evaluated with following solder paste, foot pattern and metal mask. Because mounting might be greatly different according to the manufacturer and the product number even if the solder composition is the same. We will strongly recommend to evaluate mounting previously with using foot pattern, metal mask and solder paste.

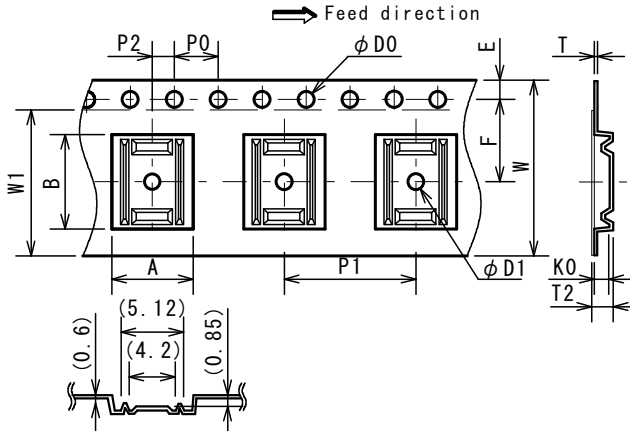
Solder paste composition	Sn3Ag0.5Cu (Senju Metal Industry Co., Ltd：M705-GRN350-32-11)

HTSSOP24-P1

■PACKING SPEC

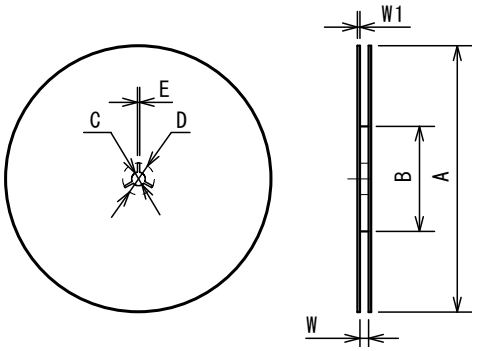
Unit: mm

TAPING DIMENSIONS



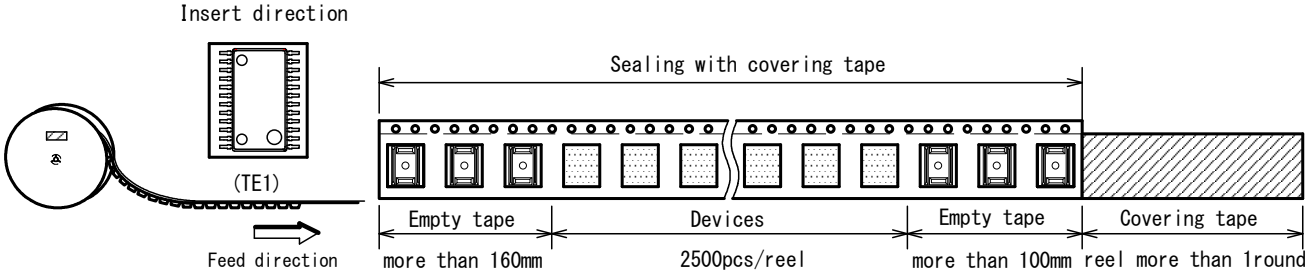
SYMBOL	DIMENSION	REMARKS
A	7.45±0.2	
B	8.60±0.1	
D0	$1.5^{+0.1}_{0}$	
D1	$1.5^{+0.1}_{0}$	
E	1.75±0.1	
F	7.5±0.1	
P0	4.0±0.1	
P1	12.0±0.1	
P2	2.0±0.1	
T	0.3±0.05	
T2	1.85	
K0	1.45±0.3	
W	16.0±0.3	
W1	13.3	THICKNESS 0.1max

REEL DIMENSIONS

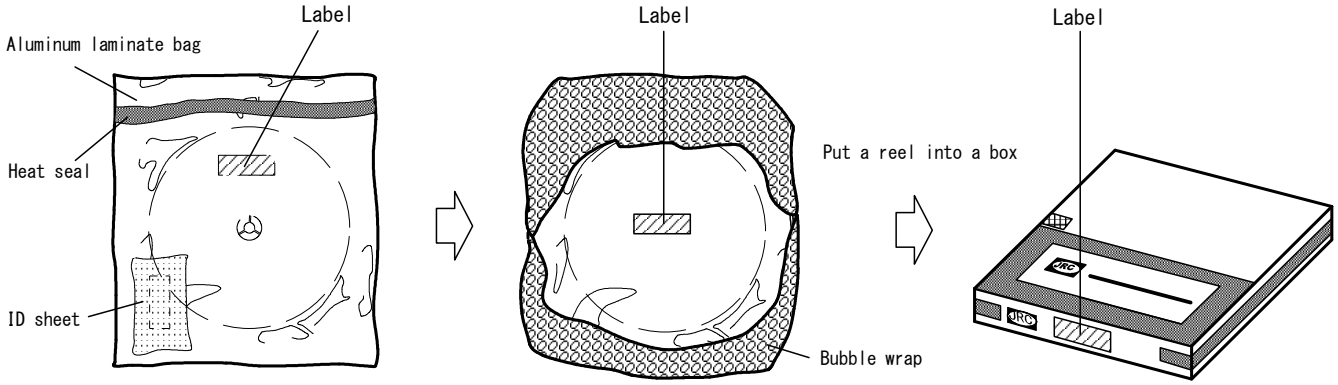


SYMBOL	DIMENSION
A	φ330±2
B	φ100±1
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	17.4±1
W1	2

TAPING STATE



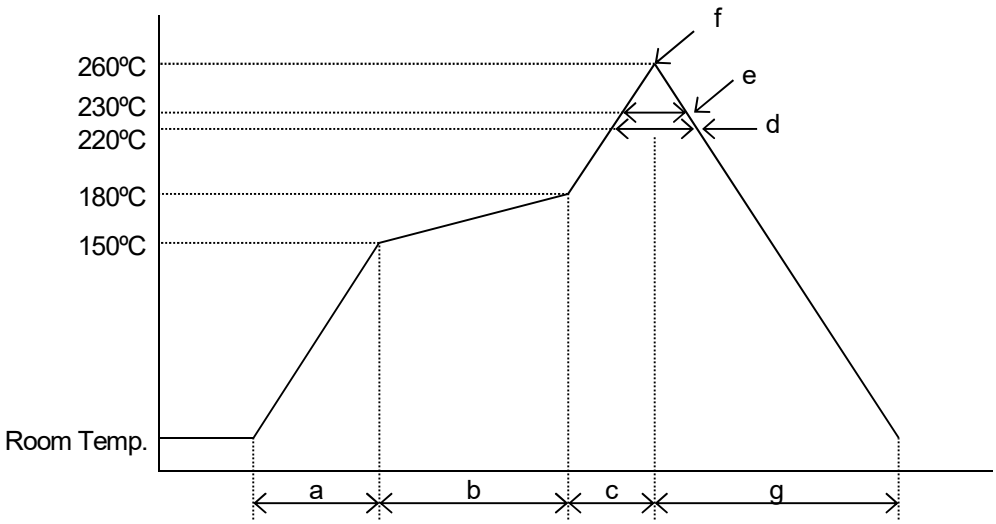
PACKING STATE



■RECOMMENDED MOUNTING METHOD

INFRARED REFLOW SOLDERING METHOD

*Recommended reflow soldering procedure



a: Temperature ramping rate : 1 to 4ºC/s
b: Pre-heating temperature : 150 to 180ºC
Pre-heating time : 60 to 120s
c: Temperature ramp rate : 1 to 4ºC /s
d: 220ºC or higher time : Shorter than 60s
e: 230ºC or higher time : Shorter than 40s
f: Peak temperature : Lower than 260ºC
g: Temperature ramping rate : 1 to 6ºC /s

The temperature indicates at the surface of mold package.

■REVISION HISTORY

Date	Revision	Changes
21.Jun.2018	Ver.1.0	New Release

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   Various Safety devices

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