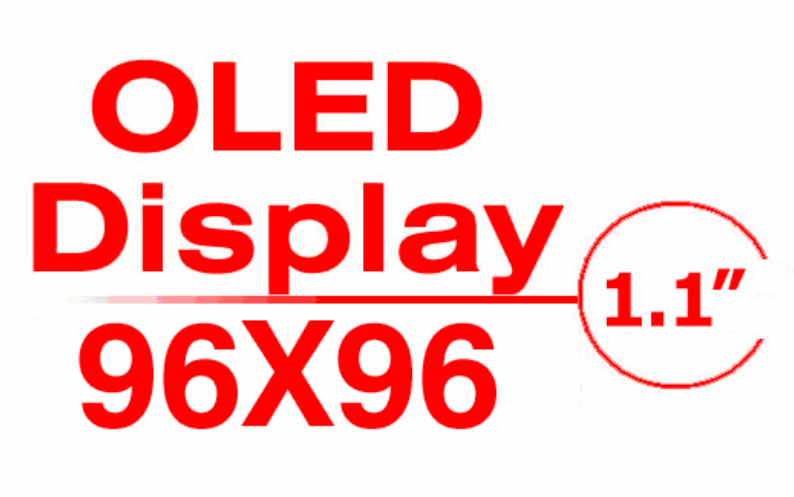
SPECIFICATION

PART NO. : OEL9M1007-Y-E



This specification maybe changed without any notice in order to improve performance or quality etc.
Please contact TRULY Semiconductors LTD. OLED R&D department for update specification and product status before design for this product or release the order.

PRODUCT CONTENTS

TRULY®信利		Customer	
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REVISION HISTORY

Rev.	Contents	Date
1.0	Initial release.	2013-08-02

n PHYSICAL DATA

No.	Items:	Specification:	Unit
1	Diagonal Size	1.1	Inch
2	Resolution	96 (H) x 96(V)	Dots
3	Active Area	19.655 (W) x 19.655(H)	mm^2
4	Outline Dimension (Panel)	25.49 (W) x 29.10(H)	mm^2
5	Pixel Pitch	0.205 (W) x 0.205 (H)	mm^2
6	Pixel Size	0.18 W) x 0.18 (H)	mm^2
7	Driver IC	SH1107G	-
8	Display Color	Yellow	-
9	Gray scale	1	Bit
10	Interface	Parallel / SPI / I^2C	-
11	IC package type	COG	-
12	Thickness	1.45±0.1	mm
13	Weight	TBD	g
14	Duty	1/96	-

n ABSOLUTE MAXIMUM RATINGS

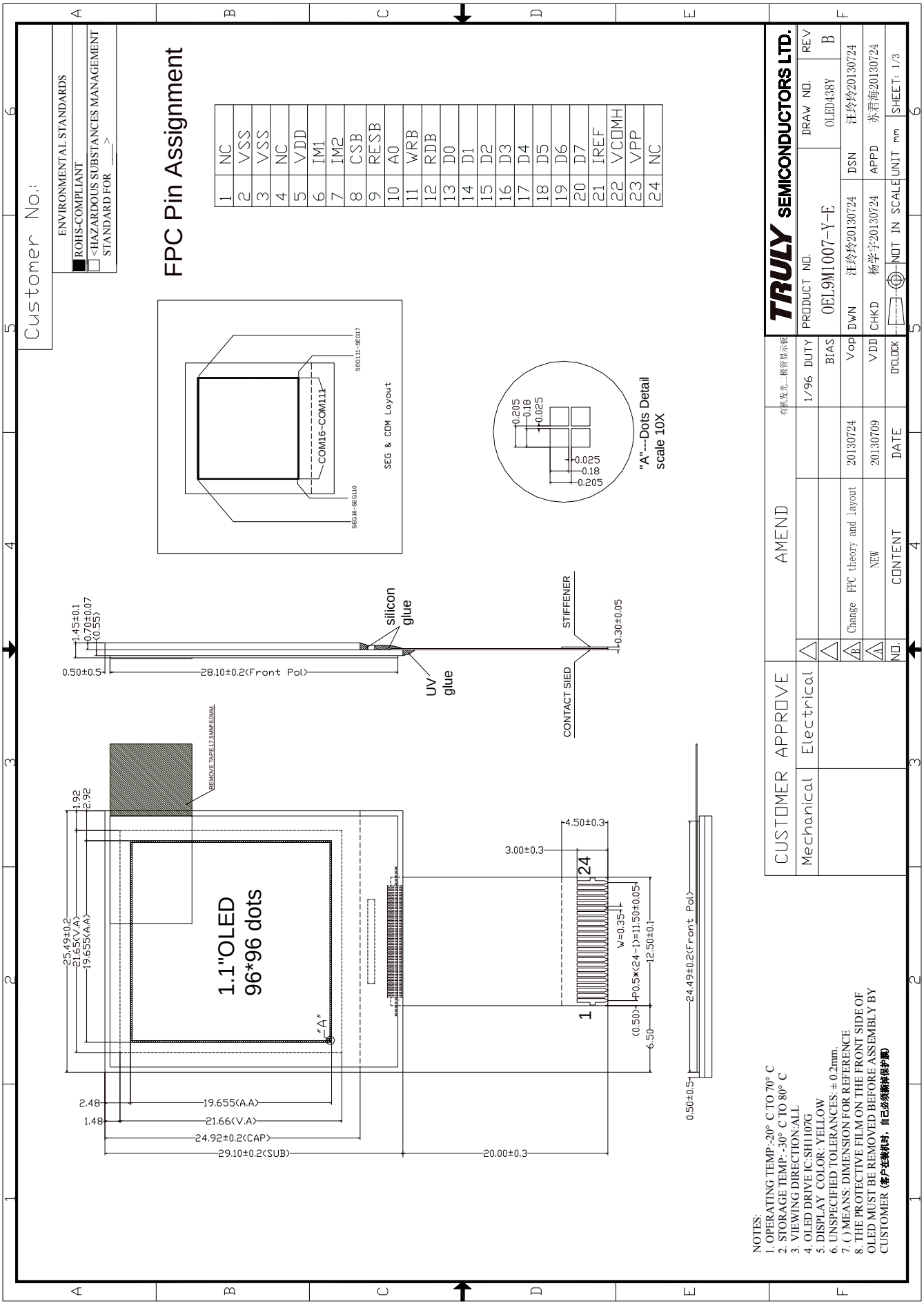
Unless otherwise specified, V_{SS} = 0V (Ta = 25℃)

Items		Symbol	Min	Typ.	Max	Unit
Supply Voltage	Logic	V_{DD}	-0.3	-	3.6	V
	Driving	V_{PP}	-0.3	-	17.0	V
Operating Temperature		Top	-20	-	70	℃
Storage Temperature		Tst	-30	-	80	℃
Humidity		-	-	-	90	%RH

NOTE:

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

n EXTERNAL DIMENSIONS



n ELECTRICAL CHARACTERISTICS

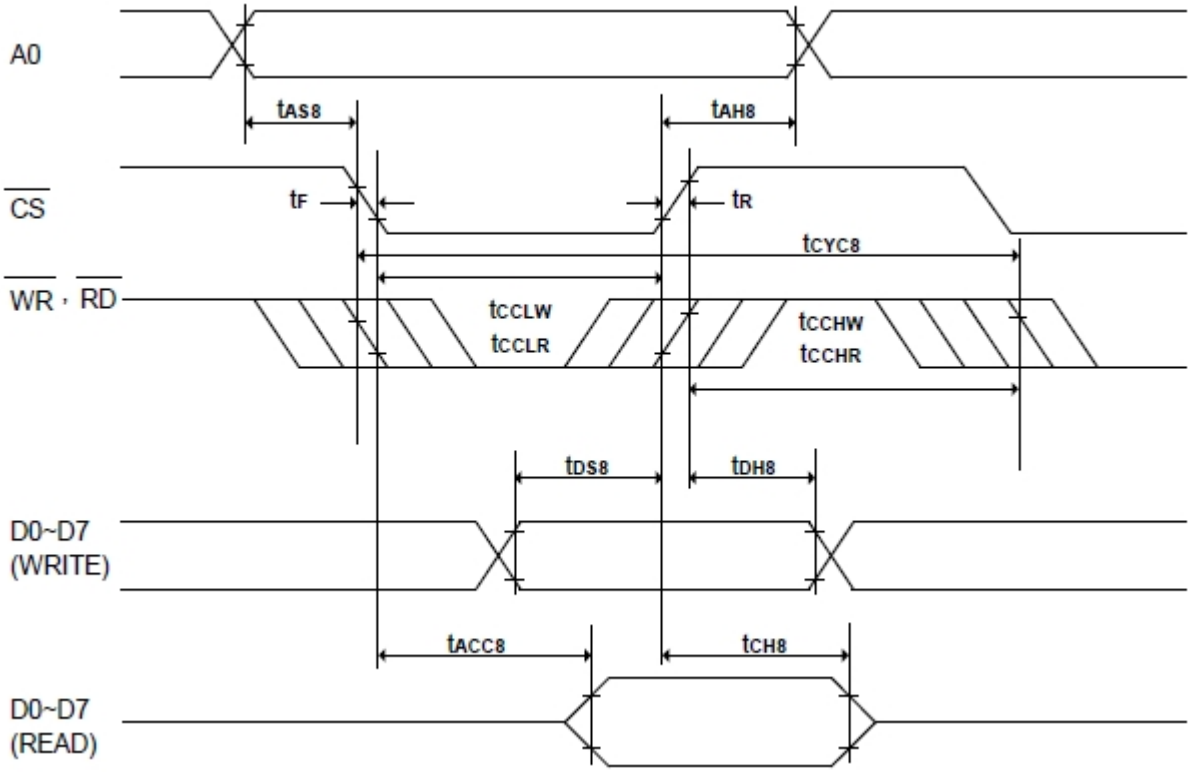
◆DC Characteristics

Unless otherwise specified, V_{SS} = 0V , V_{DD}=1.65V to 3.5V ， AVDD=2.4 to 3.5V (Ta = +25℃)

Items		Symbol	Min	Typ.	Max	Unit
Supply Voltage	Logic	V_{DD}	1.65	-	3.5	V
	Operating	V_{PP}	7.0	-	16.5	V
Input Voltage	High Voltage	V_{IH}	0.8 x V_{DD}	-	V_{DD}	V
	Low Voltage	V_{IL}	V_{SS}	-	0.2 x V_{DD}	V
Output Voltage	High Voltage	V_{OH}	0.8 x V_{DD}	-	V_{DD}	V
	Low Voltage	V_{OL}	V_{SS}	-	0.2 x V_{DD}	V

◆AC Characteristics

(1) System buses Read/Write characteristics 1 (For the 8080 Series Interface MPU)



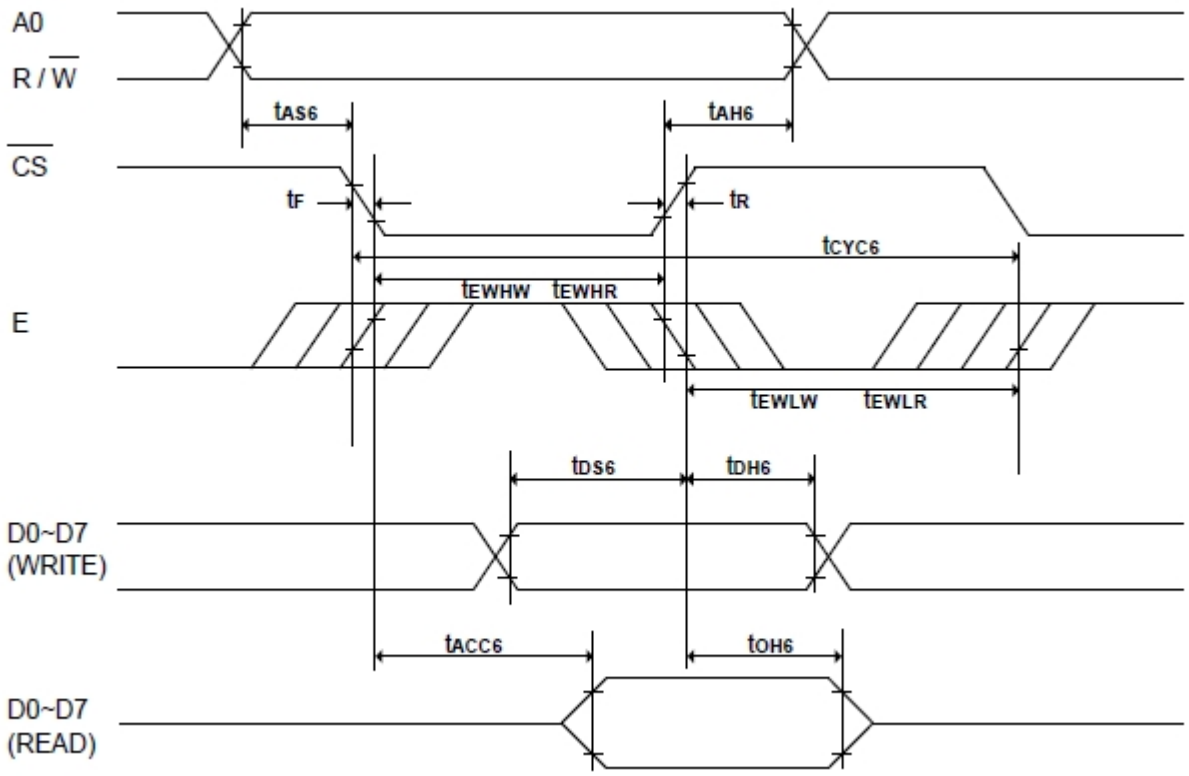
(VDD = 1.65V – 2.4V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tCYC8	System cycle time	300	-	-	ns	
tAS8	Address setup time	0	-	-	ns	
tAH8	Address hold time	0	-	-	ns	
tDS8	Data setup time	40	-	-	ns	
tDH8	Data hold time	30	-	-	ns	
tCH8	Output disable time	10	-	70	ns	CL = 100pF
tACC8	$\overline{RD}$ access time	-	-	280	ns	CL = 100pF
tCCLW	Control L pulse width (WR)	100	-	-	ns	
tCCLR	Control L pulse width (RD)	120	-	-	ns	
tCCHW	Control H pulse width (WR)	100	-	-	ns	
tCCHR	Control H pulse width (RD)	100	-	-	ns	
tR	Rise time	-	-	15	ns	
tF	Fall time	-	-	15	ns	

(V_{DD} = 2.4V – 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC8}	System cycle time	300	-	-	ns	
t_{AS8}	Address setup time	0	-	-	ns	
t_{AH8}	Address hold time	0	-	-	ns	
t_{DS8}	Data setup time	40	-	-	ns	
t_{DH8}	Data hold time	15	-	-	ns	
t_{CH8}	Output disable time	10	-	70	ns	C_L = 100pF
t_{ACC8}	$\overline{RD}$ access time	-	-	140	ns	C_L = 100pF
t_{CCLW}	Control L pulse width (WR)	100	-	-	ns	
t_{CCLR}	Control L pulse width (RD)	120	-	-	ns	
t_{CCHW}	Control H pulse width (WR)	100	-	-	ns	
t_{CCHR}	Control H pulse width (RD)	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

(2) System buses Read/Write Characteristics 2 (For the 6800 Series Interface MPU)



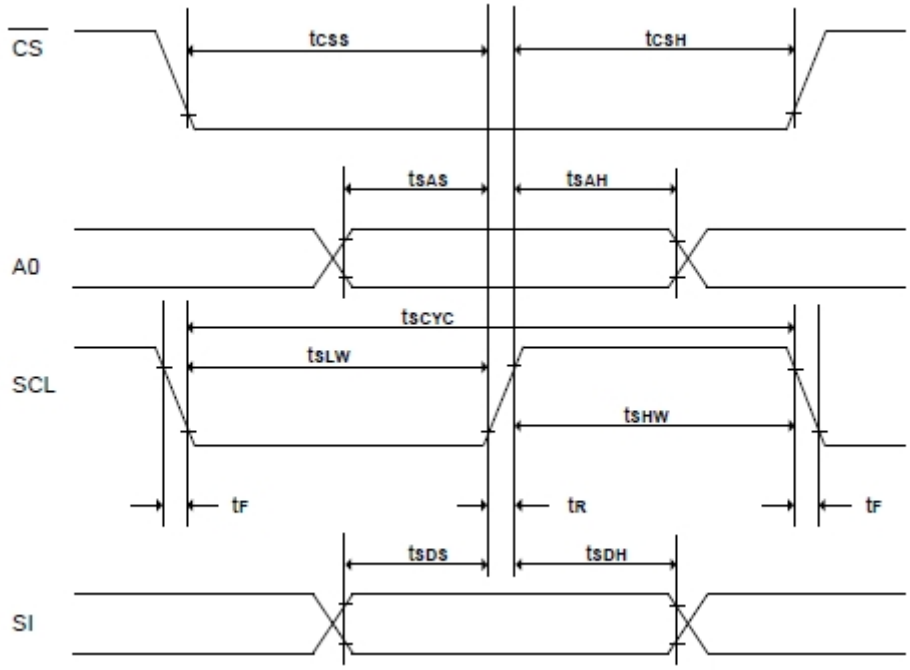
(V_{DD} = 1.65 – 2.4V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC6}	System cycle time	300	-	-	ns	
t_{AS6}	Address setup time	0	-	-	ns	
t_{AH6}	Address hold time	0	-	-	ns	
t_{DS6}	Data setup time	40	-	-	ns	
t_{DH6}	Data hold time	30	-	-	ns	
t_{OH6}	Output disable time	10	-	70	ns	C_L = 100pF
t_{ACC6}	Access time	-	-	280	ns	C_L = 100pF
t_{EWHW}	Enable H pulse width (Write)	100	-	-	ns	
t_{EWHR}	Enable H pulse width (Read)	120	-	-	ns	
t_{EWLW}	Enable L pulse width (Write)	100	-	-	ns	
t_{EWLR}	Enable L pulse width (Read)	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

(V_{DD} = 2.4 – 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC6}	System cycle time	300	-	-	ns	
t_{AS6}	Address setup time	0	-	-	ns	
t_{AH6}	Address hold time	0	-	-	ns	
t_{DS6}	Data setup time	40	-	-	ns	
t_{DH6}	Data hold time	15	-	-	ns	
t_{OH6}	Output disable time	10	-	70	ns	C_L = 100pF
t_{ACC6}	Access time	-	-	140	ns	C_L = 100pF
t_{EWHW}	Enable H pulse width (Write)	100	-	-	ns	
t_{EWHR}	Enable H pulse width (Read)	120	-	-	ns	
t_{EWLW}	Enable L pulse width (Write)	100	-	-	ns	
t_{EWLR}	Enable L pulse width (Read)	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

(3) System buses Write characteristics 3 (For 4 wires SPI)



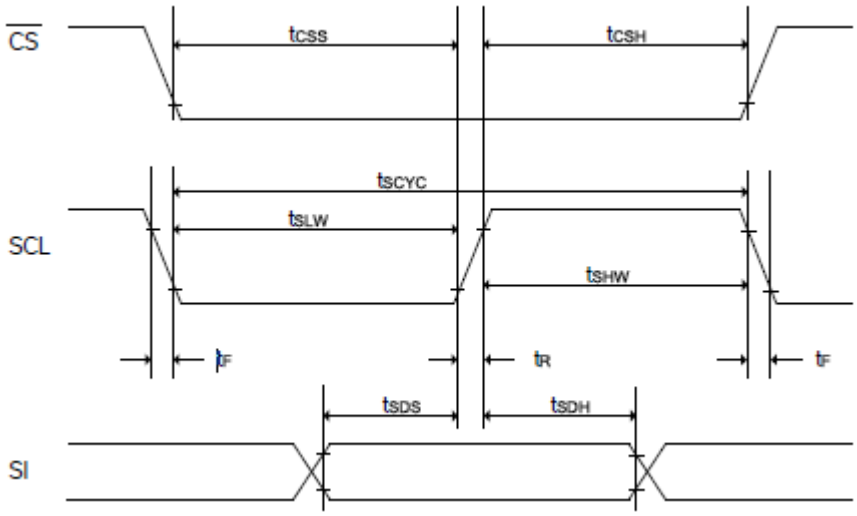
(VDD1 = 1.65 – 2.4V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	500	-	-	ns	
tSAS	Address setup time	300	-	-	ns	
tSAH	Address hold time	300	-	-	ns	
tSDS	Data setup time	200	-	-	ns	
tSDH	Data hold time	200	-	-	ns	
tCSS	$\overline{CS}$ setup time	240	-	-	ns	
tCSH	$\overline{CS}$ hold time time	120	-	-	ns	
tSHW	Serial clock H pulse width	200	-	-	ns	
tSLW	Serial clock L pulse width	200	-	-	ns	
tR	Rise time	-	-	30	ns	
tF	Fall time	-	-	30	ns	

(VDD1 = 2.4 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	250	-	-	ns	
tSAS	Address setup time	150	-	-	ns	
tSAH	Address hold time	150	-	-	ns	
tSDS	Data setup time	100	-	-	ns	
tSDH	Data hold time	100	-	-	ns	
tCSS	$\overline{CS}$ setup time	120	-	-	ns	
tCSH	$\overline{CS}$ hold time time	60	-	-	ns	
tSHW	Serial clock H pulse width	100	-	-	ns	
tSLW	Serial clock L pulse width	100	-	-	ns	
tR	Rise time	-	-	15	ns	
tF	Fall time	-	-	15	ns	

(4) System buses Write characteristics 4(For 3 wires SPI)



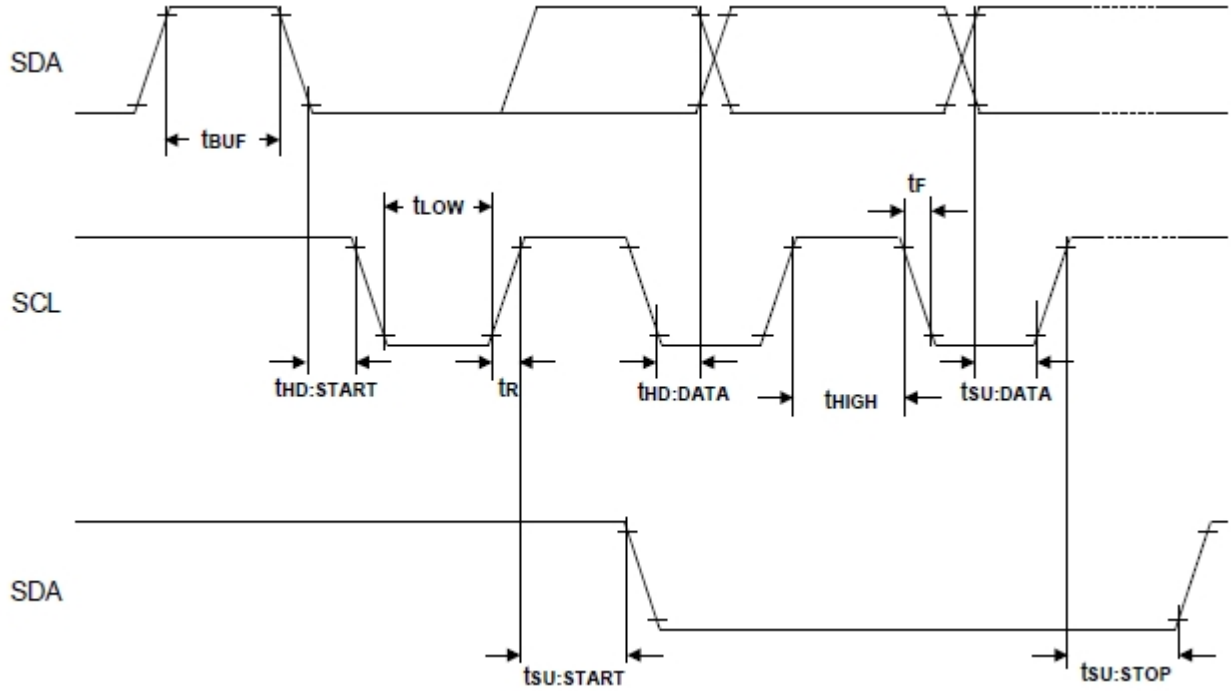
(V_{DD1} = 1.65 – 2.4V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	500	-	-	ns	
tSDS	Data setup time	200	-	-	ns	
tSDH	Data hold time	200	-	-	ns	
tCSS	$\overline{CS}$ setup time	240	-	-	ns	
tCSH	$\overline{CS}$ hold time time	120	-	-	ns	
tSHW	Serial clock H pulse width	200	-	-	ns	
tSLW	Serial clock L pulse width	200	-	-	ns	
tR	Rise time	-	-	30	ns	
tF	Fall time	-	-	30	ns	

(V_{DD1} = 2.4 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	250	-	-	ns	
tSDS	Data setup time	100	-	-	ns	
tSDH	Data hold time	100	-	-	ns	
tCSS	$\overline{CS}$ setup time	120	-	-	ns	
tCSH	$\overline{CS}$ hold time time	60	-	-	ns	
tSHW	Serial clock H pulse width	100	-	-	ns	
tSLW	Serial clock L pulse width	100	-	-	ns	
tR	Rise time	-	-	15	ns	
tF	Fall time	-	-	15	ns	

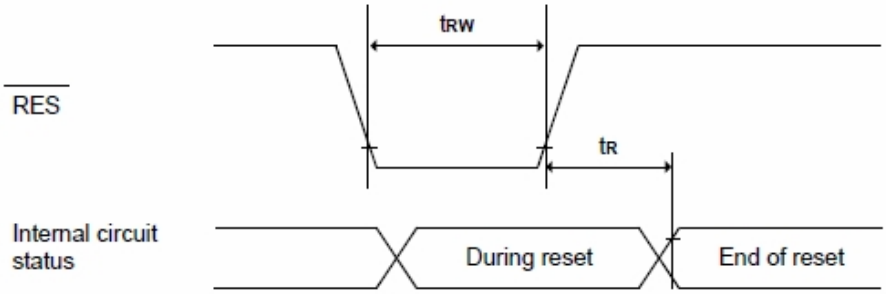
(5) I²C interface characteristics



(VDD = 1.65 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
fSCL	SCL clock frequency	DC	-	400	kHz	
TLOW	SCL clock Low pulse width	1.3	-	-	μs	
THIGH	SCL clock H pulse width	0.6	-	-	μs	
TSU:DATA	data setup time	100	-	-	ns	
THD:DATA	data hold time	0	-	0.9	μs	
TR	SCL，SDA rise time	20+0.1Cb	-	300	ns	
TF	SCL，SDA fall time	20+0.1Cb	-	300	ns	
Cb	Capacity load on each bus line	-	-	400	pF	
TSU:START	Setup timefor re-START	0.6	-	-	μs	
THD:START	START Hold time	0.6	-	-	μs	
TSU:STOP	Setup time for STOP	0.6	-	-	μs	
TBUF	Bus free times between STOP and START condition	1.3	-	-	μs	

(6) Reset Timing



(VDD = 1.65 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tR	Reset time	-	-	2.0	μs	
tRW	Reset low pulse width	10.0	-	-	μs	

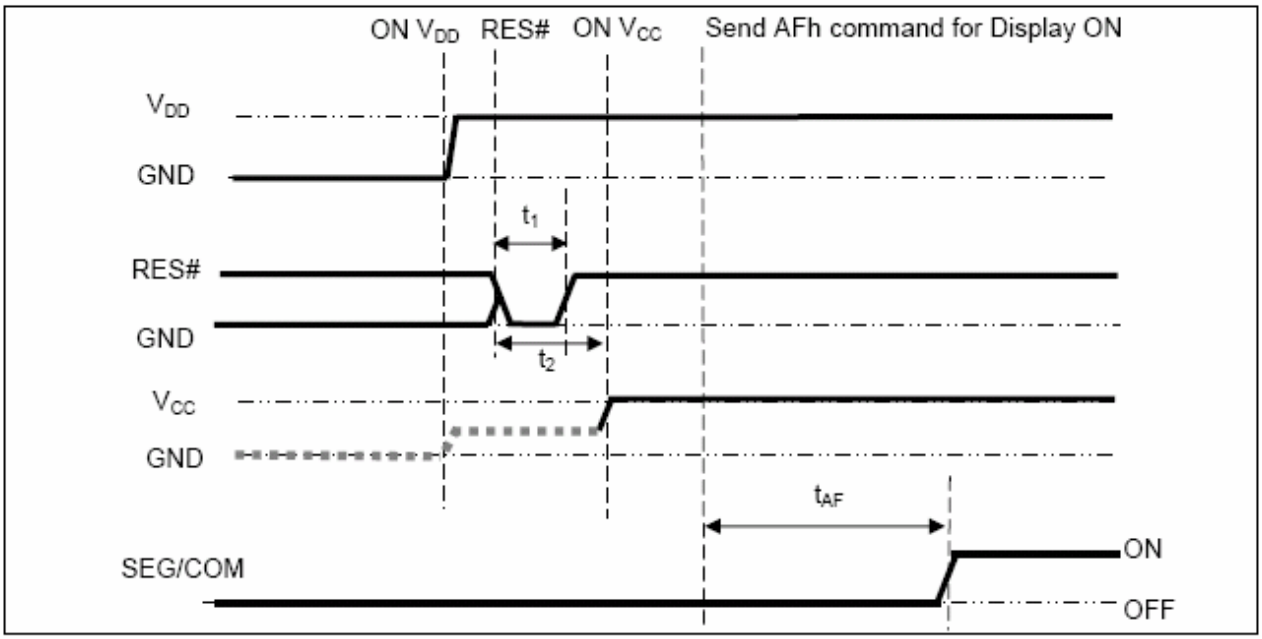
n TIMING OF POWER SUPPLY

The following figures illustrate the recommended power ON and power OFF sequence of SSD1325.

Power ON sequence:

1. Power ON V_{DD}.
2. After V_{DD} become stable, set RES# pin LOW (logic LOW) for at least 3us (t_1) and then HIGH (logic HIGH).
3. After set RES# pin LOW (logic LOW), wait for at least 3us (t_2). Then Power ON V_{CC}.(1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).

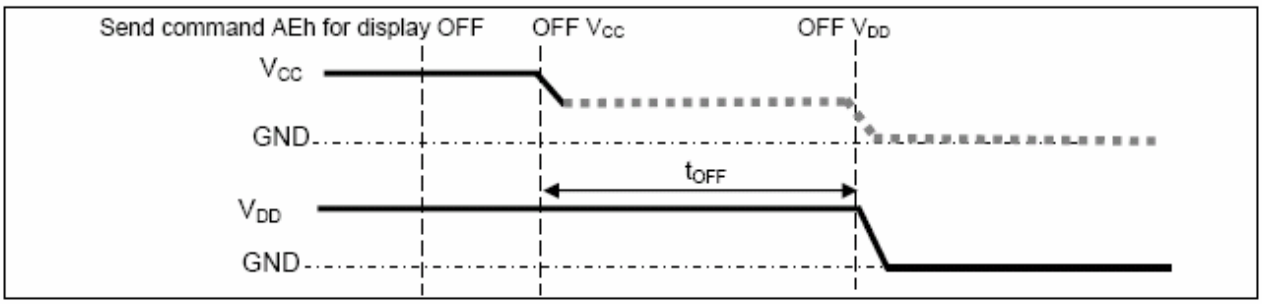
Figure 16 : The Power ON sequence



Power OFF sequence:

1. Send command AEh for display OFF.
2. Wait until panel discharges completely.
3. Power OFF V_{CC}.(1), (2)
4. Wait for t_{OFF}. Power OFF V_{DD}. (where Minimum t_{OFF}=0ms, Typical t_{OFF}=100ms)

Figure 17 : The Power OFF sequence



Note:

(1) Since an ESD protection circuit is connected between V_{DD} and V_{CC}, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 16 and Figure 17.

(2) V_{CC} should be kept float when it is OFF.

n ELECTRO-OPTICAL CHARACTERISTICS (Ta=25℃)

Items		Symbol	Min.	Typ.	Max.	Unit	Remark
Operating Luminance		L	100	120	-	cd /m^2	Yellow
Power Consumption		P	-	110	160	mW	30% pixels ON L=120cd/m^2
Frame Frequency		Fr	-	100	-	Hz	
Color Coordinate	Yellow	CIE x	0.415	0.455	0.495	CIE1931	Darkroom
		CIE y	0.485	0.525	0.565		
Response Time	Rise	Tr	-	-	0.02	ms	-
	Decay	Td	-	-	0.02	ms	-
Contrast Ratio*		Cr	10000:1	-	-		Darkroom
Viewing Angle		△ θ	160	-	-	Degree	-
Operating Life Time*		Top	20,000	-	-	Hours	L=120cd/m^2

Note:

1. 120cd/m^2 is base on V_{DD}=3.0V, V_{PP}=13.0V, contrast command setting 0xFA;

2. Contrast Ratio is defined as follows:

$$\text{Contrast ratio} = \frac{\text{Photo – detector output with OLED being “white”}}{\text{Photo – detector output with OLED being “black”}}$$

3. **Life Time** is defined when the Luminance has decayed to less than 50% of the initial Luminance specification. (Odd and even chess board alternately displayed), (The initial value should be closed to the typical value after adjusting.).

n INTERFACE PIN CONNECTIONS

No	Symbol	Description
1	NC	No connection
2	V_{SS}	Ground
3	V_{SS}	Ground
4	NC	No connection
5	V_{DD}	1.65 - 3.5V Power supply for logic and input.
6	IM1	MPU interface mode select pads.
7	IM2	MPU interface mode select pads.
8	CSB	This pad is the chip select input. When CSB = "L", then the chip select becomes active, and data/command I/O is enabled.
9	RESB	This is a reset signal input pad. When RESB is set to "L", the settings are initialized. The reset operation is performed by the RES signal level.
10	A0	This is the Data/Command control pad that determines whether the data bits are data or a command. A0 = "H": the inputs at D0 to D7 are treated as display data. A0 = "L": the inputs at D0 to D7 are transferred to the command registers. In I2C interface, this pad serves as SA0 to distinguish the different address of OLED driver.
11	WRB	This is a MPU interface input pad. When connected to an 8080 MPU, this is active LOW. This pad connects to the 8080 MPU WR signal. The signals on the data bus are latched at the rising edge of the WR signal. When connected to a 6800 Series MPU: This is the read/write control signal input terminal. When R/W = "H": Read. When R/W = "L": Write.
12	RDB	This is a MPU interface input pad. When connected to an 8080 series MPU, it is active LOW. This pad is connected to the RDB signal of the 8080 series MPU, and the data bus is in an output status when this signal is "L". When connected to a 6800 series MPU, this is active HIGH. This is used as an enable clock input of the 6800 series MPU.

13~20	D0~D7	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SI). At this time, D2 to D7 are set to high impedance. When the I2C interface is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SDA). At this time, D2 to D7 are set to high impedance.
21	IREF	This is a segment current reference pad. A resistor should be connected between this pad and VSS. Set the current at 15.625mA.
22	V_{COMH}	This is a pad for the voltage output high level for common signals. A capacitor should be connected between this pad and VSS.
23	V_{PP}	This is the most positive voltage supply pad of the chip. It should be supplied externally.
24	NC	No connection

These are the MPU interface mode select pads.

	8080	I^2C	6800	4-wire SPI
IM0	0	0	0	0
IM1	1	1	0	0
IM2	1	0	1	0

Note: 0 is connected to VSS
1 is connected to VDD

n COMMAND TABLE

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
1. Set Column Address 4 lower bits	0	1	0	0	0	0	0	Lower column address				Sets 4 lower bits of column address of display RAM in register. (POR = 00H)
2.Set Column Address 4 higher bits	0	1	0	0	0	0	1	0	Higher column address			Sets 4 higher bits of column address of display RAM in register. (POR = 10H)
3.Set memory addressing mode	0	1	0	0	0	1	0	0	0	0	D	D = 1, Vertical Addressing Mode D = 0, Page Addressing Mode (POR=20H)
4. The Contrast Control Mode Set	0	1	0	1	0	0	0	0	0	0	1	This command is to set Contrast Setting of the display. The chip has 256 contrast steps from 00 to FF. (POR = 80H)
Contrast Data Register Set	0	1	0	Contrast Data								
5. Set Segment Re-map (ADC)	0	1	0	1	0	1	0	0	0	0	ADC	The down (0) or up (1) rotation. (POR = A0H)
6. Set Entire Display OFF/ON	0	1	0	1	0	1	0	0	1	0	D	Selects normal display (0) or Entire Display ON (1). (POR = A4H)
7. Set Normal/ Reverse Display	0	1	0	1	0	1	0	0	1	1	D	Normal indication (0) when low, but reverse indication (1) when high. (POR = A6H)
8. DC-DC Control Mode Set	0	1	0	1	0	1	0	1	1	0	1	This command is to control the DC-DC voltage DC-DC will be turned on when display on converter (1) or DC-DC OFF (0). (POR = 81H)
DC-DC Setting Mode Set	0	1	0	1	0	0	0	F2	F1	F0	D	

Command Table (Continued)

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
9. Display OFF/ON	0	1	0	1	0	1	0	1	1	1	D	Turns on OLED panel (1) or turns off (0). (POR = AEH)
10. Set Page Address	0	1	0	1	0	1	1	Page Address				Specifies page address to load display RAM data to page address register. (POR = B0H)
11 Set Common Output Scan Direction	0	1	0	1	1	0	0	D	*	*	*	Scan from COM0 to COM [N - 1] (0) or Scan from COM [N -1] to COM0 (1). (POR = C0H)
12. Set Display Divide Ratio/Oscillator Frequency Mode Set	0	1	0	1	1	0	1	0	1	0	1	This command is used to set the frequency of the internal display clocks. (POR = 50H)
Divide Ratio/Oscillator Frequency Data Set	0	1	0	Oscillator Frequency				Divide Ratio				
13. Dis-charge / Pre-charge Period Mode Set	0	1	0	1	1	0	1	1	0	0	1	This command is used to set the duration of the dis-charge and pre-charge period. (POR = 22H)
Dis-charge /Pre-charge Period Data Set	0	1	0	Dis-charge Period				Pre-charge Period				
14. VCOM Deselect Level Mode Set	0	1	0	1	1	0	1	1	0	1	1	This command is to set the common pad output voltage level at deselect stage. (POR = 35H)
VCOM Deselect Level Data Set	0	1	0	VCOM = (β_1 X VREF)								
17. Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-Modify-Write start.
18. End	0	1	0	1	1	1	0	1	1	1	0	Read-Modify-Write end.
19. NOP	0	1	0	1	1	1	0	0	0	1	1	Non-Operation Command
20 Write Display Data	1	1	0	Write RAM data								
21 Read ID	0	0	1	BUSY	ON/ OFF	ID						
22. Read Display Data	1	0	1	Read RAM data								

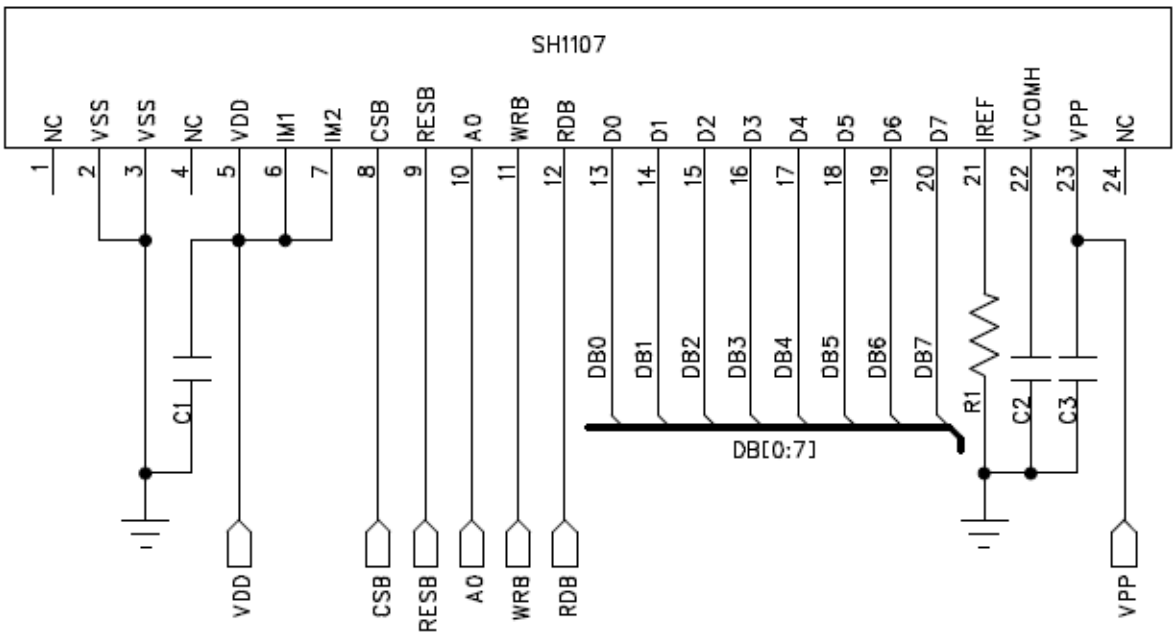
Note: Do not use any other command, or the system malfunction may result.

n INTIALIZATION CODE

```
void Initial_1107()
{
WMLCDCOM(0xAE);//Display OFF

WMLCDCOM(0x0F);//Set Column Address 4 lower bits
WMLCDCOM(0x17);//Set Column Address 4 higher bits

WMLCDCOM(0xA0);//Set Segment Re-map

WMLCDCOM(0xD9);//Set Dis-charge/Pre-charge Period
WMLCDCOM(0x56);

WMLCDCOM(0xD5);//Set Display Clock Divide Ratio/Oscillator Frequency
WMLCDCOM(0x50);

WMLCDCOM(0x20);//Set Page Addressing Mode

WMLCDCOM(0xDB);//Set VCOM
WMLCDCOM(0x35);

WMLCDCOM(0x81);//Set Contrast
WMLCDCOM(CONTRAST);

WMLCDCOM(0xC0);//Set Common Output Scan Direction

WMLCDCOM(0xA4);//Set Entire Display OFF

WMLCDCOM(0xA6);//Set Normal/Reverse Display

WMLCDCOM(0xAD);//Set DC-DC OFF
WMLCDCOM(0x80);
Clear();
WMLCDCOM(0xAF);
}
```

n SCHEMATIC EXAMPLE

◆8080 Parallel Interface Application Circuit:

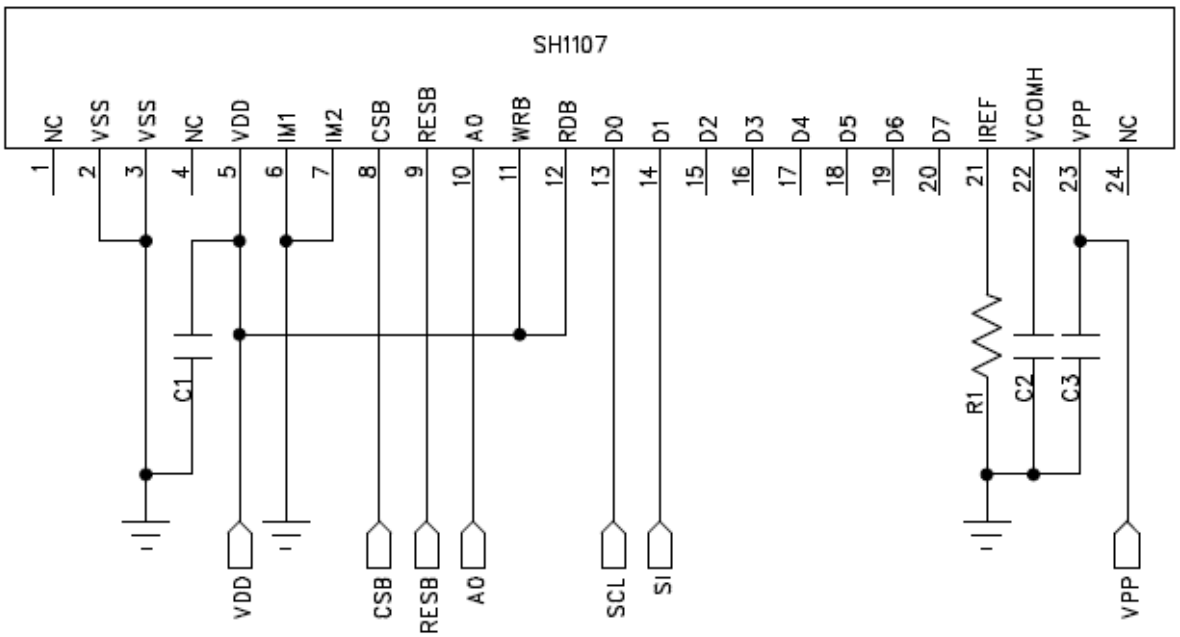


Note:

C1 ~ C3: 4.7μF.

R1: about 750KΩ, R1 = (Voltage at I_{REF} - V_{SS})/I_{REF}

◆4-wire SPI Serial Interface Application Circuit:

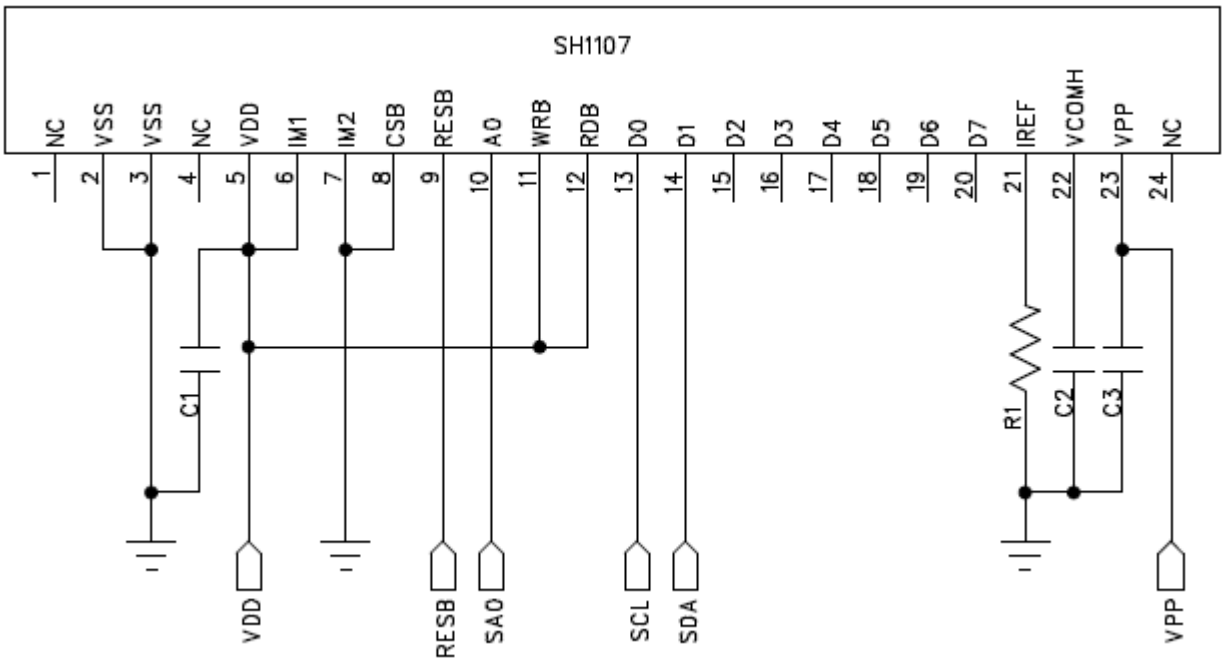


Note:

C1 ~ C3:4.7μF

R1: Recommend 750KΩ

◆I²C Interface Application Circuit:



Note:

C1 ~ C3:4.7μF

R1: Recommend 750KΩ

The least significant bit of the slave address is set by connecting the input SA0 to either logic 0(VSS) or 1(VDD)

The positive supply of pull-up resistor must equal to the value of VDD.

Recommend the value of resistor Rp equal to 1.5 KΩ

n RELIABILITY TESTS

Item		Condition	Criterion
High Temperature Storage (HTS)		80±2℃, 200 hours	1. After testing, the function test is ok. 2. After testing, no addition to the defect. 3. After testing, the change of luminance should be within +/- 50% of initial value. 4. After testing, the change for the mono and area color must be within (+/-0.02, +/- 0.02) and for the full color it must be within (+/-0.04, +/-0.04) of initial value based on 1931 CIE coordinates. 5. After testing, the change of total current consumption should be within +/- 50% of initial value.
High Temperature Operating (HTO)		70±2℃, 96 hours	
Low Temperature Storage (LTS)		-30±2℃, 200 hours	
Low Temperature Operating (LTO)		-20±2℃, 96 hours	
High Temperature / High Humidity Storage (HTHHS)		50±3℃, 90%±3%RH, 120 hours	
Thermal Shock (Non-operation) (TS)		-20±2℃ ~ 25℃ ~ 70±2℃ (30min) (5min) (30min) 10cycles	
Vibration (Packing)	10~55~10Hz,amplitude 1.5mm, 1 hour for each direction x, y, z	1. One box for each test. 2. No addition to the cosmetic and the electrical defects.	
Drop (Packing)	Height : 1 m, each time for 6 sides, 3 edges, 1 angle		
ESD (finished product housing)	±4kV (R: 330Ω C: 150pF , 10times, air discharge)	1. After testing, cosmetic and electrical defects should not happen. 2. In case of malfunction or defect caused by ESD damage, it would be judged as a good part if it would be recovered to normal state after resetting.	

Note： 1) For each reliability test, the sample quantity is 3, and only for one test item.
2) The HTHHS test is requested the Pure Water(Resistance＞10MΩ).
3) The test should be done after 2 hours of recovery time in normal environment.

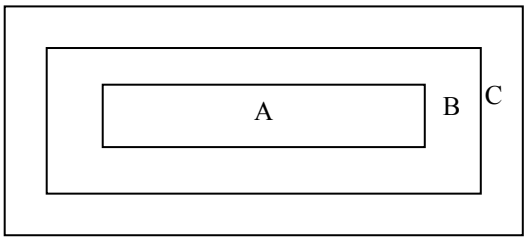
n OUTGOING QUALITY CONTROL SPECIFICATION

◆Standard

According to GB/T2828.1-2003/ISO 2859-1：1999 and ANSI/ASQC Z1.4-1993, General Inspection Level II.

◆Definition

1 Major defect: The defect that greatly affect the usability of product.
2 Minor defect: The other defects, such as cosmetic defects, etc.
3 Definition of inspection zone:



Zone A: Active Area

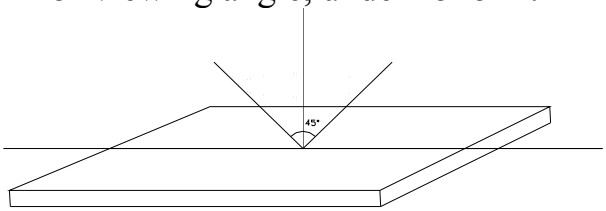
Zone B: Viewing Area except Zone A

Zone C: Outside Viewing Area

Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble of quality and assembly to customer's product.

◆Inspection Methods

1 The general inspection: under 20W x 2 or 40W fluorescent light, about 30cm viewing distance, within 45º viewing angle, under 25±5℃.



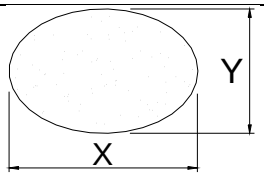
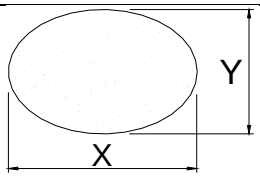
2 The luminance and color coordinate inspection: By PR705 or BM-7 or the equal equipments, in the dark room, under 25±5℃.

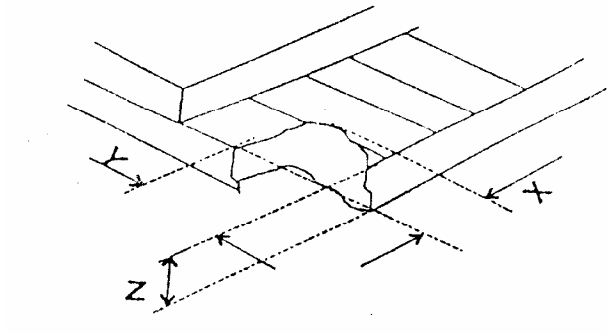
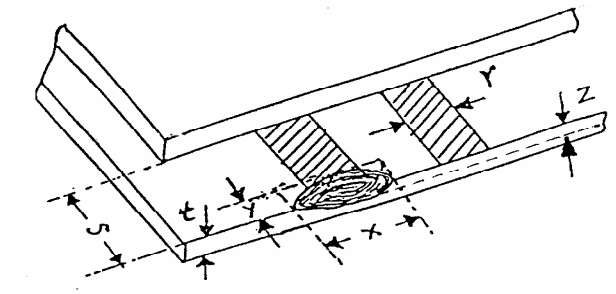
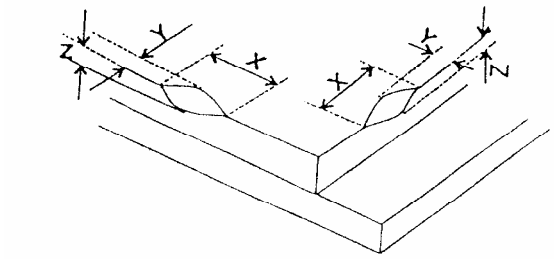
◆Inspection Criteria

1 Major defect: AQL= 0.65

Item	Criterion
Function Defect	1. No display or abnormal display is not accepted
	2. Open or short is not accepted.
	3. Power consumption exceeding the spec is not accepted.
Outline Dimension	Outline dimension exceeding the spec is not accepted.
Glass Crack	Glass crack tends to enlarge is not accepted.

2 Minor Defect: AQL= 1.5

<table>
<tr><td>Item</td><td colspan="4">Criterion</td></tr>
<tr><td rowspan="5">Spot Defect (dimming and lighting spot)</td><td colspan="2" rowspan="2">Size (mm)</td><td colspan="2">Accepted Qty</td></tr>
<tr><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="3">  </td><td>Φ≦0.07</td><td colspan="2">Ignored</td></tr>
<tr><td>0.07＜Φ≦0.10</td><td>3</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.10＜Φ≦0. 15</td><td>1</td></tr>
<tr><td colspan="4">Note : Φ= (x + y) / 2</td><td>0.15＜Φ</td><td>0</td></tr>
<tr><td rowspan="6">Line Defect (dimming and lighting line)</td><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.02</td><td colspan="2">Ignored</td></tr>
<tr><td>L≦3.0</td><td>0.02＜W≦0.03</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>L≦2.0</td><td>0.03＜W≦0.05</td><td>1</td></tr>
<tr><td>/</td><td>0.05＜W</td><td>As spot defect</td></tr>
<tr><td colspan="5">Remarks: The total of spot defect and line defect shall not exceed 4 pcs. The distance between two lines defects must exceed 1 mm</td></tr>
<tr><td>Polarizer Stain</td><td colspan="4">Stain which can be wiped off lightly with a soft cloth or similar cleaning is accepted, otherwise, according to the Spot Defect and the Line Defect.</td></tr>
<tr><td rowspan="6">Polarizer Scratch</td><td colspan="4">1. If scratch can be seen during operation, according to the criterions of the Spot Defect and the Line Defect.</td></tr>
<tr><td colspan="4">2. If scratch can be seen only under non-operation or some special angle, the criterion is as below :</td></tr>
<tr><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.02</td><td colspan="2">Ignore</td></tr>
<tr><td>3.0＜L≦5.0</td><td>0.02＜W≦0.04</td><td>2</td><td rowspan="3">Ignore</td></tr>
<tr><td>L≦3.0</td><td>0.04＜W≦0.06</td><td>1</td></tr>
<tr><td>/</td><td>0.06＜W</td><td>0</td></tr>
<tr><td rowspan="5">Polarizer Air Bubble</td><td colspan="2">Size</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="4">  </td><td>Φ≦0.20</td><td colspan="2">Ignored</td></tr>
<tr><td>0.20＜Φ≦0.30</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.30＜Φ≦0.50</td><td>1</td></tr>
<tr><td>0.50＜Φ</td><td>0</td></tr>
</table>

<table>
<tr><td rowspan="4">Glass Defect (Glass Chiped)</td><td>1. On the corner
 
(mm)
<table><tr><td>x</td><td>≤ 1.5</td></tr><tr><td>y</td><td>≤ 1.5</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>2. On the bonding edge
 
(mm)
<table><tr><td>x</td><td>≤ a / 4</td></tr><tr><td>y</td><td>≤ s / 3 &≤0.7</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>3. On the other edges
 
(mm)
<table><tr><td>x</td><td>≤ a / 8</td></tr><tr><td>y</td><td>≤ 0.7</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>Note: t: glass thickness ; s: pad width ; a: the length of the edge</td></tr>
<tr><td>TCP Defect</td><td>Crack, deep fold and deep pressure mark on the TCP are not accepted</td></tr>
<tr><td>Pixel Size</td><td>The tolerance of display pixel dimension should be within ±20% of the spec</td></tr>
<tr><td>Luminance</td><td>Refer to the spec or the reference sample</td></tr>
<tr><td>Color</td><td>Refer to the spec or the reference sample</td></tr>
</table>

n CAUTIONS IN USING OLED MODULE

◆Precautions For Handling OLED Module:

1. OLED module consists of glass and polarizer. Pay attention to the following items when handling:
   i. Avoid drop from high, avoid excessive impact and pressure.
   ii. Do not touch, push or rub the exposed polarizes with anything harder than an HB pencil lead.
   iii. If the surface becomes dirty, breathe on the surface and gently wipe it off with a soft dry cloth. If it is terrible dirty, moisten the soft cloth with Isopropyl alcohol or Ethyl alcohol. Other solvents may damage the polarizer. Especially water, Ketone and Aromatic solvents.
   iv. Wipe off saliva or water drops immediately, contact the polarizer with water over a long period of time may cause deformation.
   v. Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peeling-off may occur with high temperature and high humidity.
   vi. Condensation on the surface and the terminals due to cold or anything will damage, stain or dirty the polarizer, so make it clean as the way of iii.
2. Do not attempt to disassemble or process the OLED Module.
3. Make sure the TCP or the FPC of the Module is free of twisting, warping and distortion, do not pull or bend them forcefully, especially the soldering pins. On the other side, the SLIT part of the TCP is made to bend in the necessary case.
4. When assembling the module into other equipment, give the glass enough space to avoid excessive pressure on the glass, especially the glass cover which is much more fragile.
5. Be sure to keep the air pressure under 120 kPa, otherwise the glass cover is to be cracked.
6. Be careful to prevent damage by static electricity:
   i. Be sure to ground the body when handling the OLED Modules.
   ii. All machines and tools required for assembling, such as soldering irons, must be properly grounded.
   iii. Do not assemble and do no other work under dry conditions to reduce the amount of static electricity generated. A relative humidity of 50%-60% is recommended.
   iv. Peel off the protective film slowly to avoid the amount of static electricity generated.
   v. Avoid to touch the circuit, the soldering pins and the IC on the Module by the body.
   vi. Be sure to use anti-static package.
7. Contamination on terminals can cause an electrochemical reaction and corrade the terminal circuit, so make it clean anytime.
8. All terminals should be open, do not attach any conductor or semiconductor on the terminals.
9. When the logic circuit power is off, do not apply the input signals.
10. Power on sequence: $V_{DD} \rightarrow V_{PP}$, and power off sequence: $V_{PP} \rightarrow V_{DD}$.
11. Be sure to keep temperature, humidity and voltage within the ranges of the spec, otherwise shorten Module’ s life time, even make it damaged.
12. Be sure to drive the OLED Module following the Specification and datasheet of IC controller, otherwise something wrong may be seen.

13. When displaying images, keep them rolling, and avoid one fixed image displaying more than 30 seconds, otherwise the residue image is to be seen. This is the speciality of OLED.

◆Precautions For Soldering OLED Module:

1. Soldering temperature : 260°C ± 10°C.
2. Soldering time : 3-4 sec.
3. Repeating time : no more than 3 times.
4. If soldering flux is used, be sure to remove any remaining flux after finishing soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended to protect the surface with a cover during soldering to prevent any damage due to flux spatters.

◆ Precautions For Storing OLED Module:

1. Be sure to store the OLED Module in the vacuum bag with dessicant.
2. If the Module can not be used up in 1 month after the bag being opened, make sure to seal the Module in the vacuum bag with dessicant again.
3. Store the Module in a dark place, do not expose to sunlight or fluorescent light.
4. The polarizer surface should not touch any other objects. It is recommended to store the Module in the shipping container.
5. It is recommended to keep the temperature between 0°C and 30°C , the relative humidity not over 60%.

◆ Limited Warranty

Unless relevant quality agreements signed with customer and law enforcement, for a period of 12 months from date of production, all products (except automotive products) TRULY will replace or repair any of its OLED modules which are found to be functional defect when inspected in accordance with TRULY OLED acceptance standards (copies available upon request). Cosmetic/visual defects must be returned to TRULY within 90 days of shipment. Confirmation of such date should be based on freight documents. The warranty liability of TRULY is limited to repair and/or replacement on the terms above. TRULY will not be responsible for any subsequent or consequential events.

◆Return OLED Module Under Warranty:

1. No warranty in the case that the precautions are disregarded.
2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects.

◆PRIOR CONSULT MATTER

1. For TRULY standard products , we keep the right to change material ,process … for improving the product property without any notice on our customer.
2. If you have special requirement about reliability condition, please let us know before you start the test on our samples.