High Voltage, High Efficiency 65W Buck Converter

Features

- Selectable Switching Frequency up to 2 MHz
- Optimal High Efficiencies for 3.3 V to 21 V Vout
- Maximum Output Current of 3.25 A
- Wide Input Voltage Range: 7 V to 27 V
- Selectable Soft Start Times
- OCP/OVP/OTP Protections
- Programmable UVLO
- 3 mm x 3 mm QFN Package

Applications

- VBUS Supply Generation for USB-PD Ports:
  - Multiple Output USB-PD Chargers
  - Charging Hubs
  - Displays and Televisions
  - Laptop Docking Stations

Product Description

The SZPL3102A is a fully integrated high efficiency synchronous buck DC/DC converter intended to be paired with USB port controllers. The device is optimized for the highest efficiency performance, including dual input LDOs for self-bias, across a wide output voltage range.

The SZPL3102A is designed to supply the full range VBUS rail for USB-PD SPR ports and can be controlled by popular USB-PD controllers or fast charging devices. On start-up, the device employs an internal feedback path to allow safe regulation until the external PD controller powers up and becomes available to regulate the output voltage. Following this initial start-up period, the SZPL3102A hands over output control to the external PD controller.

The SZPL3102A is available in a compact 3 mm x 3 mm custom QFN package, delivering high power density with a minimal number of external components.

Application Diagram

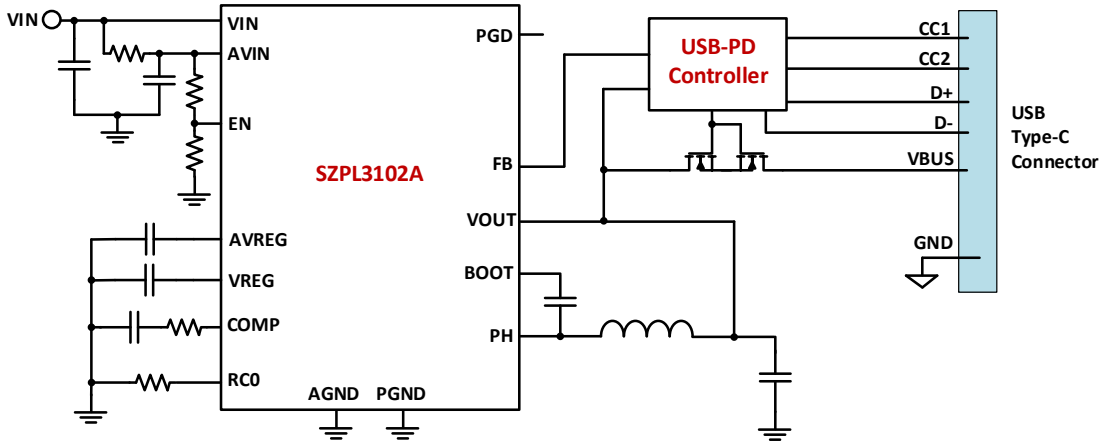

Figure 1. Typical SZPL3102A USB-PD Port Application Diagram

Package Pinout

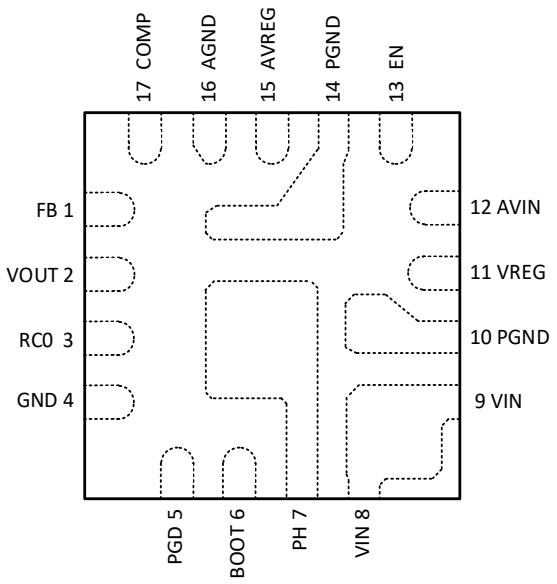

Figure 2. Package Pinout - Top View

Pin Definitions

Pin #	Name	Description
1	FB	Feedback input pin, nominally regulated to 1.25 V. Connect to the tap of a VOUT-to-AGND resistor divider network (if needed by the USB port controller device) and the analog feedback control output of a USB port controller device.
2	VOUT	Voltage sense line from regulated output of converter and secondary input to internal LDOs.
3	RC0	Analog input. A resistor to ground sets switching frequency (F_{SW}) and soft start time (t_{SS}).
4	GND	Connect to ground.
5	PGD	Power good output signal. Active high, open drain output. Connect to pullup resistor to VREG.
6	BOOT	Bootstrap high side driver voltage supply. Connect to 0.1 uF capacitor to PH node.
7	PH	Phase (switch) node of the buck converter's output FETs. Connect to output inductor.
8, 9	VIN	Input voltage to the buck converter's output FETs (high side drain). Locally decouple with 1 uF + 0.1 uF capacitors, followed by enough capacitors to provide the required input RMS current.
10	PGND	Power ground connection of output FETs (low side source). Connect to ground.
11	VREG	Internal 3.3 V LDO output. Connect to a 1 uF bypass capacitor to ground.
12	AVIN	Input voltage to the buck converter for analog circuits. Connect to tap of VIN RC low-pass filter.
13	EN	Analog control input. A potential higher than the UVLO threshold enables switching operation and output soft start process. A potential lower than the shutdown threshold places the device in a low power state. Decouple with one 1 nF to 100 nF capacitor placed close to the part. See the Functional Description paragraph for a more detailed explanation of operation.
14	PGND	Connect to ground.
15	AVREG	Internal 3.3 V LDO output. Connect a 1 uF bypass capacitor to ground.
16	AGND	Connect to ground.
17	COMP	Compensation error amplifier output. Connect to a RC network to ground. See the Applications Information section for recommendations.

Functional Block Diagram

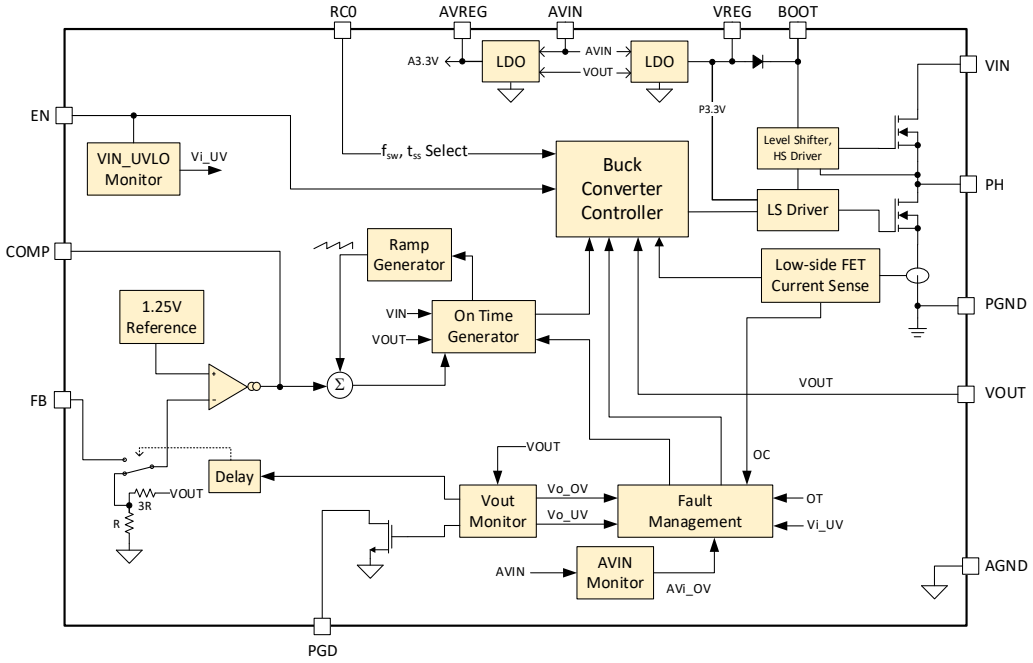

Figure 3. Functional Block Diagram

Product Ordering Information

Part Number	Package	Description
SZPL3102A-CF33	QFN (3 mm x 3 mm)	Integrated, Wide Voltage, Buck Converter with Momentary Feedback Divider

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