

6CH VIDEO AMPLIFIER WITH SD/ HD LPF

■ GENERAL DESCRIPTION

The NJM2583A is a single supply voltage 6ch Video amplifier. It includes LPF, Y/C MIX circuit and SDC interface. LPF for the component signal can select SD/HD.

The NJM2583A is suitable for DVD recorder, set top box and the high quality AV systems with the SD/HD output.

■ PACKAGE OUTLINE



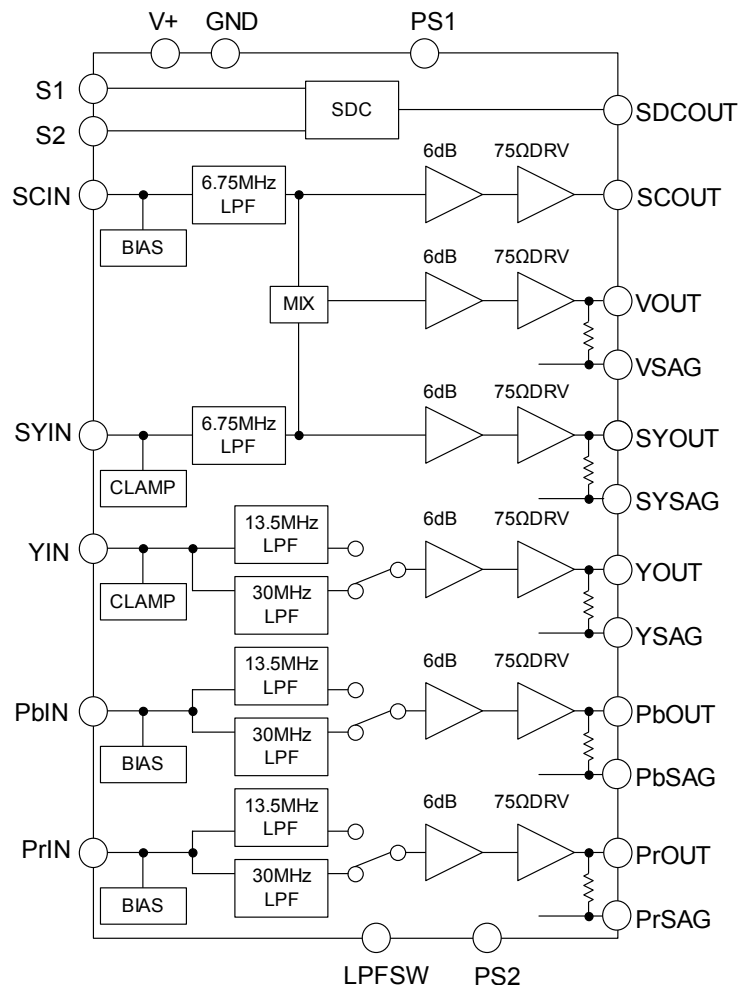
NJM2583AV

■ FEATURES

- Operating Voltage +4.5 to +5.5V
- SY,SC,Y,Pb,Pr Inputs
- 6dB Amplifier
- Internal 75Ω Driver Circuit
- 4th Order LPF

V, SY, SC	6.75MHz
Y, Pb, Pr	13.5MHz (Progressive), 30MHz (HD)
- Y/C MIX Circuit
- SDC Interface (S1/ S2)
- Power Save Circuit
- Bipolar Technology
- Package Outline SSOP32

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V ⁺	10.0	V
Power Dissipation	P _D	1250 (Note 1)	mW
Operating Temperature Range	T _{opr}	-40 to +85	°C
Storage Temperature Range	T _{stg}	-40 to +150	°C

(Note 1) At on a board of EIA/JEDEC specification. (114.3 x 76.2 x 1.6mm 2 layers, FR-4)

■ RECOMMENDED OPERATING CONDITION (Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V _{opr}		+4.5	+5.0	+5.5	V

■ ELECTRICAL CHARACTERISTICS (Ta=25°C, V⁺=5V, R_L=150Ω)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I _{CC}	No Signal	-	65	90	mA
Operating Current at Power Save	I _{save}	Power Save Mode	-	2.0	4.0	mA
Maximum Output Voltage Swing	V _{om}	(Note 2) Vin=100kHz, Sine Signal, THD=1%	2.4	-	-	Vp-p
Voltage Gain1	G _{v1}	(Note 2) Vin=1MHz, 1.0Vp-p, Sine Signal	5.8	6.3	6.8	dB
Voltage Gain2	G _{v2}	(Note 3) Vin=3.58MHz, 0.3Vp-p, Sine Signal	5.8	6.3	6.8	dB
Gain Difference Between channel	ΔG _{v1}	(Note 2) Vin=1MHz, 1.0Vp-p, Sine Signal	-0.2	0	+0.2	dB
Low Pass Filter Characteristic 1	G _{fy6.75M}	(Note 4) 6.75MHz/1MHz, 1.0Vp-p, Sine Signal	-1.0	0	1.0	dB
	G _{fy27M}	(Note 4) 27MHz/1MHz, 1.0Vp-p, Sine Signal	-	-40	-24	dB
Low Pass Filter Characteristic 2	G _{fc6.75M}	(Note 3) 6.75MHz/3.58MHz, 0.3Vp-p, Sine Signal	-1.0	0	1.0	dB
	G _{fc27M}	(Note 3) 27MHz/3.58MHz, 0.3Vp-p, Sine Signal	-	-40	-24	dB
Low Pass Filter Characteristic 3	G _{fSD13.5M}	(Note 5) 13.5MHz/1MHz, 1.0Vp-p, Sine Signal	-1.0	0	1.0	dB
	G _{fSD54M}	(Note 5) 54MHz/1MHz, 1.0Vp-p, Sine Signal	-	-40	-24	dB
Low Pass Filter Characteristic 4	G _{fHD30M}	(Note 6) 30MHz/1MHz, 1.0Vp-p, Sine Signal	-1.0	0	1.0	dB
	G _{fHD100M}	(Note 6) 100MHz/1MHz, 1.0Vp-p, Sine Signal	-	-40	-24	dB
Differential Gain	DG	(Note 2) Vin=1.0Vp-p, 10step Video Signal	-	0.5	-	%
Differential Phase	DP	(Note 2) Vin=1.0Vp-p, 10step Video Signal	-	0.5	-	deg
S/N Ratio1	SN1	(Note 2) Vin=1.0Vp-p, 100% White video signal, R _L =75Ω, 100KHz to 6MHz	-	80	-	dB
S/N Ratio2	SN2	Vin=1.0Vp-p, 100% White video signal, R _L =75Ω, 100KHz to 6MHz, Y/C MIX OUT	-	70	-	dB

(Note 2) (SYIN, YIN, PbIN, PrIN) Input

(Note 3) (SCIN) Input

(Note 4) (SYIN) Input

(Note 5) (YIN, PbIN, PrIN) Input, 13.5MHz LPF

(Note 6) (YIN, PbIN, PrIN) Input, 30MHz LPF

■ ELECTRICAL CHARACTERISTICS (Ta=25°C, V⁺= 5V, R_L=150Ω)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
SDC Output Voltage Low Level	SDCL	RL=2kΩ+100kΩ	-	0.1	0.5	V
SDC Output Voltage Mid Level	SDCM	RL=2kΩ+100kΩ	1.6	2.1	2.4	V
SDC Output Voltage High Level	SDCH	RL=2kΩ+100kΩ	4.3	4.6	-	V
SW Voltage High Level	VthH		2.2	-	V ⁺	V
SW Voltage Low Level	VthL		0	-	1.0	V
Switch inflow current High Level	I _{SWH}	V=5V	-	-	120	μA
Switch inflow current Low Level	I _{SWL}	V=0.3V	-	-	8.0	μA

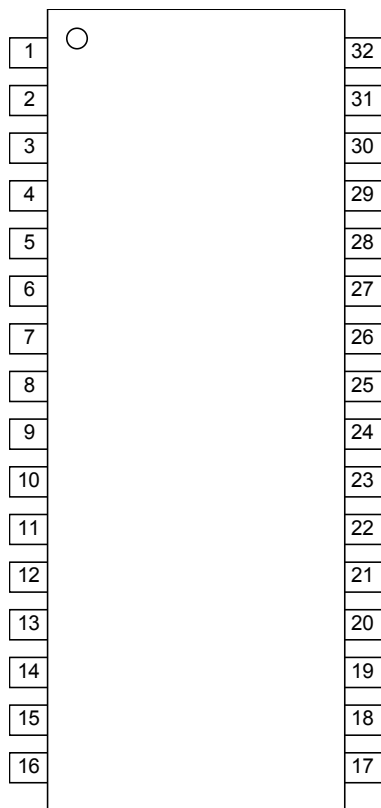
■ CONTROL TERMINAL

PARAMETER	STATUS	NOTE
PS1 (Power Save1)	H	(SY, V, SC) Power Save: OFF (Active)
	L	(SY, V, SC) Power Save: ON (Mute)
	OPEN	(SY, V, SC) Power Save: ON (Mute)
PS2 (Power Save2)	H	(Y, Pb, Pr) Power Save: OFF (Active)
	L	(Y, Pb, Pr) Power Save: ON (Mute)
	OPEN	(Y, Pb, Pr) Power Save: ON (Mute)
LPF SW (LPF)	H	30MHz LPF
	L	13.5MHz LPF
	OPEN	13.5MHz LPF

■ SDC OUT

S1	S2	SDC OUT	Aspect Ratio
L (OPEN)	L (OPEN)	0V	4:3 Normal
L (OPEN)	H	2.1V	4:3 Letter box
H	H	2.1V	4:3 Letter box
H	L (OPEN)	4.6V	16:9 Squeeze

■ PIN CONFIGURATION



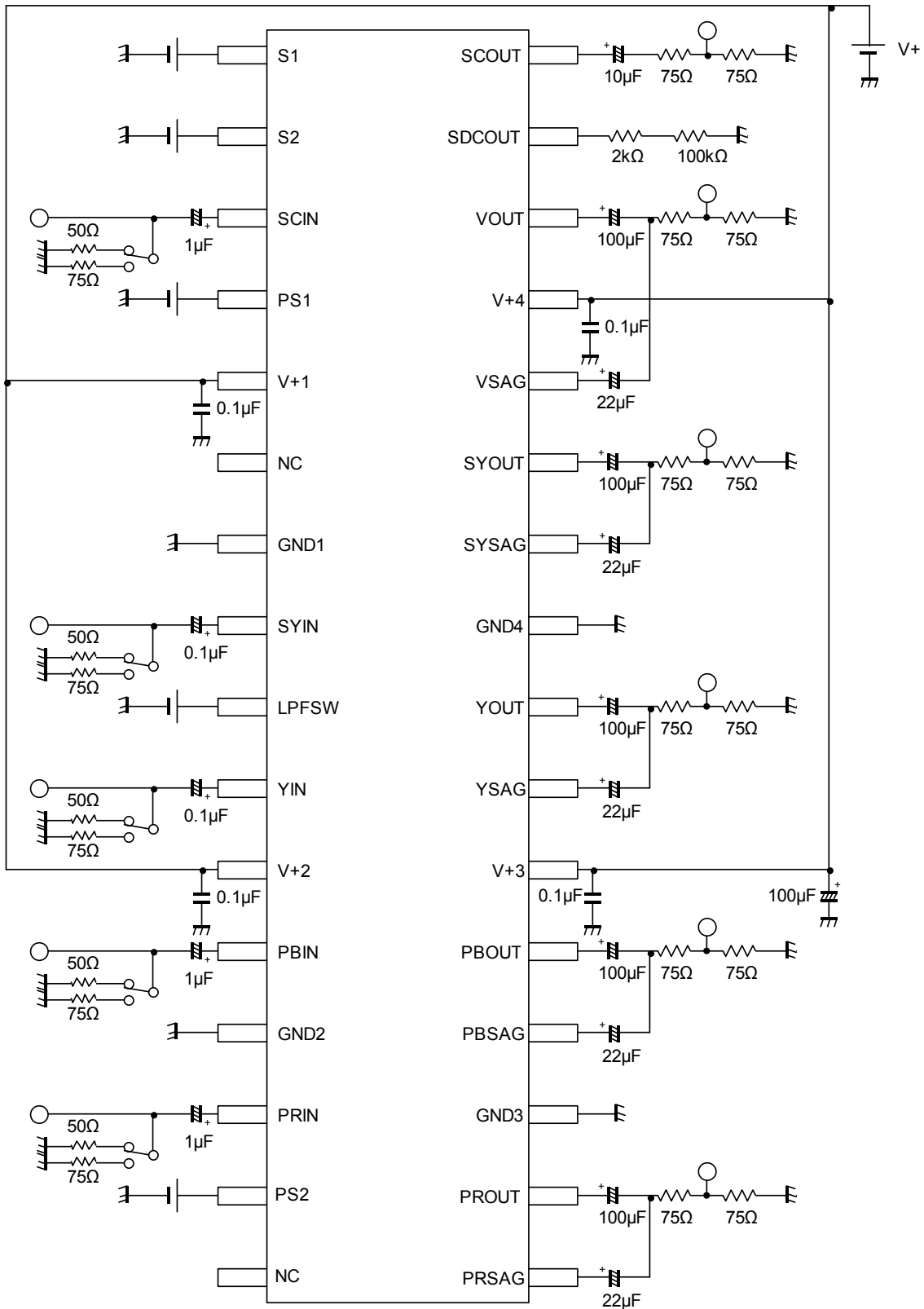
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|----------|------------|
| 1. S1 | 17. PRSAG |
| 2. S2 | 18. PROUT |
| 3. SCIN | 19. GND3 |
| 4. PS1 | 20. PBSAG |
| 5. V+1 | 21. PBOUT |
| 6. NC | 22. V+3 |
| 7. GND | 23. YSAG |
| 8. SYIN | 24. YOUT |
| 9. LPFSW | 25. GND4 |
| 10. YIN | 26. SYSAG |
| 11. V+2 | 27. SYOUT |
| 12. PBIN | 28. VSAG |
| 13. GND2 | 29. V+4 |
| 14. PRIN | 30. VOUT |
| 15. PS2 | 31. SDCOUT |
| 16. NC | 32. SCOUT |

■ TERMINAL FUNCTION

PIN No.	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT	DC VOLTAGE
1	S2	SDC control		-
2	S1	SDC control		
4	PS1	(SY, V, SC, SDC) Power save		
9	LPFSW	(Y, Pb, Pr) LPF control		
15	PS2	(Y, Pb, Pr) Power save		
3	SCIN	Chroma signal input		2.5V
12	PBIN	Component signal (Pb) input		
14	PRIN	Component signal (Pr) input		
8	SYIN	Y signal input		1.7V
10	YIN	Component signal (Y), G input		
17	PRSAG	Component signal (Pr) sag correction		2.5V
20	PBSAG	Component signal (Pb) sag correction		
23	YSAG	Component signal (Y) sag correction		1.3V
26	SYSAG	Y signal sag correction		
28	VSAG	Composite video signal sag correction		

PINNo.	PINNAME	FUNCTION	EQUIVALENT CIRCUIT	DC VOLTAGE
18	PROUT	Component signal (Pr) output		2.5V
21	PBOUT	Component signal (Pb) output		1.3V
24	YOUT	Component signal(Y) output		
27	SYOUT	Y signal output		
30	VOUT	Composite video signal output		
31	SDCOUT	SDC output		-
32	SCOUT	Chroma signal output		2.5V

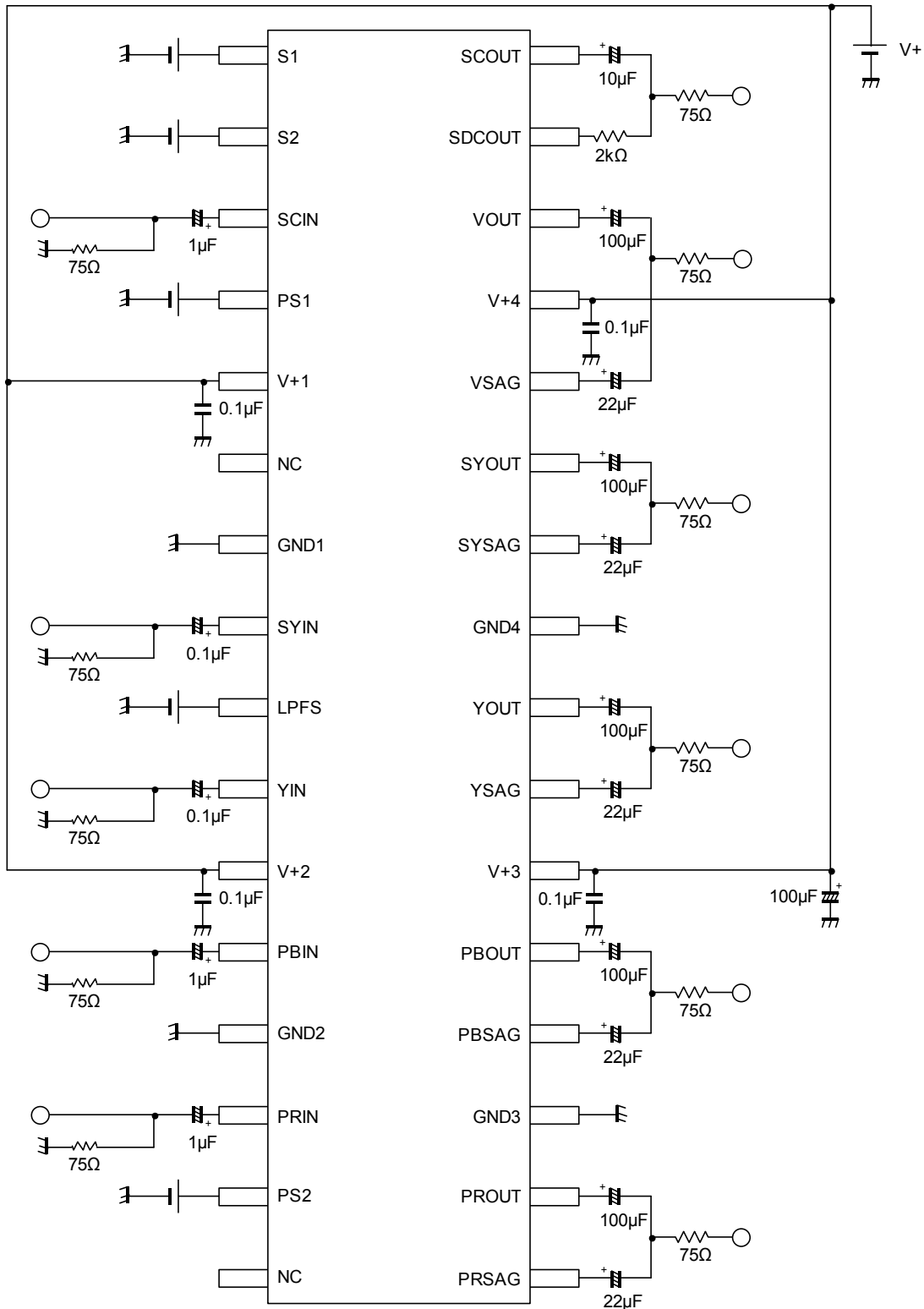
TEST CIRCUIT



(Note)

1. Put a bypass capacitor of $0.1\mu\text{F}$ near a $V+$ pin ($V+1$ to $V+4$).
2. Shorten the feedback loop of an output coupling capacitor and the SAG correction capacitor of the video signal output and put a 75Ω series resistance near IC pin.

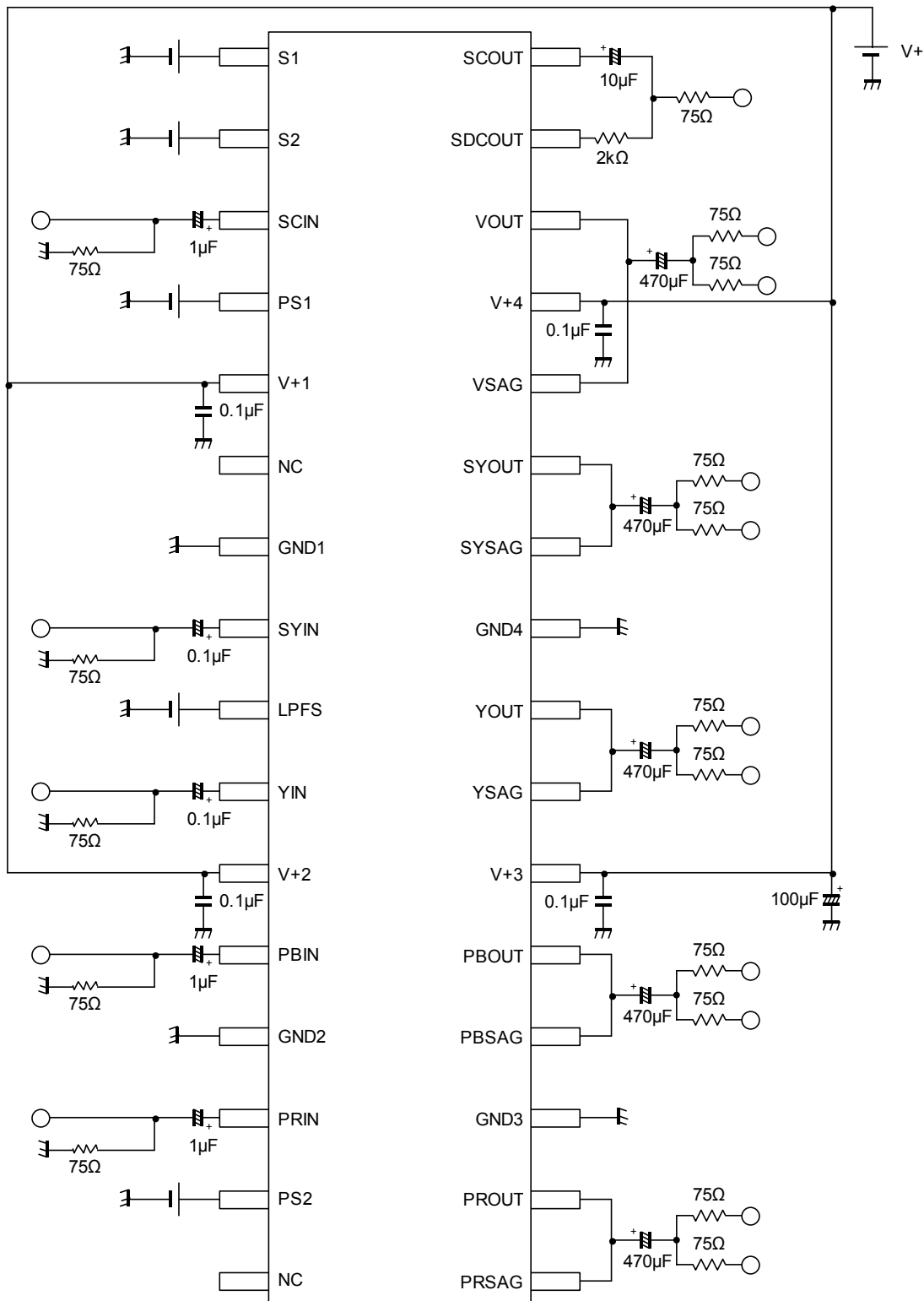
APPLICATION CIRCUIT 1



(Note)

1. Put a bypass capacitor of 0.1μF near a V+ pin (V+1 to V+4).
2. Shorten the feedback loop of an output coupling capacitor and the SAG correction capacitor of the video signal output and put a 75Ω series resistance near IC pin.

APPLICATION CIRCUIT 2 (Two-line driving circuit)

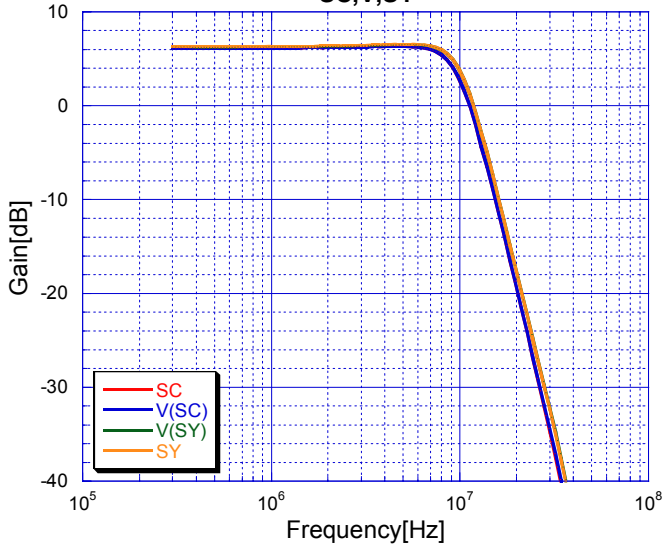


(Note)

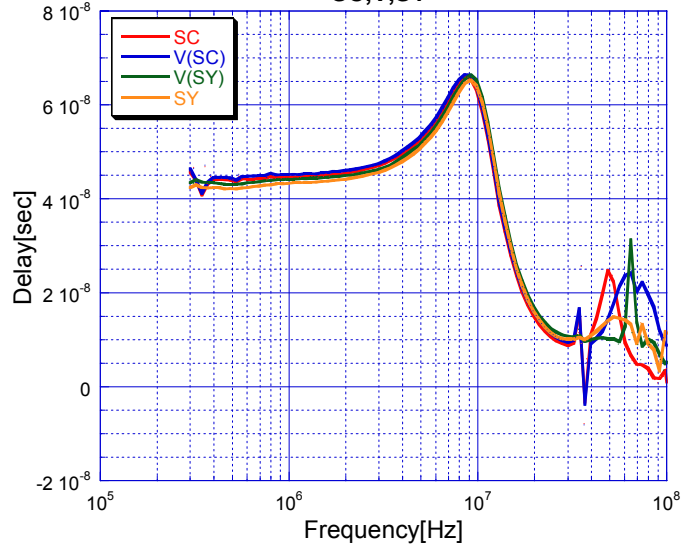
1. Put a bypass capacitor of $0.1\mu\text{F}$ near a V+ pin (V+1 to V+4).
2. Shorten the feedback loop of an output coupling capacitor and the SAG correction capacitor of the video signal output and put a 75Ω series resistance near IC pin.
3. Two-line driving circuit
 This circuit drives two-line of 150Ω . However, it may cause to lose synchronization by an input signal of large APL change (100% white signals more than 1Vp-p). Confirm the large APL change waveform (100% white signals more than 1Vp-p) and evaluate sufficiently.

TYPICAL CHARACTERISTICS

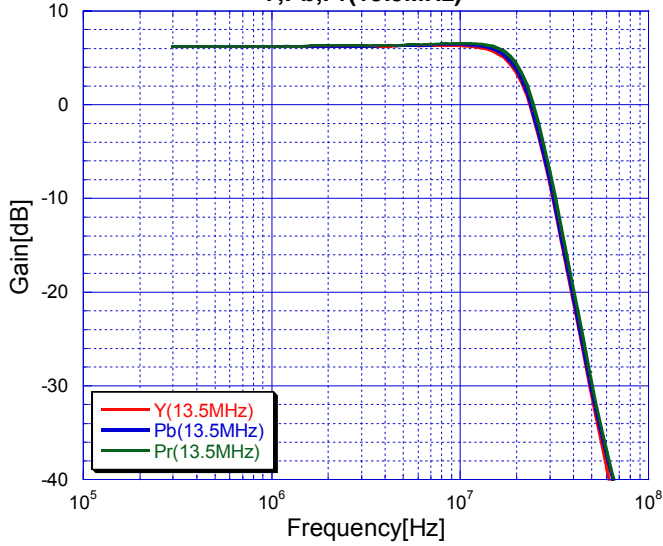
**Voltage Gain vs. Frequency
SC,V,SY**



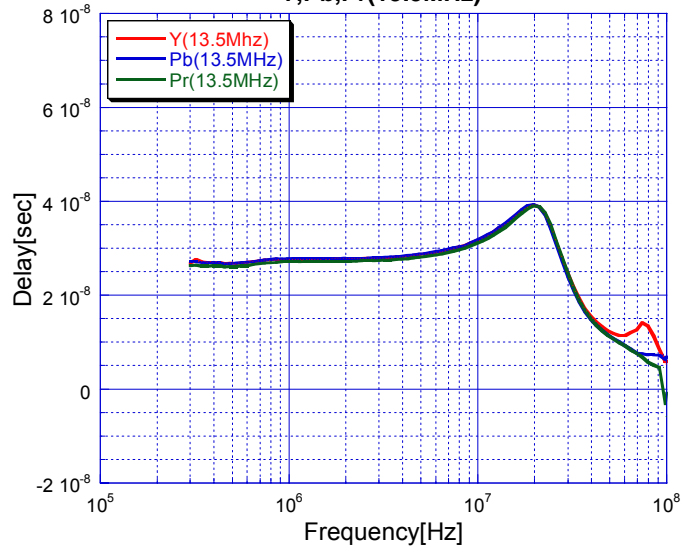
**Group Delay vs. Frequency
SC,V,SY**



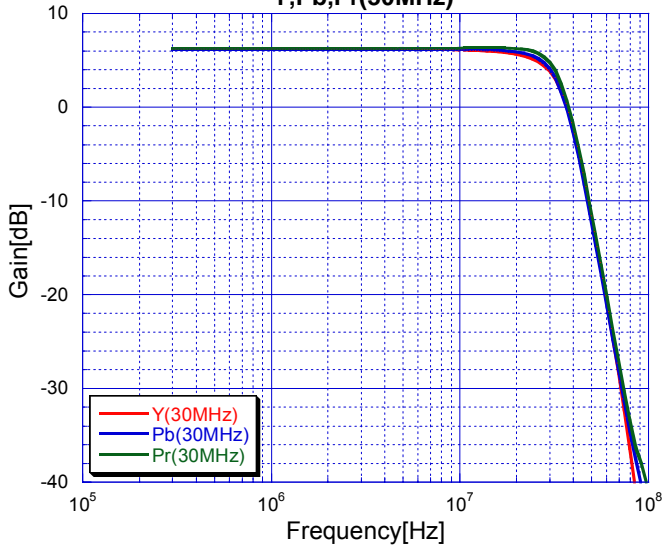
**Voltage Gain vs. Frequency
Y,Pb,Pr(13.5MHz)**



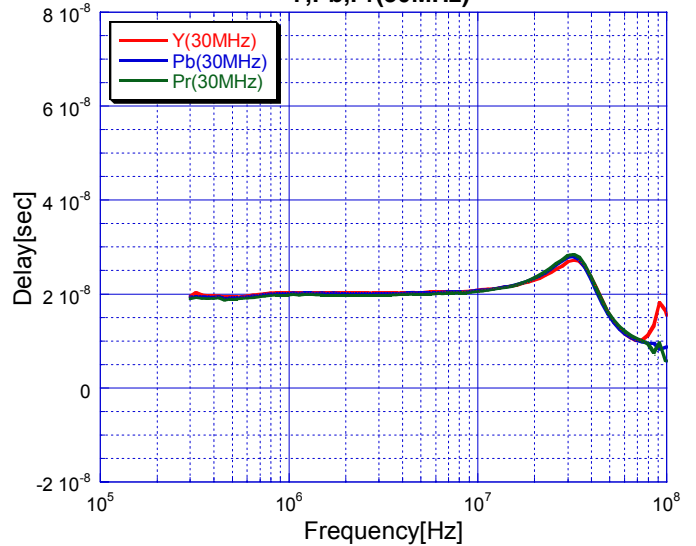
**Group Delay vs. Frequency
Y,Pb,Pr(13.5MHz)**



**Voltage Gain vs. Frequency
Y,Pb,Pr(30MHz)**



**Group Delay vs. Frequency
Y,Pb,Pr(30MHz)**





[CAUTION]
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