



UT30P04

Power MOSFET

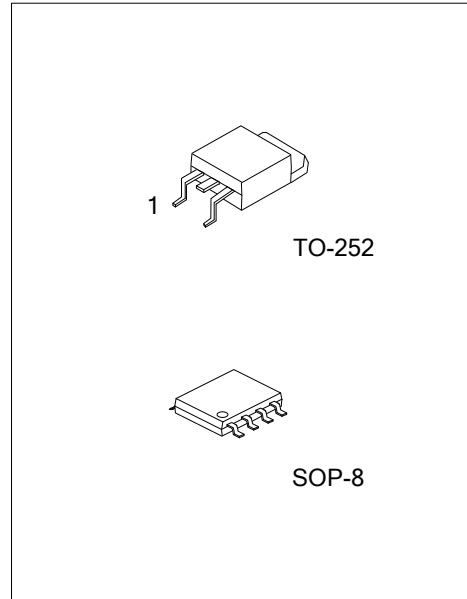
P-CHANNEL ENHANCEMENT MODE POWER MOSFET

DESCRIPTION

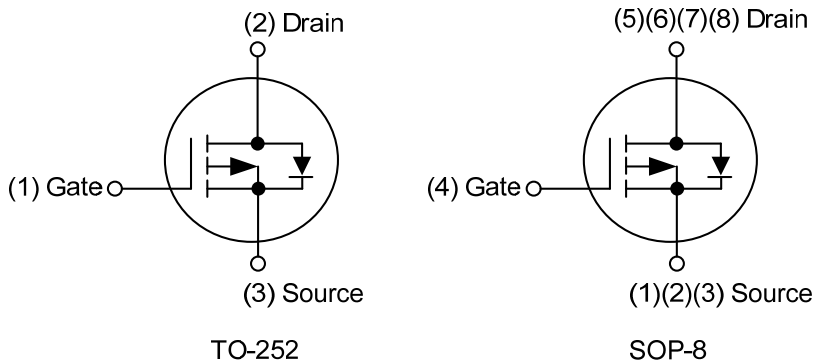
The UTC **UT30P04** is a P-channel enhancement mode Power MOSFET, providing customers fast switching, ruggedized device design, low on-resistance and cost-effectiveness with UTC's advanced technology.

FEATURES

- * $R_{DS(ON)} \leq 36 \text{ m}\Omega @ V_{GS}=-10\text{V}, I_D=-15\text{A}$
- $R_{DS(ON)} \leq 52 \text{ m}\Omega @ V_{GS}=-4.5\text{V}, I_D=-15\text{A}$
- * Low on-Resistance
- * Fast Switching Speed



SYMBOL



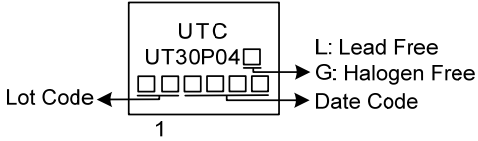
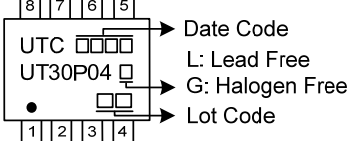
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT30P04L-TN3-R	UT30P04G-TN3-R	TO-252	G	D	S	-	-	-	-	-	Tape Reel
UT30P04L-S08-R	UT30P04G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UT30P04G-TN3-R</p> <ul style="list-style-type: none"> (1)Packing Type (2)Package Type (3)Green Package 	<ul style="list-style-type: none"> (1) R: Tape Reel (2) TN3: TO-252, S08: SOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING

TO-252	SOP-8
 <p>The diagram shows a TO-252 package with the following markings: 'UTC' and 'UT30P04' at the top. Below 'UT30P04' are five small squares. An arrow labeled 'Lot Code' points to the first square. An arrow labeled 'Date Code' points to the last square. To the right of the package, 'L: Lead Free' and 'G: Halogen Free' are listed with arrows pointing to the top and bottom of the package respectively. A '1' is located at the bottom center of the package.</p>	 <p>The diagram shows an SOP-8 package with the following markings: 'UTC' and 'UT30P04' in the center. Above the package are five squares labeled 8, 7, 6, 5, 4, 3, 2, 1 from left to right. An arrow labeled 'Date Code' points to squares 8, 7, 6, 5. An arrow labeled 'L: Lead Free' points to square 4. An arrow labeled 'G: Halogen Free' points to square 3. An arrow labeled 'Lot Code' points to square 2. A dot is located at the bottom left of the package.</p>

■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$ Unless Otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current ($T_C=25^\circ\text{C}$)		I_D	-30	A
Pulsed Drain Current (Note 2)		I_{DM}	-60	A
Avalanche Energy (Note 3)		E_{AS}	39	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	1.1	V/nS
Power Dissipation	$T_C=25^\circ\text{C}$	TO-252	50	W
		SOP-8	1.9	W
Operating Junction Temperature		T_J	-55 ~ +150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L=0.1\text{mH}$, $I_{AS}=-27.9\text{A}$, $V_{DD}=-20\text{V}$, $R_G=25\Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq -30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-252	θ_{JA}	110	$^\circ\text{C}/\text{W}$
	SOP-8		90 (Note)	$^\circ\text{C}/\text{W}$
Junction to Case (Note)	TO-252	θ_{JC}	2.5 (Note)	$^\circ\text{C}/\text{W}$
	SOP-8		65.7 (Note)	$^\circ\text{C}/\text{W}$

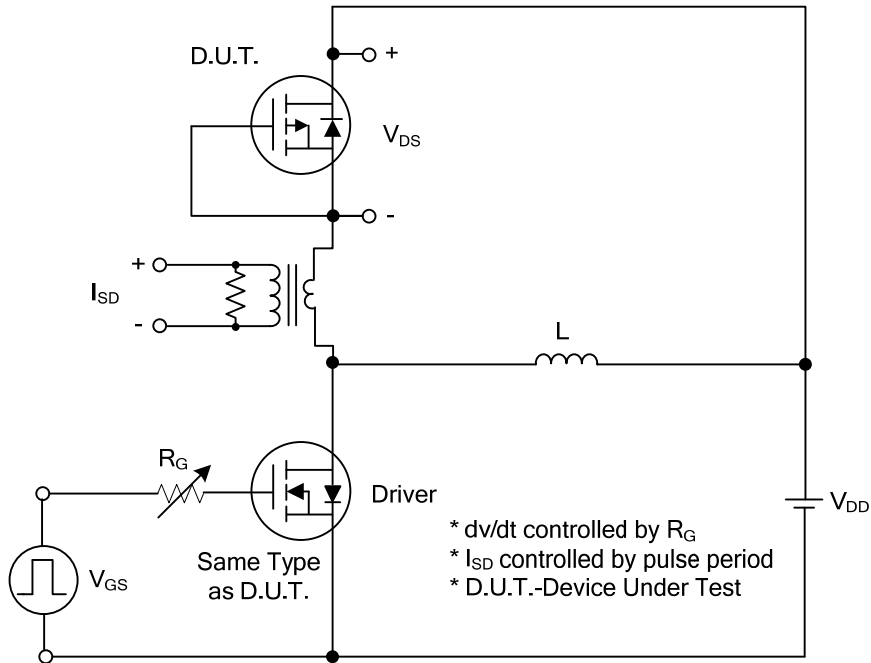
Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

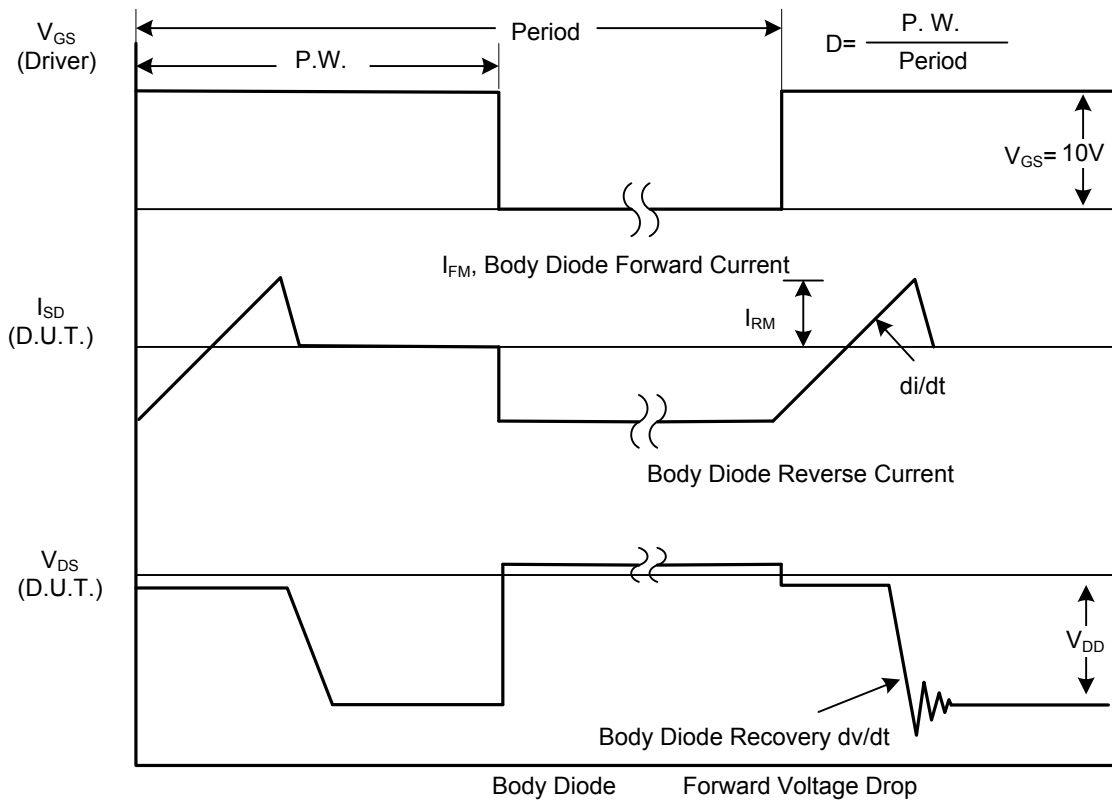
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = -250\mu\text{A}$, $V_{GS} = 0\text{V}$	-40			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS} = -40\text{V}$, $V_{GS} = 0\text{V}$			-1	μA
Gate- Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{V}$, $V_{GS} = \pm 20\text{V}$			± 250	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, $I_D = -250\mu\text{A}$	-1.0		-3.0	V
Static Drain-Source On-State Resistance (Note 1)	$R_{DS(ON)}$	$V_{GS} = -10\text{V}$, $I_D = -15\text{A}$			36	$\text{m}\Omega$
		$V_{GS} = -4.5\text{V}$, $I_D = -15\text{A}$			52	$\text{m}\Omega$
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{V}$, $V_{DS} = -20\text{V}$, $f = 1.0\text{MHz}$		1107		pF
Output Capacitance	C_{OSS}			158		pF
Reverse Transfer Capacitance	C_{RSS}			134.9		pF
GATE CHARGE (Note 2)						
Total Gate Charge	Q_G	$V_{DS} = -32\text{V}$, $V_{GS} = -10\text{V}$, $I_D = -30\text{A}$, $I_G = -1\text{mA}$ (Note 1, 2)		30		nC
Gate to Source Charge	Q_{GS}			3.5		nC
Gate to Drain Charge	Q_{GD}			10.9		nC
SWITCHING PARAMETERS (Note 2)						
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DS} = -15\text{V}$, $V_{GS} = -10\text{V}$, $I_D = -30\text{A}$, $R_{GS} = 6.0\Omega$ (Note 1, 2)		7		ns
Rise Time	t_R			16.3		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			42.4		ns
Fall-Time	t_F			27		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I_S				-30	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				-60	A
Drain-Source Diode Forward Voltage	V_{SD}	$I_F = -10\text{A}$, $V_{GS} = 0\text{V}$			-1.2	V
Reverse Recovery Time	t_{rr}	$I_F = -30\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$		70		ns
Reverse Recovery Charge	Q_{rr}			212.6		nC

Notes: 1. Pulsed test: Pulse width $\leq 300\mu\text{sec}$, duty cycle $\leq 2\%$.
2. Independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

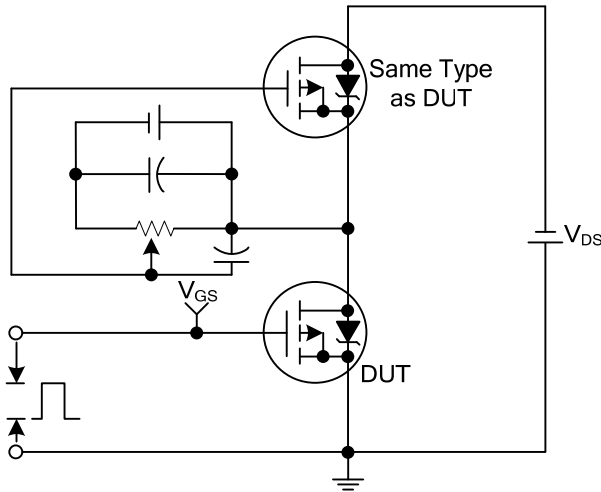


Peak Diode Recovery dv/dt Test Circuit

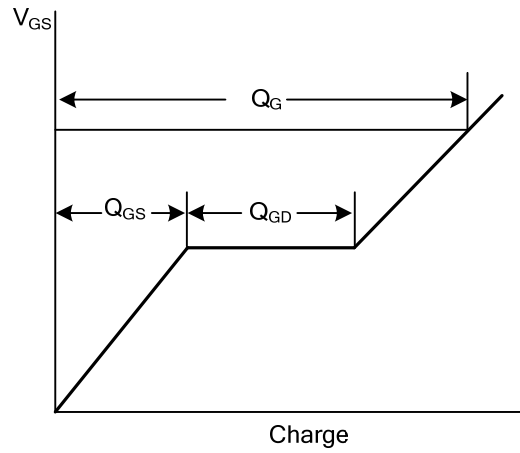


Peak Diode Recovery dv/dt Waveforms

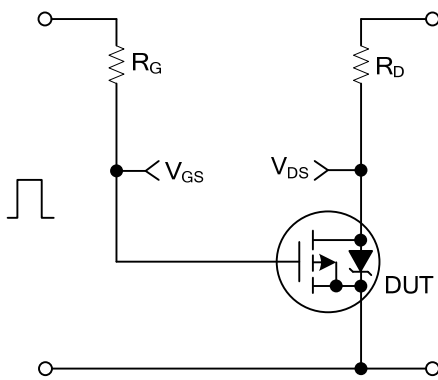
■ TEST CIRCUITS AND WAVEFORMS



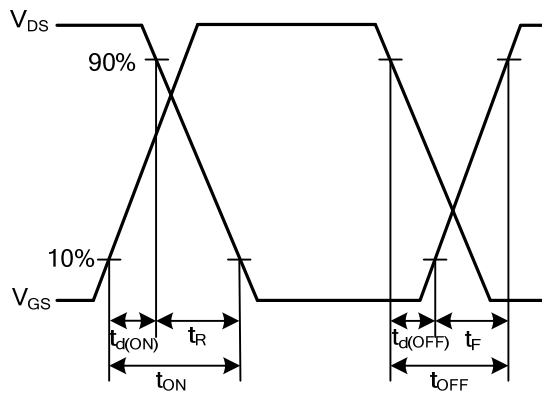
Gate Charge Test Circuit



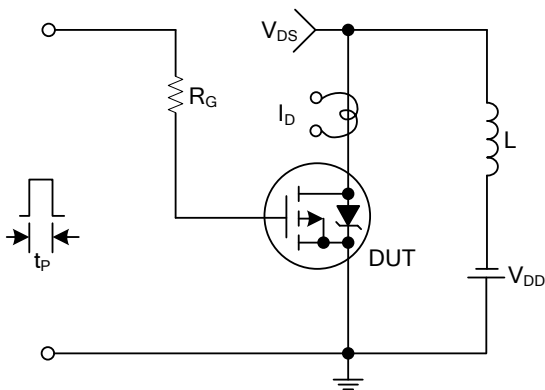
Gate Charge Waveforms



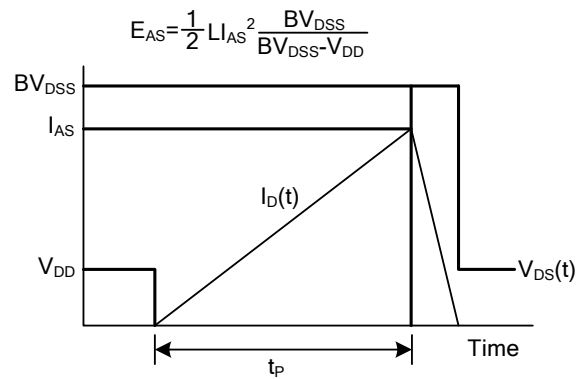
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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