YAMAR
Datasheet

SIG102 - Multi I/O Control over DC Powerline Network

1 Overview

The SIG102 transceiver device merges both data and power over the powerline, eliminating the need for control and data wires. Eight configurable I/Os ports can be configured as PWM output, Analog to digital converter (ADC) input, and digital I/Os. The SIG102 is a solution for multiple sensors and actuator networks over DC power lines.
The SIG102 is an economical device for applications as controlling motors or lights, reading sensors, etc., eliminating the need for dedicated control wires and a microcontroller (host ECU), reducing the harness size and increases reliability.
The device has a unique built-in byte-oriented UART multiplex signaling modem designed to overcome the powerline noisy conditions at bitrates up to 115.2Kbit/s. Sleep mode allows low power consumption when the device is not used. A SIG102 QFN48 (7x7 mm) package provides a small size PCB footprint

The SIG102 network consists of one SIG102 device operating as a master, controlled by any ECU via its UART port (HDI, HDO, and HDC pins). Up to 255 SIG102 devices can operate as slaves. When the device operates as a master (attached to ECU) it remotely controls other SIG102 Slaves IOs ports over the powerline and locally controls its ports.
Multiple networks can operate over the same powerline using selectable carrier frequencies between 5MHz and 30MHz in the spacing of 100 kHz.

Applications

- **Renewable energy Nano-Grid**
- **Battery management (BMS)**
- **Climate control network**
- **Sensors/actuators bus**
- **Robotics control network**
- **Lighting control**
- **Vehicle control networks**

Features

- **Master controlling up to 255 I/O slaves**
- **Standalone slave with 8 configurable digital or analog I/O pins**
- **Noise robust communication network over DC powerline**
- **Selectable bitrate from 9.6kbit/s up to 115.2kbit/s**
- **Multiple networks may operate over a single powerline**
- **251 selectable carrier frequencies (5MHz to 30MHz)**
- **Communicates over a wide range of DC voltages.**
- **Small footprint 48 pin QFN package**
- **Sleep modes for low power consumption**
- **I/O Watchdog protection**

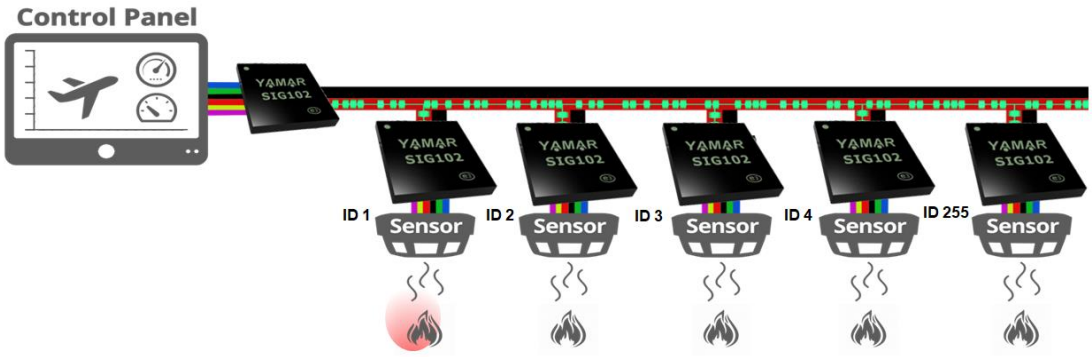

Figure 1 - SIG102 sensors actuators network

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2 Description

The SIG102 is a multi I/O powerline transceiver device with a unique modem specially designed for economical communication over a noisy DC powerline. The device has eight configurable input/output pins operating as ADC inputs, PWM outputs, and digital I/O. All eight I/O pins can be controlled remotely from a master SIG102 device over a DC powerline or locally by a host ECU's UART port using HDI, HDO, and HDC pins.
A Sleep mode reduces significantly the power consumption when there is no need for communication over the powerline.

2.1 The Signaling technology

SIG102 communication is based on a unique Signaling technology. The device transmits and receives UART bytes; modulate it by a multiphase signaling carrier over the powerline. At the receiving side, this phase-modulated pattern is extracted from the powerline and decoded back as UART bytes. There is no restriction to the number of bytes (message size).

2.2 The SIG102 network

The SIG102 operates as a Master-Slaves network of multiple SIG102 devices over a selectable carrier frequency between 5MHz and 30MHz with 100 kHz spacing. Multiple independent networks may operate over the same powerline by selecting different carrier frequencies for each network. It is recommended to keep at least 1MHz spacing between two carriers (networks).
Two alternate frequencies are pre-defined for fast hoping using FREQ_SEL[1:0] pins when the communication fails on the main frequency. The main operating frequency and two alternative frequencies are set by dedicated registers described in section 3.3.2.

Figure 2 depicts a typical SIG102 network consists of one SIG102 master device which remotely controls sensor and actuators attached to SIG102 slave devices. Also, the master SIG102 device can transfer and receive data to/from a slave SIG102 device attached also to an ECU. Figure 2 demonstrating a single powerline *byte-field* transmission from SIG102 TX device to three SIG102 RX devices coupled through $C_{coupling}$ to the same powerline. Upon detection start bit on SIG102 TX device HDI, a powerline *byte-field* transmission begins. After fix latency of T_{RX_delay}, the powerline *byte-field* is decoded and digitally output on SIG102 RX devices' HDO.

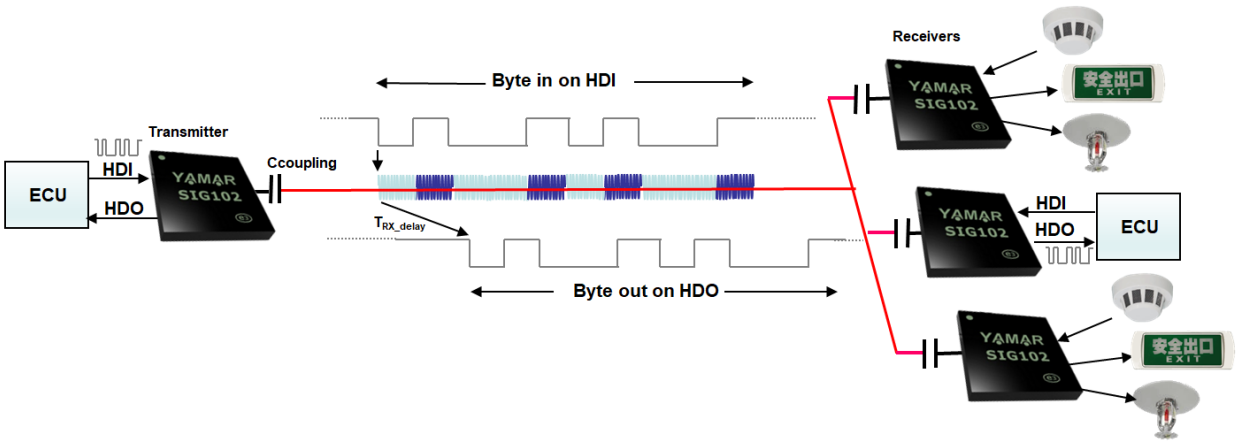


Figure 2 – SIG102 typical network

2.2.1 SIG102 channel parameters

Carrier frequency:	251 selectable frequencies between 5MHz - 30MHz with 100 kHz spacing.
Powerline bitrate:	9.6kbit/s, 10.4bit/s, 19.2Kbit/s, 38.4Kbit/s, 57.6kbit/s, and 115.2kbit/s.
Powerline voltage:	Any, with proper powerline coupling interfacing (see 2.5.8)
Cable length:	Depends on the powerline loads AC signal-attenuation (100m is practicable)
Cable type:	Any cable.

2.3 Device Architecture

Figure 3 depicts the SIG102 blocks.

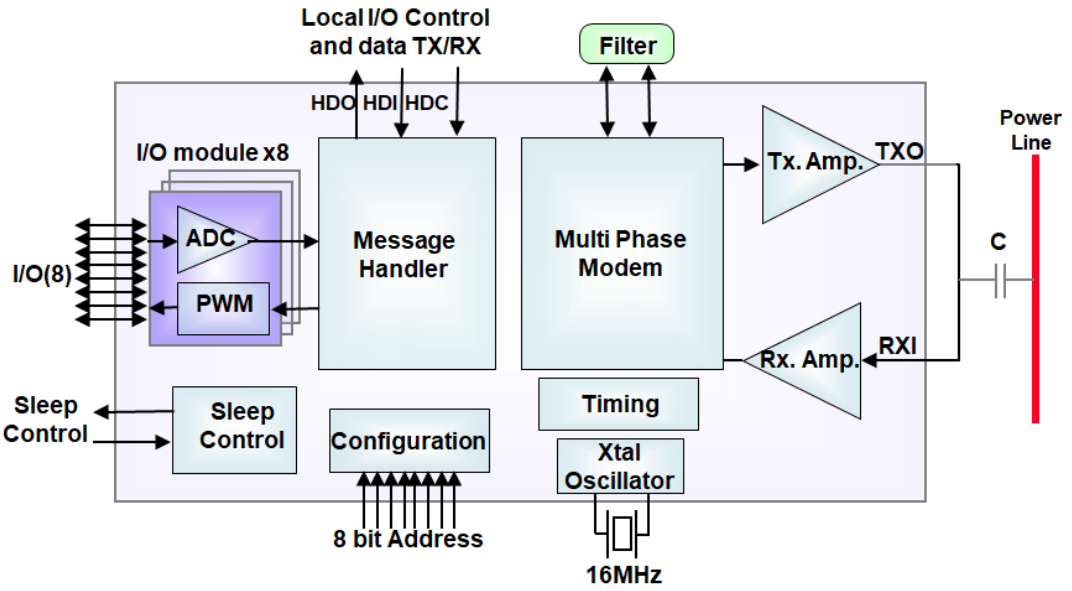


Figure 3- SIG102 Logical Blocks

The SIG102 main building blocks:

- **Message handler** - Interface with UART/LIN ECU.
- **IOs controller** - Control IOs configuration and status.
- **Multi-Phase Modem -** Phase modulates and demodulates the data to and from the DC-BUS powerline.
- **Sleep control** - Ensures low power consumption during Sleep mode.

2.4 Pin configuration and function

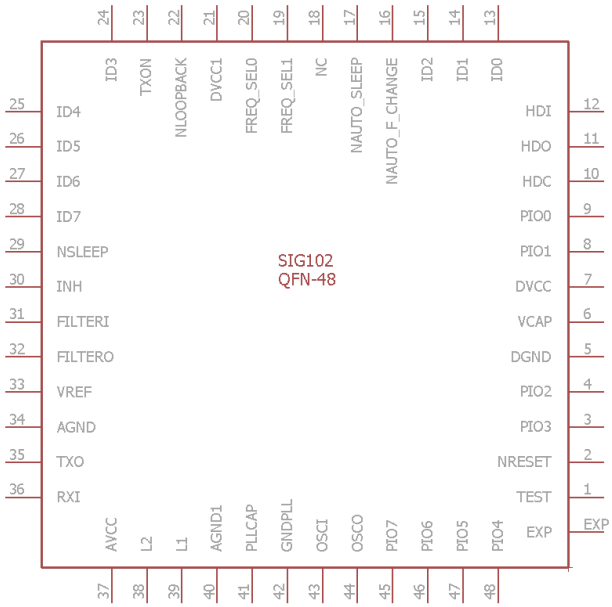


Figure 4 – SIG102 pinout diagram in QFN48 7x7 mm package

2.4.1 Signals and Pinout description

Table 1 - Pinout description

<table>
<tr><th>Name</th><th>Pin #</th><th>Pin type</th><th>Internal PU/PD</th><th>Description</th></tr>
<tr><td>HDO</td><td>11</td><td>Output 12mA</td><td></td><td>Outputs the received data from the powerline or from internal registers to the host.</td></tr>
<tr><td>HDI</td><td>12</td><td>Digital input</td><td>PU</td><td>Transfers data from the host to the powerline or the internal registers.</td></tr>
<tr><td>HDC</td><td>10</td><td>Digital input</td><td>PU</td><td>Host ECU Data / Command input. When low, enables read and write from/to the SIG102 control registers (see section 7.14).</td></tr>
<tr><td>TEST</td><td>1</td><td>Digital Input</td><td>PD</td><td>Should be connected to GND.</td></tr>
<tr><td>NRESET</td><td>2</td><td>Digital Input</td><td>PU</td><td>Reset, active low.</td></tr>
<tr><td>NSLEEP</td><td>29</td><td>Digital Input</td><td></td><td>Sleep mode control input (see section 6.3).
Should be pull-up to 3.3V when not in use.</td></tr>
<tr><td>NAUTO_F _CHANGE</td><td>16</td><td>Digital Input</td><td></td><td>When low, the SIG102 will automatically hop between the main carrier frequency and two alternate frequencies (see 3.3.3).</td></tr>
<tr><td>NAUTO_SLEEP</td><td>17</td><td>Digital Input</td><td></td><td>When low, the SIG102 will automatically enter Sleep mode in case there is no Transmission or reception to/from the powerline for more than AutoSleep-timeout setting (see 6.4).</td></tr>
<tr><td>NC</td><td>11</td><td></td><td></td><td>Should be left floated.</td></tr>
<tr><td>NLOOPBACK</td><td>22</td><td>Digital Input</td><td>PU</td><td>When high, loopback from HDO to HDI is disabled (see 3.3.4)</td></tr>
<tr><td>INH</td><td>30</td><td>Digital Output 8mA</td><td></td><td>When high, SIG102 is in Normal mode
When low, SIG102 is in Sleep mode</td></tr>
<tr><td>FREQ_SEL0</td><td>20</td><td>Digital Input</td><td></td><td rowspan="2">Main and 2 alternate frequencies selection control.
<table><tr><th>FREQ_SEL[1:0]</th><th>Default Frequency [MHz]</th><th></th></tr><tr><td>'00','11'</td><td>13</td><td>Main</td></tr><tr><td>'01'</td><td>5</td><td>Alternate 1</td></tr><tr><td>'10'</td><td>22</td><td>Alternate 2</td></tr></table>see 3.3.2</td></tr>
<tr><td>FREQ_SEL1</td><td>19</td><td>Digital Input</td><td></td></tr>
<tr><td>TXON</td><td>23</td><td>Output 12mA</td><td></td><td>TX_ON output - High when transmission onto the powerline is active.</td></tr>
<tr><td>PIO0</td><td>9</td><td>ADC In/ Digital In/Output PWM 12mA</td><td>PD (digital Input only)</td><td>Device I/O pin 0, default set as digital input.</td></tr>
<tr><td>PIO1</td><td>8</td><td>ADC In/ Digital In /Output 12mA</td><td>PD (digital Input only)</td><td>Device I/O pin 1, default set as digital input.</td></tr>
<tr><td>PIO2</td><td>4</td><td>ADC In/ Digital In/Output PWM 12mA</td><td>PD (digital Input only)</td><td>Device I/O pin 2, default set as digital input.</td></tr>
<tr><td>PIO3</td><td>3</td><td>ADC In/ Digital In/Output PWM 12mA</td><td>PD (digital Input only)</td><td>Device I/O pin 3, default set as digital input.</td></tr>
<tr><td>PIO4</td><td>48</td><td>ADC In/ Digital In/Output PWM 12mA</td><td>PD (digital Input only)</td><td>Device I/O pin 4, default set as digital input.</td></tr>
<tr><td>PIO5</td><td>47</td><td>ADC In/ Digital In/Output PWM 12mA</td><td>PD (digital Input only)</td><td>Device I/O pin 5, default set as digital input.</td></tr>
<tr><td>PIO6</td><td>46</td><td>ADC In/ Digital In/Output PWM 12mA</td><td>PD (digital Input only)</td><td>Device I/O pin 6, default set as digital input.</td></tr>
</table>

<table>
<tr><th>Name</th><th>Pin #</th><th>Pin type</th><th>Internal PU/PD</th><th>Description</th></tr>
<tr><td>PIO7</td><td>45</td><td>ADC In/ Digital In/Output PWM 12mA</td><td>PD (digital Input only)</td><td>Device I/O pin 7, default set as digital input.</td></tr>
<tr><td>ID0</td><td>13</td><td>Digital Input</td><td>PD</td><td>Device address bit [0]</td></tr>
<tr><td>ID1</td><td>14</td><td>Digital Input</td><td>PD</td><td>Device address bit [1]</td></tr>
<tr><td>ID2</td><td>15</td><td>Digital Input</td><td>PD</td><td>Device address bit [2]</td></tr>
<tr><td>ID3</td><td>24</td><td>Digital Input</td><td>PD</td><td>Device address bit [3]</td></tr>
<tr><td>ID4</td><td>25</td><td>Digital Input</td><td>PD</td><td>Device address bit [4]</td></tr>
<tr><td>ID5</td><td>26</td><td>Digital Input</td><td>PD</td><td>Device address bit [5]</td></tr>
<tr><td>ID6</td><td>27</td><td>Digital Input</td><td>PD</td><td>Device address bit [6]</td></tr>
<tr><td>ID7</td><td>28</td><td>Digital Input</td><td>PD</td><td>Device address bit [7]</td></tr>
<tr><td>TXO</td><td>35</td><td>Analog Output Max 66 mA</td><td></td><td>Powerline Transmit signal out
<table>
<tr><th>TXON State</th><th>REG_1[4]</th><th>TX level [V-p-p]</th><th>Impedance [Ω]</th></tr>
<tr><td>High</td><td>'0'</td><td>1</td><td>18 [1]</td></tr>
<tr><td></td><td>'1' (Default)</td><td>2</td><td></td></tr>
<tr><td>Low</td><td></td><td>High Z</td><td>5.3k [2]</td></tr>
</table>
[1]Series output impedance
[2]Input impedance referenced to VREF</td></tr>
<tr><td>RXI</td><td>36</td><td>Analog Input</td><td></td><td>Powerline receive Input</td></tr>
<tr><td>VREF</td><td>33</td><td>Analog Output</td><td></td><td>Analog out reference VCC/2 for filtering capacitor. Place 1uF between VREF to AGND. The VREF is used as a virtual ground for the external analog circuitry.</td></tr>
<tr><td>FILTERI</td><td>31</td><td>Analog, Bi-directional</td><td></td><td>External filter I/O</td></tr>
<tr><td>FILTERO</td><td>32</td><td>Analog, Bi-directional</td><td></td><td>External filter I/O</td></tr>
<tr><td>OSCO</td><td>44</td><td>Analog output</td><td></td><td>16MHz Crystal Output</td></tr>
<tr><td>OSCI</td><td>43</td><td>Analog Input</td><td></td><td>16MHz Crystal Input</td></tr>
<tr><td>L1</td><td>39</td><td>Analog Input</td><td></td><td>External inductor L1 (pin capacitance should be maximal 1pF), see 2.5.4.</td></tr>
<tr><td>L2</td><td>38</td><td>Analog Input</td><td></td><td>External inductors L2 (optional), see 2.5.4.</td></tr>
<tr><td>AVCC</td><td>37</td><td>Power</td><td></td><td>Analog 3.3V supply</td></tr>
<tr><td>AGND</td><td>40,34</td><td>Power</td><td></td><td>Analog ground</td></tr>
<tr><td>VCAP</td><td>6</td><td>Power</td><td></td><td>1.8V core supply output for filtering capacitor. Place 4.7uF between VCAP and DGND.</td></tr>
<tr><td>DGND</td><td>5</td><td>Power</td><td></td><td>Digital Ground</td></tr>
<tr><td>DVCC</td><td>21,7</td><td>Power</td><td></td><td>Digital 3.3V supply</td></tr>
<tr><td>GNDPLL</td><td>42</td><td>Power</td><td></td><td>Analog Ground</td></tr>
<tr><td>PLLCAP</td><td>41</td><td>Power</td><td></td><td>PLL 1.8V output to a filtering capacitor. Place 1uF between PLLCAP and GNDPLL.</td></tr>
<tr><td>EXP</td><td></td><td>Power</td><td></td><td>Expose pad, should be connected to DGND.</td></tr>
</table>

PD – Internal Pull-down resistor 50K ohm +/-%30
PU – Internal Pull-up resistor 50K ohm +/-%30

2.5 Implementation

2.5.1 SIG102 reference schematic

Figure 5 depicts a typical SIG102 schematic.

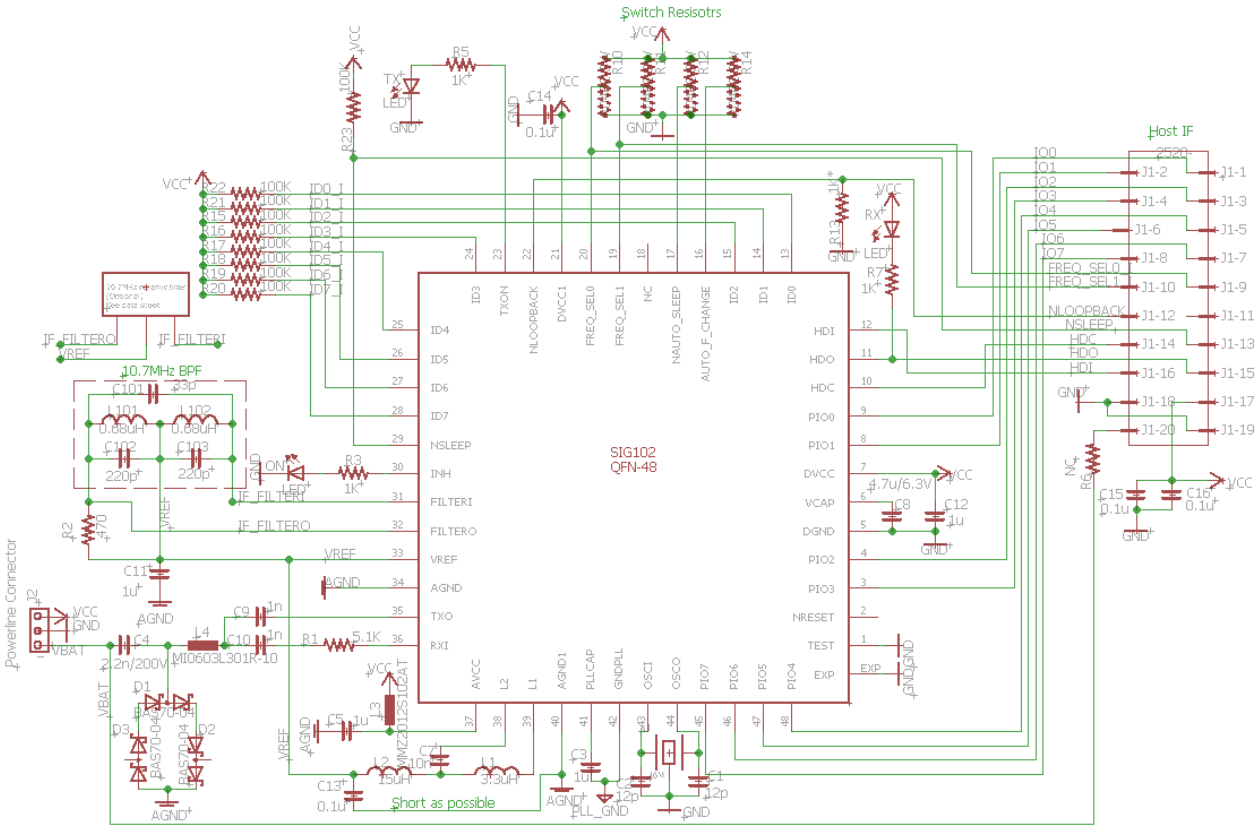


Figure 5 – SIG102 reference schematic

2.5.2 External 10.7MHz filter (BPF)

The SIG102 operates using an external 10.7MHz narrow bandpass filter. The minimum recommended filter bandwidth is 330 kHz @ 3dB. Narrower bandwidth limits the maximal SIG102 bitrate.
Figure 6 depicts the recommended 10.7MHz discrete filter**.**

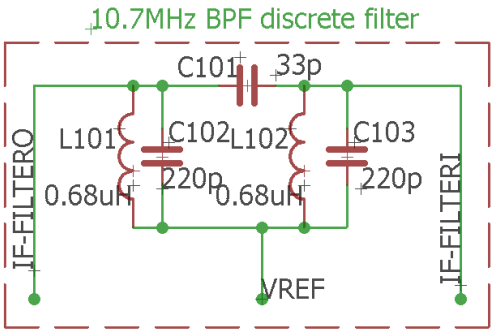


Figure 6- 10.7MHz discrete bandpass filter

Alternatively, Table 2 describes the recommended 10.7MHz ceramic filters.

Table 2 – Recommended 10.7MHz ceramic filters

Manufacturer	Part #	3dB BW [KHz] min.	Insertion loss [dB] max.	Stopband attenuation [kHz]	In/Out imped. [Ω]	Package
AEC	LTCV10.7MA19	350	3.0	950	470	SMD
Strong-First	LTCV10.7MA20	330	3.0	680	330	SMD
Murata	SFECF10M7EA00-R0	330	3.0	700	330	SMD

2.5.3 External Crystal

The device operates with a low cost, small size 16MHz crystal connected between OSCI and OSCO pins. Each of these pins should be connected to the DGND via a load capacitor. The load capacitors values should be determined according to the crystal manufacturer's recommendations and the actual PCB layout. The PCB traces should be as short as possible.
The overall frequency tolerance should not exceed ± 50ppm.
Recommended crystals:

- **NDK - NX2520SA-16MHz, SMD, 2.5x2 mm**
- **NDK - NX3225SA/GB-16MHz, SMD, 3.2x2.5mm**
- **NDK - NX2016GC-16MHz, SMD, 2.0x1.6mm**
- **ECS - ECS-160-12-37B-CTN-TR, SMD, 2.0x1.6mm**

2.5.3.1 16MHz clock from an external source

The device can operate from an external 16HMz clock that meets the requirements above.
Figure 7 depicts an external 16MHz clock connection to the device.

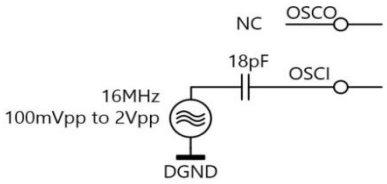


Figure 7 - External 16MHz clock connection

2.5.4 L1 and L2 inductors

The SIG102 requires one or two inductors for its operation, depending on the desired operating frequency.

- For full in-band operation, 5MHz - 30MHz:
  - L1 - 3.3uH
  - L2 - 15uH with 10nF series capacitor between L2 pin and L2 inductor.

- For low in-band operation, 5MHz -12MHz:
  - L1 - 18uH
  - L2 - NC

- For high in-band operation, 12MHz - 30MHz:
  - L1 - 3.3uH
  - L2 - NC

Figure 8 depicts the in-band operation inductors' connection to pins L1 and L2.

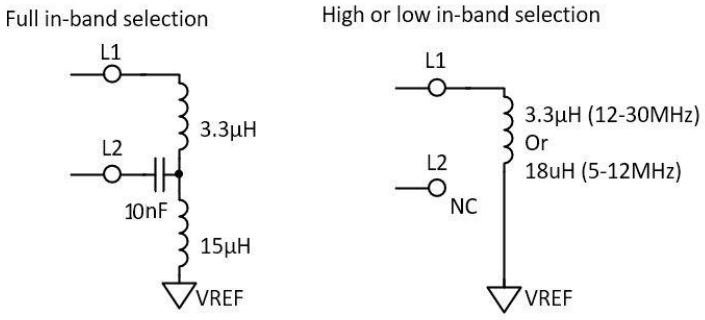


Figure 8 - L1 and L2 inductors connections

2.5.4.1 Recommended L1 & L2 inductors

Table 3 describes the recommended L1 and L2 inductors.

Table 3 - Recommended L1 and L2 manufacturers

Inductor	ABRACON	VISHAY	TDK
L1=3.3uH	815-AIML-0805-3R3K-T	ILSB0805ER3R3K	NL453232T-3R3J-PF
L2=15uH	815-AIML-0805-150K-T	ILSB0805ER150K	NL453232T-150J-PF
L1=18uH	815-AIML-0805-180K-T	ILSB0805ER180K	NL453232T-180J-PF

2.5.5 Optional EMC chip-bead (L4)

For enhanced mitigation of high harmonics above 30MHz conducted over the powerline, it is recommended to add L4 in series to the coupling capacitor C4 (see Figure 5).

Table 4 describes the recommended EMC chip-beads.

Table 4 - Recommended L4 (optional)

LAIRD	MI0603L301R-10
LAIRD	HZ0603A222R-10
TDK	MMZ1608Q

2.5.6 Ceramic capacitors

Low ESR capacitors will provide better performance. X5R and X7R capacitors are recommended, especially for VCAP (C8) and PLLCAP (C3).

2.5.7 TXO output level and drive control

The TXO pin output level and drive capability to the powerline are controlled by REG_*1[4]*, as described in Table 5.

Table 5 - TXO signal level

TXON State	REG_1[4]	TX level [V-p-p]
High	'0'	1
	'1' (Default)	2
Low (Rx)		High Z

Set the TXO output drive capability by configuring REG_*1[7]*, as described in Table 6.

Table 6- TXO output drive control

TXON State	REG_1[7]	Output drive [A]	Impedance [Ω]
High	'0' (Default)	33mA	18 [1]
	'1'	66mA	
Low (Rx)		Disabled	5.3k [2]

[1]Series output impedance

[2]Input impedance referenced to VREF

2.5.8 Powerline coupling interface

The SIG102 is coupled to the powerline through a single small footprint DC blocking ceramic capacitor, typically 2.2nF. The $C_{coupling}$ voltage rating depends on the powerline voltage and its expected impulses.
For high voltage powerline applications (e.g. battery monitoring system in EV or solar panels), it is required to add galvanic isolation.

2.5.9 External protection network

A simple external diode protection network is recommended before the $C_{coupling}$, to protect against high powerline pulses (above 2 V-P-P). The protection network consists of three low capacitance (< 10pF) fast Schottky diodes serially connected in both polarities (e.g. BAS70-04).

2.5.10 Recommended connection to power-supply

Power-supplies have filtering capacitors in their DC inputs. These capacitors attenuate strongly the SIG102 carrier signal. It is recommended to add an inductor (>22uH) or ferrite bead (>100Ω @ 5MHz-30MHz) in series to the power supply connection to the DC powerline to reduce the carrier signal attenuation.
Figure 9 depicts a typical SIG102 connection to a DC powerline and its 3.3V power supply.

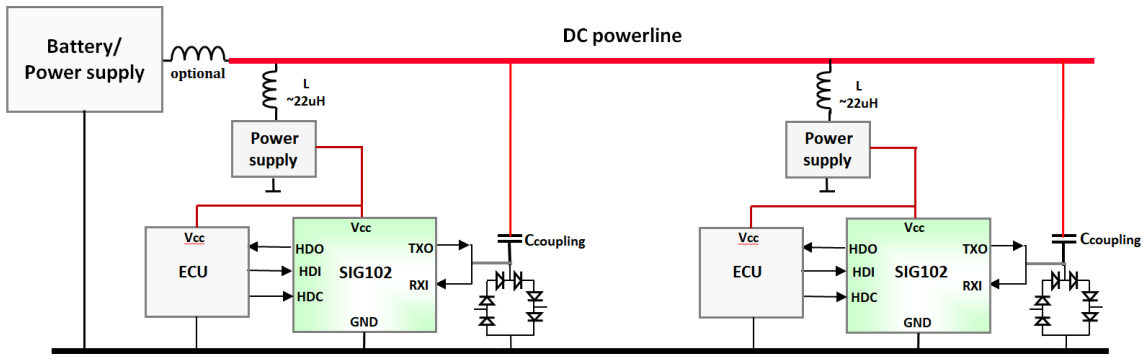


Figure 9 – SIG102 connection to 3.3V power-supply and powerline

3 Operation

3.1 Interfacing to UART/LIN ECU

The SIG102 interfaces directly to any uC UART/LIN I/O pins (3.3V logic).
The UART/LIN communication protocol uses four pins as described in Table 7.

Table 7 – UART/LIN interface pins

SIG102	ECU	Description
HDI	**Tx**	Data Input from the host ECU.
HDC	**GPO**	Data/Command select input. When pulled down, the SIG102 enters command mode, enabling access to SIG102 internal registers.
HDO	**Rx**	Data output to the host ECU.
NLOOPBACK	**GPO**	Enable loopback of HDI to HDO pin. - When interfacing a UART port, ECU may disable/enable the loopback option. - When interfacing a LIN ECU, tie pin to GND. HDI loops back to HDO.

Figure 10 depicts a typical SIG102 to UART/LIN ECU interface connection.

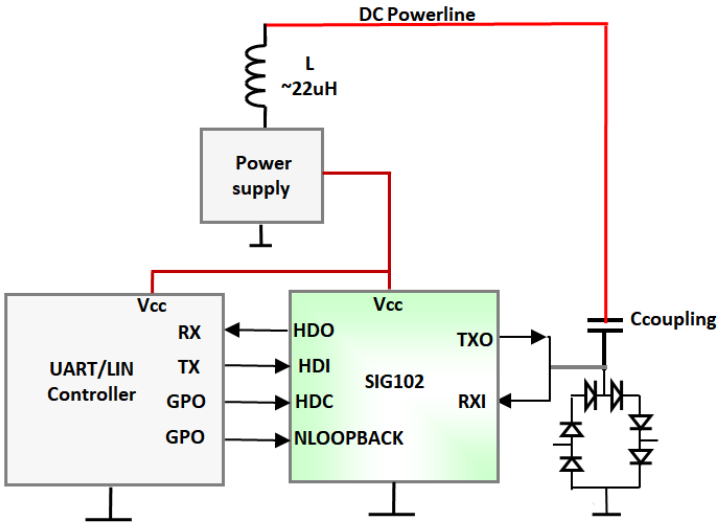


Figure 10 - Typical SIG102 to UART ECU interface

3.2 SIG102 messages

3.2.1 Message structure

The SIG102 message structure contains the following:

- A *byte-field (UART byte)* is defined with one start bit, 8 data bits, and one stop bit.
- A *PLC-byte* is defined as the signaling pattern of the *byte-field* over the powerline.
- A *break-field* is defined as one start bit, 12 to 30 zero bits, and one stop bit.
- A *PLC-break* is defined as the signaling pattern of the *break-field* over the powerline

The SIG102 is a byte-oriented powerline transceiver. Each UART/LIN *byte-field* on the HDI pin is encoded into a modulated powerline *PLC-byte* at the length of the ECU UART bitrate. At the receiving side, each *PLC-byte* is decoded back after a fixed delay of ~2.5T_{bit} to the HDO *byte-field*. A *break-field* at the beginning of a message is handled the same.

3.2.2 Transmit flow

Upon detection of a start bit on HDI, the SIG102 starts its *byte-field*/*break-field* transmission over the powerline until receiving a stop bit from ECU. In case of ECU transfers bytes continuously (i.e. inter-byte spacing between bytes < 1/3 T_{bit}), the SIG102 will not stop its transmission. If the inter-byte space is longer than 1/3 T_{bit}, the SIG102 will stop its transmission over the powerline and will wait for the next start bit.

3.2.3 Receive flow

Upon detection of a powerline *PLC-byte/PLC-break*, the SIG102 will decode the *PLC-byte* and transfer the *byte-field* to the receiving ECU's HDO pin (a start bit followed by the data bits and stop bit).

The delay (i.e. powerline latency) between Transmitter start bit drop on HDI to Receiver start bit drop is T_{RX_delay} = ~2.5 T_{bit}.

Figure 11 depicts a single *byte-field -> PLC-byte -> byte-field* TX-RX flow. ECU A transfers 0x55 *byte-field* on HDI with local loopback feedback on HDO (loopback is enabled). Upon start bit detection, a powerline transmission of *PLC-byte* 0x55 (length of 10 x T_{bit}), begins. Then, after T_{RX_delay} of ~2.5 T_{bit}, the *PLC-byte* is extracted on RX device B HDO pin to its ECU.

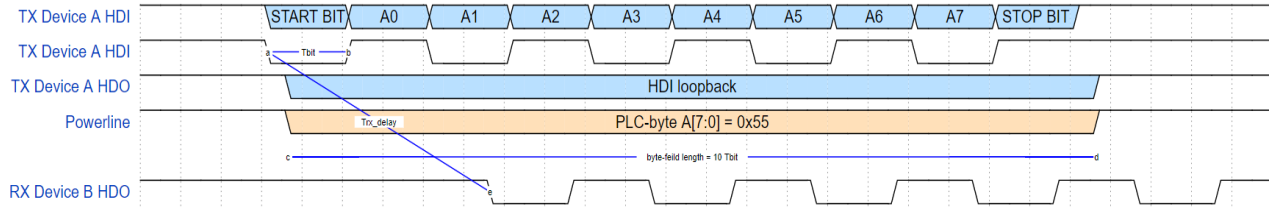


Figure 11 – SIG102 single *PLC-byte* TX-RX example

Figure 12 depicts a single *break-field* TX-RX flow. ECU transfers a *break-field* on HDI with local loopback feedback on HDO (loopback is enabled). Upon start bit detection, a powerline transmission of *PLC-break* (length of 13 x T_{bit}), begins. Then, after T_{RX_delay} of ~2.5 T_{bit}, the *break-field* is extracted on RX device B HDO to its ECU.

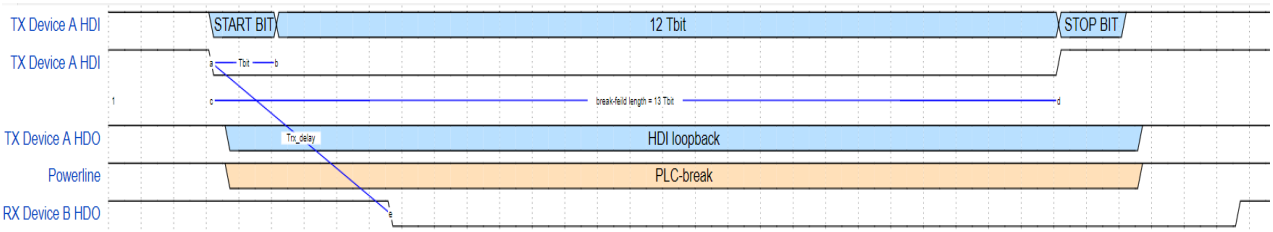


Figure 12 – SIG102 single *break-field* TX-RX example

3.3 Device configuration

3.3.1 Bitrate configuration

Table 8 describes the SIG102 supported bitrate selection.
Bitrate configuration is made by setting REG_0[2:0] bits using the *WRITE-REG* command (see 7.14).

Table 8 – Bitrate selection

REG_0 Bitrate_sel[2:0]	Bitrate [bit/s]	T_{bit} [µs]
000	9600	104
001	10417	96
010	19200 **(default)**	52
011	38400	26
100	57600	17.36
101	115200	8.68

3.3.2 Carrier frequency management

The SIG102 operates on its configured main frequency. Two alternate frequencies (ALT1 and ALT2) are available for frequency hopping in case that the operating frequency is blocked by interference.
The active working frequency is determined by FREQ_SEL[1:0] hardware pins setting. For each change in FREQ_SEL[1:0] pins, the SIG102 will switch to the selected carrier frequency (Main/ALT1/ALT2) according to Table 9 mapping.
Set the Main/ALT1/ALT2 frequencies by configuring REG_2/ REG_3/ REG_4 respectively (see 7).

For each configuration of REG_2, the active frequency is automatically switched to the Main frequency (as set in REG_2), regardless of FREQ_SEL[1:0] pins set. Switching to ALT1/ALT2 again will take place only at the next change of FREQ_SEL[1:0] pins.
ECU may read the active operating carrier frequency value stored in read-only REG_5.
Table 9 describes the carrier frequency setting and control.

Table 9 – Carrier frequency setting and control

Carrier Frequency	FREQ_SEL[1:0]	Register name	Default Frequency [MHz]
Main	'00','11'	REG_2[7:0]	13
ALT1	'01'	REG_3[7:0]	5
ALT2	'10'	REG_4[7:0]	22

3.3.2.1 Carrier frequency configuration

ECU can define carrier frequency from 5MHz to 30MHz with a spacing of 100 kHz (Total of 251 selectable carriers). Upon completion of configuration or change of FREQ_SEL[1:0] pins, the SIG102 will update its operating carrier frequency within a 1msec period. During this period, the SIG102 is kept in *Soft-Reset* and will not communicate with its ECU nor detect new messages from the powerline and no other internal register configuration is allowed. It is recommended to place the carrier frequency configuration last during multiple registers configuration and wait at least 1ms after HDC is released.

When multiple SIG102 networks operate over a single powerline, it is recommended to select their carrier frequencies spaced more than 1MHz between each other.

The carrier-selected value is calculated as given in the Definition of equation (1).

Definition of equation

REG_2/3/4 = (Carrier Freq. [MHz] - 5) * 10 **(1)**

EXAMPLE 1

- When setting the frequency to 14.1MHz:
  REG_2/3/4 = (14.1 - 5) * 10 = **0x5B**

EXAMPLE 2

- When Setting to 5MHz:
  REG_2/3/4 = (5 - 5) * 10 = **0x00**

3.3.3 Auto frequency change mode

The Auto frequency change mode is enabled either by pull the NAUTO_F_CHANGE pin low or by clearing REG_0[3] bit. The last action prevails.
When enabled, the SIG102 automatically hops between Main, ALT1, or ALT2 configured frequencies when no powerline *PLC-byte* activity detected more than 1 sec. It indicates that neither transmission nor reception is detected over the powerline.

The hopping method is as follows:

Main ---> ALT1 ---> Main ---> ALT2 ---> Main …

3.3.4 Loopback

LOOPBACK between HDI and HDO is required when interfacing to a LIN ECU. Loopback has to be disabled when interfacing with a LIN transceiver (see 3.1).
Loopback is enabled either by pull the LOOPBACK pin low or by clearing *REG_0[5]*. The last action prevails.

3.3.5 Remote loopback mode

The remote loopback function, when enabled, triggers the receiving SIG102 to transmit-back its last received powerline *PLC-byte* over the powerline. This function is useful in point to point communication between two SIG102 devices as part of the ECU built-in ACK/NACK mechanism. For example, the checksum byte at the end of a message is returned to the transmitting Master to validate the integrity of the received message by the Slave.

Remote loopback mode is enabled by setting *REG_0[4]*. The SIG102 RX device will respond only when the powerline is idle for at least 3 x T_{bit} times after full reception of the last byte.

Figure 13 depicts an example of a remote loopback operation. ECU A transfers two data bytes [0x00][0x01] that are transmitted over the powerline to ECU B. Upon detecting the last transmitted 0x01 byte, SIG102 device B waits for 3 x T_{bit} time before automatically transmit-back 0x01 over the powerline to device A.

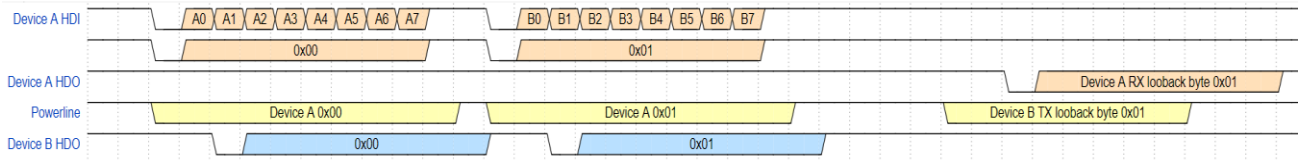


Figure 13 – Remote loopback example

3.3.6 SIG102 UUID

Each SIG102 device is hard-coded with a 48 bit universally unique identifier (UUID[47:0]).
The UUID is stored in REG_37 to REG_3C and can be retrieved using the READ-REG commands (see 7.8 to 7.13 7.13).

3.3.7 Typical set-up and operation example

1. Interface HDI, HDO, and HDC pins to the host ECU.
2. Enable/disable loopback of HDI pin to HDO pin (see 3.3.4).
3. Select SIG102 bitrate according to ECU UART/LIN bitrate (see3.3).
4. Select a carrier frequency (default 13MHz) (see 3.3.2).
5. Transmit bytes via HDI pin to the powerline.
6. Receive bytes from the powerline via HDO pin.

4 SIG102 I/O Pins Description

The SIG102 has eight configurable I/O pins that can be configured individually to either digital Input (default) /digital output /analog input/ PWM output.

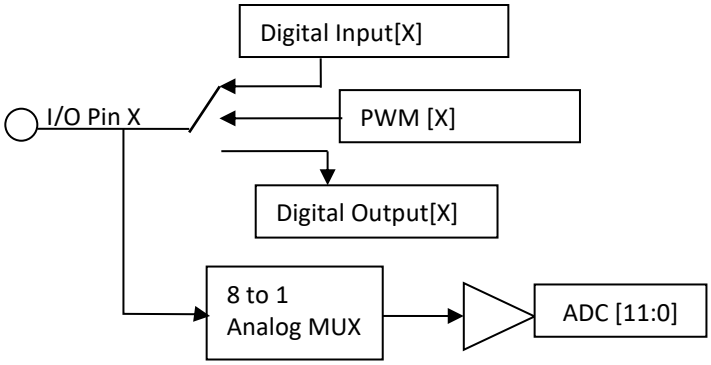


Figure 14 – I/O pins Block diagram

4.1 I/O Pins Configuration

Each I/O can be configured to be either Digital Input / Output, ADC Input, or PWM output.
All I/Os is default configured as Digital Inputs, with internal pull-down.

4.1.1 REG_21 – ' I/O Direction' (Address 0x21)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W [1]	R/W [1]	R/W [1]	R/W [1]	R/W [1]	R/W [1]	R/W [1]	R/W [1]
IO 7 direction	IO 6 direction	IO 5 direction	IO 4 direction	IO 3 direction	IO 2 direction	IO 1 direction	IO 0 direction

Bit [7:0] - IO direction control.

'1' set IO as an Input pin
'0' set IO as an output pin.
Default all IO set as Input pins.

4.1.2 REG_22 – ' I/O Functionality' (Address 0x22)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]
IO 7 function	IO 6 function	IO 5 function	IO 4 function	IO 3 function	IO 2 function	IO 1 function	IO 0 function

Bit [7:0] - IO Functionally control.
'1' set IO as Analog or PWM pin
'0' set IO as a digital pin.
Default all IO set as digital pins.

I/O Pin	7	6	5	4	3	2	1	0
Configuration	Digital Input	ADC Input	Digital Input	Digital Input	Digital Output	Digital Output	PWM Output	PWM Output

For example, writing '0xF0' and '0x43' to REG_21 and REG_22 respectively, configures the I/Os the following way:

4.1.3 REG_23 – 'IO Watchdog Control' (Address 0x23)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R	R	R	R	R	R/W [0]	R/W [0]	R/W [0]
Reserved	Reserved	Reserved	Reserved	Reserved	IO Watchdog timer[2:0]		

Bit[2:0] - Set the IO Watchdog timer duration in seconds. If the Watchdog timer is enabled, the SIG102 will power down its outputs if it didn't receive any data from the powerline nor from its host (if connected) for the defined period. Default this feature is disabled.
Bit[7:3] -Reserved.
R - Readable bit, W - Writeable bit [x] - Value on power-up. '1' - bit is set; '0' - bit is cleared

4.2 Digital IO

The SIG102 eight IOs can be set as digital input or outputs (CMOS 3.3V).
Setting or reading digital IOs is made through REG_24.

4.2.1 REG_24 – 'Digital IO' (Address 0x24)

The 'Digital IO' register write operation sets the IO configured as digital output correspondingly.
The 'Digital IO' register read operation responds with the current state of the IO (if configured as digital input or output (latch)).

*** Note - For IO that is configured as analog or PWM, the read value will always return '0'.*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]
IO 7	IO 6	IO 5	IO 4	IO 3	IO 2	IO 1	IO 0

Bit[7:0] – Set value for IO X as output, Read value of IO X as digital input or Output (latch).

EXAMPLE 3
Preform WRITE-REG to REG_24 with the value of 0x55 results in IO 3 output logical '0' and IO 2 output logical '1'.
By default all digital inputs are PD. Assume IO 7 is externally PU.
Preform READ-REG to REG_24, the SIG102 responds with byte 0x84.

I/O Pin	7	6	5	4	3	2	1	0
Configuration	Digital Input	ADC Input	Digital Input	Digital Input	Digital Output	Digital Output	PWM Output	PWM Output
REG_24 WRITE VALUE	0	1	0	1	0	1	0	1
REG_24 READ VALUE	1	0	0	0	0	1	Always '0'	Always '0'

4.3 PWM Outputs

The SIG102 IOs can be set up to eight PWM channels with an 8 bits resolution.
All the PWM channels share the same selectable PWM frequency, between 31.37 kHz (~32uS PWM cycle) down to 122.5Hz (~8ms PWM cycle).
For each channel, the time that the PWM output is high during a PWM cycle (duty cycle) is configured using the PWM_DUTY_X register, where X is the PWM channel number. In addition, an 8-bit resolution referenced delay period can also be configured using PWM_DELAY_X to delay the start of the duty cycle from the beginning of the PWM cycle.
When using multiple PWM channels, it is recommended to add a delay between the PWM channels to moderate the overall peak current consumption of all active PWM channels.

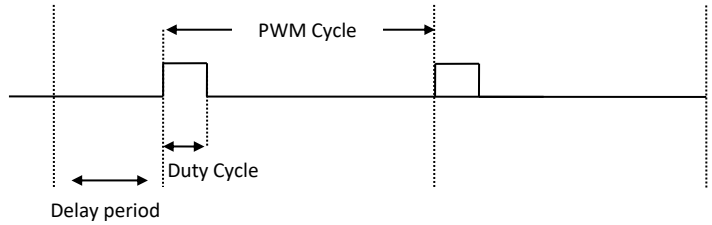


Figure 15- PWM Diagram

4.3.1 REG_20 - PWM Frequency (Address 0x20)

Set the PWM frequency divider for all 8 optional PWM IOs.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]
PWM frequency divider							

Bit [7:0] - PWM frequency divider.

The PWM frequency value is calculated as given in Definition of Equation **(**2)
Equation 2

$$\textbf{PWM frequency [KHz] = 31.37kHz / (PWM frequency divider[7:0] + 1)} \quad \textbf{(2)}$$

The Max PWM Frequency is 31.37 kHz (/PWM frequency divider == 0x00)
The Min PWM Frequency is 122.5Hz (/PWM frequency divider == 0xFF)

4.3.2 REG_10 to REG_17 - PWM Delay_X (Address 0x10 to address 0x17)

Set the PWM delay for all 8 optional PWM IOs.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]
PWM_Delay_X							

Bit [7:0] - PWM delay_X.

By default, all the PWM channels are synchronized. The delay period enables the user to differentiate each pin output period.

The PWM delay value is calculated as given in Definition of Equation **(**3)

Equation 3

PWM delay [sec] = (1 / PWM frequency[Hz]) * (PWM_Delay[7:0] / 255) (3)

4.3.1 REG_18 to REG_1F - PWM DUTY_CYCLE_X (Address 0x18 to address 0x1F)

Set the PWM duty cycle for all 8 optional PWM IOs.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]
PWM_Duty_Cycle_X							

Bit [7:0] - PWM Duty_CYCLE_X.

The PWM Duty cycle value is calculated as given in Definition of Equation **(**4)

Equation 4

PWM duty cycle [sec] =(1 / PWM frequency[Hz]) * (PWM_Duty_Cycle[7:0] / 255) (4)

The following steps are required to configure a PWM channel:

- ✓ Set the PWM frequency in the PWM Frequency register.
- ✓ Set the PWM duty cycle in the PWM_DUTY_X register.
- ✓ Set the PWM delay in the PWM_DELAY_X register.
- ✓ Set the desire I/Os as PWM output (see REG_21 and REG_22).

4.4 Analog to Digital Converter (ADC)

The ADC module allows converting up to eight analog inputs into 12 bits of binary data. Each one of the SIG102 I/Os can be configured as analog input. All the analog inputs are internally mux into one ADC module.
The maximal sampling rate is 50 kSps.
The allowed ADC input signal is between 0 to 3.3V, this gives a maximum resolution of ~0.805mV per bit.
To guarantee a conversion error of less than that 0.5LSB, the source impedance at the input pin (R_{source}) may not exceed 45 kOhm.

4.4.1 REG_25 to REG_34 – ADC_X_H and ADC_X_L (Address 0x25 to 0x34)

Each channel 12 bits conversion result is stored in 2 registers, ADC_X_L and ADC_X_H, whereas the X represents the channel (IO) number between 0 to 7.

ADC_H_X

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]
ADC_H_X – ADC Conversion[11:4]							

Bit [7:0] - ADC MSB conversion results bit[11:4].

ADC_L_X

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W [0]	R/W [0]	R/W [0]	R/W [0]	R	R	R	R
ADC_L_X – ADC Conversion[3:0]				Reserved			

Bit [3:0] - Reserved.
Bit [7:4] - ADC LSB conversion results bit[3:0].

EXAMPLE 4

The conversion result is 0x20 followed by 0x43;
ADC_X_L = 0x20;
ADC_X_H = 0x43;
Calculation of the conversion result will be:
(ADC_X_H * 16) + (ADC_X_L / 16) = 0x43 *16 + 0x20 /16 = 1072 +2 = 1074= (1074/4096) * 3.3V = 0.865V.

4.4.2 ADC Write and Read operation

An ADC conversion starts by performing the WRITE-REG command (locally or remotely, see 5.2) to the ADC_L_X ADC_H_X registers. When the conversion is completed, the results are stored in the corresponding ADC register.
Users can retrieve the last ADC conversion by sending a READ-REG command to a specific ADC channel address.
When reading from the ADC_X_H address, the SIG102 replies with a single byte of higher nibble conversion result (ADC conversion[11:4]).
When reading from ADC_X_L, the SIG102 replies with the full word conversion result (2 bytes, ADC_L_X followed by ADC_H_X).

** *Note - Reading for inactive ADC channel address will result in no response message from the SIG102 device.*

4.4.2.1 REG_35 - WRITE/READ ADC ALL (Address 0x35)

To simplify ADC write and read operation, the WRITE/READ ADC ALL register allows users to activate a sequentially analog conversion from all active ADC channels and reply with all conversion results within one message. By performing the WRITE-REG command to REG_35, a sequentially analog conversion from each one of the active ADC pin is being made. By performing the READ-REG command, the SIG102 returns with 2 bytes conversion results per active analog IOs, starting from low IO index to high IO index (Maximal 2 X 8 = 16 bytes).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]
WRITE-READ-ADC-ALL							

EXAMPLE 5
SIG102 IOs 0, 3, and 7 are configured as analog inputs. To enable a sequentially ADC conversion of ADC channel 0, 3, and 7, a **WRITE-REG to 'ADC Read/Write All'** register is performed (The write data byte is ignored).
Upon receiving the WRITE-REG command, the SIG102 will start an ADC conversion starting from channel ADC 0 and ending at channel ADC 7.
Then, perform a READ-REG command from the **'ADC Read/Write All'** register.
The SIG102 response with ADC0, ADC3 and ADC7 conversion results: 0x60, 0x35, 0x10, 0x00, 0xF0, and 0x1F (for instance) as follows:

1st byte	**2nd byte**	**3rd byte**	**4th byte**	**5th byte**	**6th byte**
0x60	0x35	0x10	0x00	0xF0	0x1F
IO 0 ADC_L	IO 0 ADC_H	IO 3 ADC_L	IO 3 ADC_H	IO 7 ADC_L	IO 7 ADC_H
ADC0 - 0x356 = 0.68V		ADC3 - 0x001 = 0.805mV		ADC7 - 0x1FF = 0.411V	

5 SIG102 I/Os settings and control

Setting and controlling each IO is made by WRITE-REG and READ-REG operations from/to the IO control registers, either locally using the command mode (HDC pin required), or remotely over the powerline from a SIG102 Master device using dedicated PLC commands (see 5.2).
Table 10 described the IO control registers summary.

Table 10 - IO Control register summary

Register Address	**R/W**	**Register name**	**Function**
0x10	r/w	*PWM_delay_0*	PWM IO 0 delay period configuration
0x11	r/w	*PWM_delay_1*	PWM IO 1 delay period configuration
0x12	r/w	*PWM_delay_2*	PWM IO 2 delay period configuration
0x13	r/w	*PWM_delay_3*	PWM IO 3 delay period configuration
0x14	r/w	*PWM_delay_4*	PWM IO 4 delay period configuration
0x15	r/w	*PWM_delay_5*	PWM IO 5 delay period configuration
0x16	r/w	*PWM_delay_6*	PWM IO 6 delay period configuration
0x17	r/w	*PWM_delay_7*	PWM IO 7 delay period configuration
0x18	r/w	*PWM_duty_0*	PWM IO 0 duty cycle configuration
0x19	r/w	*PWM_duty_1*	PWM IO 1 duty cycle configuration
0x1A	r/w	*PWM_duty_2*	PWM IO 2 duty cycle configuration
0x1B	r/w	*PWM_duty_3*	PWM IO 3 duty cycle configuration

0x1C	r/w	*PWM_duty_4*	PWM IO 4 duty cycle configuration
0x1D	r/w	*PWM_duty_5*	PWM IO 5 duty cycle configuration
0x1E	r/w	*PWM_duty_6*	PWM IO 6 duty cycle configuration
0x1F	r/w	*PWM_duty_7*	PWM IO 7 duty cycle configuration
0x20	r/w	*PWM frequency*	PWM frequency configuration
0x21	r/w	*I/O Configure 1*	Configure I/O[7:0] as Inputs ('1') Or Outputs ('0')
0x22	r/w	*I/O Configure 2*	Configure I/O[7:0] functionality as digital ('0') or PWM / ADC ('1')
0x23	r/w	*IO Watchdog*	WatchDog module control
0x24	r/w	*Digital I/Os*	Write to this register will update the digital outputs I/Os status correspondingly. Read from this register will feedback the status of the digital inputs I/Os and output I/Os (latch).
0x25	r/w	*ADC0_H*	Read command returns the last measured ADC0 higher nibble value (1 byte). Write command enables new ADC conversion on IO 0
0x26	r/w	*ADC0_L*	Read command returns the measured ADC0 word value (2 bytes). Write command enables new ADC conversion on IO 1
0x27	r/w	*ADC1_H*	Read command returns the measured ADC1 higher nibble value (1 byte). Write command start new ADC conversion on IO 1
0x28	r/w	*ADC1_L*	Read command returns the measured ADC1 word value (2 bytes). Write command enables new ADC conversion on IO 1
0x29	r/w	*ADC2_H*	Read command returns the measured ADC2 higher nibble value (1 byte). Write command start new ADC conversion on IO 2
0x2A	r/w	*ADC2_L*	Read command returns the measured ADC2 word value (2 bytes). Write command enables new ADC conversion on IO 2
0x2B	r/w	*ADC3_H*	Read command returns the measured ADC3 higher nibble value (1 byte). Write command start new ADC conversion on IO 3
0x2C	r/w	*ADC3_L*	Read command returns the measured ADC3 word value (2 bytes). Write command enables new ADC conversion on IO 3
0x2D	r/w	*ADC4_H*	Read command returns the measured ADC4 higher nibble value (1 byte). Write command start new ADC conversion on IO 4
0x2E	r/w	*ADC4_L*	Read command returns the measured ADC4 word value (2 bytes). Write command enables new ADC conversion on IO 4
0x2F	r/w	*ADC5_H*	Read command returns the measured ADC5 higher nibble value (1 byte). Write command start new ADC conversion on IO 5
0x30	r/w	*ADC5_L*	Read command returns the measured ADC5 word value (2 bytes). Write command enables new ADC conversion on IO 5
0x31	r/w	*ADC6_H*	Read command returns the measured ADC6 higher nibble value (1 byte). Write command start new ADC conversion on IO 6
0x32	r/w	*ADC6_L*	Read command returns the measured ADC6 word value (2 bytes). Write command enables new ADC conversion on IO 6
0x33	r/w	*ADC7_H*	Read command returns the measured ADC7 higher nibble value (1 byte). Write command start new ADC conversion on IO 7
0x34	r/w	*ADC7_L*	Read command returns the measured ADC7 word value (2 bytes). Write command enables new ADC conversion on IO 7
0x35	r/w	*ADC Read/Write All*	Read command returns the measurements of all active ADC IOs sequentially. Write command enables new ADC conversion for all active ADC IOs (See 4.4.2.1).
0x36	r/w	*Slave Device ID*	SIG102 Slave Address – Set the SIG102 Slave ID from 0x00 to 0xFE. 0xFF ID is preserved as broadcast global ID (see 5.2.1.2).

5.1 I/Os local control

Accessing to each one of the IO control registers is done locally by ECU interfacing the HDI, HDO, and HDC pins, and performing WRITE-REG and READ-REG commands (see 7.14).

5.2 I/Os Remote slaves control (Commands over powerline)

A SIG102 IOs can be controlled remotely over the powerline by a set of commands transmitted from a SIG102 master (attached to a host ECU).

Table 11 describes the PLC SIG102 commands summary.

Table 11 – PLC SIG102 commands summary

Command name	Command Identifier	Description
PLC WRITE-REG	0xFB	Write to the SIG102 internal registers.
PLC READ-REG	0xBA	Read from the SIG102 internal registers.
PLC SLEEP	0x3C	Put the remote slaves in Sleep mode.
PLC CHANGE FREQUENCY MAIN	0xB4	Change the remote slave frequency channel to the Main frequency.
PLC CHANGE FREQUENCY ALT1	0xB1	Change the remote slave frequency channel to ALT1 frequency.
PLC CHANGE FREQUENCY ALT2	0x32	Change the remote slave frequency channel to ALT2 frequency.

5.2.1 PLC command structure

The PLC command is as follows:

Break Field	Sync Field	Identifier	SIG102 Slave ID	DATA bytes	Checksum

- **Break Field -** Break field length is at least 13-bit times.
- **Sync Field -** '0x55' byte.
- **Identifier byte -** The specific command byte.
- **SIG102 Slave ID -** SIG102 ID byte. **0xFF is the global ID**.
- **Data bytes -** Includes the bytes according to selectable command.

5.2.1.1 Checksum calculations

The checksum is an inverted 8-bit sum of the Identifier and Data byte including (own) carry as given in Definition of Equation (5)

Equation 5

$$\textbf{Checksum = ~ (Identifier Byte + SIG102 Slave ID+ Data bytes + Carry)} \quad (5)$$

5.2.1.2 SIG102 ID

The SIG102 ID range is from 0x00 to 0xFE.
ID 0xFF is preserved as the global ID. Using the global ID allows the user to send broadcast SIG102 commands over the powerline. All commands will be executed by all active SIG102 salves. A read command with a global ID will not be responded.

The SIG102 ID is set either by setting HW pins ID0 to ID7 or by the configuration of REG_36. The last action prevails.
Upon power-up/hard-reset event, SIG102 ID is set according to HW pins state and remains until the next change on pin ID0 to ID7 or REG_36 configuration.

5.2.1.2.1 REG_36 – SIG102 ID (Address 0x36)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]
SIG102 ID							

Bit [7:0] - SIG102 ID.

5.2.2 PLC Commands description

5.2.2.1 PLC READ-REG command

This command reads the data from the internal registers of the remoted SIG102 slave.

The format of the command to the SIG102 slave:

Break field	Sync Byte	Identifier Byte	SIG102 Slave ID	Reg. Address

- **Break** field **-** Hold the Data in line at low for a duration of 13 to 31 bits
- **Sync Byte -** send a 0x55 byte.
- **Identifier Byte - 0xBA** for the read command.
- **SIG102 Slave ID -** The ID of the remote SIG102 slave we would like to read from. In the case of **Global ID, 0xFF** is transmitted, the SIG102 will not send a reply message.
- **Reg Add -** The internal SIG102 register address to read from.

Upon receiving the Read register command from the master, the SIG102 response with the internal register value followed by a checksum byte.

The format of Read-Register command Response to the Master -

Data	Checksum

Data - Internal register value.

- Reading from 'ADC_H_X' responds with the conversion results MSB[11:3].
- Reading from 'ADC _L_X' responds with 'ADC_L_X followed by 'ADC _H_X' (conversion result[11:0]) .
- Reading from the 'ADC Read/Write All' register will output 2 data bytes (Low and high nibbles
- bytes) represent last ADC sampling for each active ADC channel, a maximum of 16 bytes for all ADC channels (see 4.4)
- Reading from all other internal registers will output 1 data byte.

Checksum - The message checksum byte.

5.2.2.2 PLC WRITE-REG command

This command writes data to internal registers of remoted SIG102 salve.

The format of the command:

Break field	Sync Byte	Identifier Byte	SIG102 Slave ID	Reg. Addr	Data	Checksum

- **Break field** - Hold the Data in line at low for a duration of 13 to 31 bits
- **Sync Byte** - send a 0x55 byte.
- **Identifier Byte** - **0xFB** for the write command
- **Slave ID** - The ID of the remote SIG102 slave we would like to write to.
- **Reg Add** - The internal SIG102 register address to write.
- **Data** - The data to be written to SIG102 slave internal register
- **Checksum** - The message checksum byte.

* Sending write command to an ADC channel activates the A/D conversion. The Data byte field is ignored (see 4.4).

5.2.2.3 PLC SLEEP command

Upon receiving this command, the SIG102 will compare the received ID to its ID or the broadcast ID. If there is a match the SIG102 will enter Sleep mode.

The format of the command:

Break field	Sync Byte	Identifier Byte	SIG102 Slave ID	Checksum

- **Break** field - Hold the Data in line at low for a duration of 13 to 31 bits
- **Sync Byte** - send a 0x55 byte.
- **Identifier Byte** - **0x3C** for the Sleep command (as in LIN2.0 specifications)
- **Slave ID** - The ID of the remote SIG102 slave we would like to put into Sleep mode.
- **Checksum** - The message checksum byte.

5.2.2.4 PLC CHANGE FREQUENCY commands

Upon receiving this command, the SIG102 will compare the received ID to its ID or the broadcast ID. If there is a match the SIG102 will change the frequency channel selection according to the identifier byte.

The format of the command:

Break field	Sync Byte	Identifier Byte	SIG102 Slave ID	Checksum

- **Break** field - Hold the Data in line at low for a duration of 13 to 31 bits
- **Sync Byte** - send a 0x55 byte.
- **Identifier Byte** -
- **0xB4** - Change frequency to **Main frequency**
- **0xB1** - Change frequency to **Alternate Frequency 1**,
- **0x32** - Change frequency to **Alternate frequency 2**.
- **Slave ID** - The ID of the remote SIG102 slave we would like to change its frequency selection.
- **Checksum** - The message checksum byte.

5.2.3 SIG102 PLC Commands examples

Example 1

Analog conversion of ADC channel 0 from SIG102 Slave **#5** start with a **PLC WRITE-REG command** to register ADC0_H:

Break Field	Sync Byte	Identifier Byte	SIG102 Slave ID	Reg. Address	Data	Checksum
0x00 ,0x00	**0x55**	**0xFB**	**0x05**	**0x25** ('ADC0_H' Address)	*** 0xXX**	**0xd9**

* When writing to an ADC channel the data byte is ignored.

Then, reading from **ADC_0_H**, by sending **PLC READ-REG** command:

Break Field	Sync Byte	Identifier Byte	SIG102 Slave ID	Reg Address
0x00 ,0x00	**0x55**	**0xBA**	**0x05**	**0x25** ('ADC0_H' Address)

The SIG102 response with the higher nibble conversion result **0x0134** (for instance) and a checksum byte. The conversion results are stored in the 'ADC0_H' and 'ADC0_L' registers.
The 'ADC0_H' stores the 8 MSB and the 'ADC0_L' store the 4 LSB shifted 4 times to the right.
'ADC0_H' = 0x13, 'ADC0_L' = 0x40.

Data	Checksum
0x13	**0x08**

Where Checksum = ~(0xBA + 0x05 +0x25 + 0x13) = ~(0xF7) = 0x08.

Reading from **ADC_0_L**, by sending **PLC READ-REG command** -

Sync Break	Sync Byte	Identifier Byte	SIG102 Slave ID	Reg. Address
0x00 ,0x00	**0x55**	**0xBA**	**0x05**	**0x26** ('ADC0_L' Address)

The SIG102 response with the full word conversion result **0x0134** and a checksum byte.

Data	Checksum
0x40,0x13	**0xC6**

Where Checksum = ~(0xBA + 0x05 +0x26 + 0x40 +0x13) = ~(0x138) => add the carry => ~(0x39)= 0xC6.

Example 2

SIG102 IOs 0, 3, and 7 are configured as analog inputs. to enable a sequentially ADC conversion of ADC 0, 3, and 7 from all active SIG102 slaves (global ID) starts with a **PLC WRITE-REG** to register **'ADC Read/Write All'** -

Break Field	Sync Byte	Identifier Byte	SIG102 Slave ID	Reg. Address	Data	Checksum
0x00 ,0x00	**0x55**	**0xFB**	**0xFF (global ID)**	**0x35** ('ADC R/W All' Address)	*** 0xXX**	**0xce**

* When writing to the 'ADC Read/Write All' register the data byte is ignored.
Upon receiving the write command, the SIG102 will start an ADC conversion starting from channel ADC0 and ending at channel ADC7.

Then, to read from SIG102 slave #3, send **PLC READ-REG to 'ADC Read/Write All' -**

Break Field	Sync Byte	Identifier Byte	SIG102 Slave ID	Reg. Address
0x00 ,0x00	**0x55**	**0xBA**	**0x03**	**0x35** ('ADC R/W All' Address)

The SIG102 response with ADC 0,3 and 7 conversion result **0x0254 , 0x0011 and 0x018F** (for instance) and a checksum byte. Starting from ADC0 lower nibble byte and ending with ADC7 higher nibble byte.

Data ADC0	Data ADC3	Data ADC7	Checksum
0x40,0x25	**0x10,0x01**	**0xF0,0x18**	**0xC2**

Where Checksum = ~(0xBA + 0x03+ 0x40 +0x25 + 0x10 +0x01 + 0xF0 + 0x18) = ~(0x23B) => add the carry => ~(0x3D)= 0xC2.

Example 3

Send **PLC-SLEEP** command to SIG102 slave #250:

Break Field	Sync Byte	Identifier Byte	SIG102 Slave ID	Checksum
0x00 ,0x00	**0x55**	**0x3C**	**0xFA**	**0xc8**

Where Checksum = ~(0x3C + 0xFA) = ~(0x136) => add the carry => ~(0x37)= 0xC8.

6 Power Operation Modes

The SIG102 has three power operation modes; Normal (RX/TX), Standby, and Sleep.

6.1 Normal mode

In Normal mode, the SIG102 is either in RX mode, listening for a powerline *PLC-byte* and *PLC-break*, or in TX mode, transmitting a message over the powerline.

6.2 Standby mode

The SIG102 enters Standby mode upon wake-up from Sleep mode, while the NSLEEP pin is still low. The SIG102 is kept in *Soft-Reset*, whereas communication with the ECU is suspended until the NSLEEP pin is set High.

6.3 Sleep modes (power-saving)

The SIG102 has four Sleep modes for best power consumption/performance during Sleep. See 6.3.4 - Sleep modes description. During this mode, only a small amount of hardware operates to detect wake-up messages (*WUM*) from the powerline and return to Normal mode operation.

Four interface pins are used for Sleep modes operation, as described in Table 12.

Table 12- Sleep interface pins

NSLEEP	Digital input	High - Normal mode is active. Low - Sleep /Standby mode is active. Upon transition from low to high, WUM is transmitted over the powerline.
INH	Digital output	Output indication to Inhibit the ECU. High - Normal mode is active. Low - Sleep mode is active.
HDO	Digital output	**Normal mode** - data output to ECU. **Sleep/Standby mode** - asserted low while wake-up message (WUM) is being detected /transmitted over the powerline.
HDC	Digital input	**Normal mode** – ECU's Host Command mode. **Sleep mode** - ECU wakes-up the SIG102 locally by toggling the HDC high-low-high. The SIG102 then exits the Sleep mode to Standby mode (NSLEEP still asserted low), or Normal mode (NSLEEP is high).

6.3.1 Wake-up message (*WUM)*

When *Auto-WUM* is enabled (*REG_6[6]='1'*), upon the rise of the NSLEEP pin the SIG102 transmits a *WUM* over the powerline to wake-up all network-connected devices.
ECU can configure the length of the WUM as described in Table 13.

Table 13 - Wake-up message length configuration

REG_6[4]	Wake-up message length
0	*SLP2* - 250usec / *SLP1, SLP3* - 75msec
1	*SLP2* - 1.5msec / *SLP1, SLP3* - 150msec

During WUM transmission, the HDO pin is asserted low until WUM transmission is completed, indicating to the ECU the wake-up process status. ECU shall wait for the HDO rise before initiating new bytes transfer.

6.3.2 Entering Sleep mode

During Sleep mode, the device is kept in *Soft-Reset* state and will not transfer bytes from the ECU nor receive bytes from the powerline. When the device enters Sleep mode, the INH pin is asserted low.
There are two ways to enter Sleep mode;

6.3.2.1 Enter Sleep by NSLEEP pin

By asserting the NSLEEP pin low, the SIG102 will enter Sleep mode.

6.3.2.2 Enter Sleep by register setting

By setting *REG_6[7]* high, the SIG102 will enter Sleep mode, and reset automatically *REG_6[7]* to low.

6.3.3 Exiting Sleep mode

There are three ways to exit Sleep mode. When exiting Sleep mode, the INH pin is raised and the device switches to Standby or Normal mode.

6.3.3.1 Exit Sleep by *WUM* detection

Upon detection of a *WUM*, the device exits Sleep mode, the INH pin raises and the device enters Standby mode.
In case the NSLEEP pin is low, the device remains in Standby mode, where the device is kept in *Soft-Reset*.
In case the NSLEEP pin is high, the device switches to Normal mode.

During WUM reception, the HDO pin is asserted low until WUM reception is completed, indicating the ECU on the wake-up process status. ECU shall wait for HDO to rise, before initiating new bytes transfer.

6.3.3.2 Exit sleep by NSLEEP pin

Upon detection of NSLEEP pin rise, the device exits Sleep mode, INH pin rises and enters Normal mode. When *Auto-WUM is* enabled, a WUM is transmitted over the powerline (see 6.3.1).

6.3.3.3 Exit Sleep by HDC toggling

Upon detection of HDC pin toggle high-low-high, the device exits Sleep mode, INH pin rises, and enters Standby mode.
In case the NSLEEP pin is still low, the device remains in Standby mode, where the device is kept in *Soft-Reset*.
In case the NSLEEP pin is high, the device switches to Normal mode.
In this case, the **WUM is NOT transmitted** over the powerline.
ECU shall use the HDC pin to exit Sleep mode when the NSLEEP pin is not connected.

6.3.4 Sleep modes description

ECU can select between four Sleep modes (see 7.7). Table 14 describes SIG102 sleep modes.

Table 14 - Sleep modes description

Sleep mode	Description	Typical Power consumption [A]	Performance
Enhanced sleep (SLP1)	The device wakes-up every 32ms to sense the powerline for WUM detection.	120µ	Wake-up detection with-in 64mSec. Best detection in a noisy environment.
Fast wake-up (SLP2)	The device continuously monitors the powerline for WUM detection.	1000µ	Fast wake-up detection with-in 250uSec.
Low-power (SLP3)	The device wakes-up every 32ms to sense the powerline for WUM detection.	85µ	Wake-up Detection with-in 64mSec.
Deep Sleep (SLP4)	The device does NOT wake-up to sense for bus activity, staying in deep sleep. Wake-up only locally by the ECU.	65µ	No bus wake-up detection.

6.3.4.1 Enhanced Sleep mode (*SLP1*)

By setting *REG_6[1:0] = '00*', the enhanced Sleep mode (*SLP1*) is selected.
When entering *SLP1*, the device wakes-up every 32ms periodically to monitor (sense period) for activity on the powerline. If a WUM is detected, the device exits sleep mode as described in section 6.3.3.1, otherwise, the device returns to Sleep mode until the next sense period, and so on...

6.3.4.2 Fast wake-up Sleep mode (*SLP2*)

By setting *REG_6[1:0] = '01'*, the Fast wake-up Sleep mode (*SLP2*) is selected. The device continuously monitors the powerline for WUM detection. The WUM detection is within 250usec. When WUM is detected, the device exits Sleep mode as described in section 6.3.3.1.

6.3.4.3 Low-power Sleep mode (*SLP3*)

By setting *REG_6[1:0] = '10*', the low-power mode (*SLP3*) is selected. The device wakes-up every 32msec to sense activity on the powerline. If a WUM is detected, the device exits Sleep mode as described in section 6.3.3.1, otherwise, the device returns to Sleep until the next sense period, and so on.

6.3.4.4 Deep Sleep mode (*SLP4*)

By setting *REG_6[1:0] = '11'*, the Deep Sleep mode (*SLP4*) is selected. The device does NOT wake-up to sense the powerline for activity, rather than stay in deep sleep, whereas most of its hardware is shut down to maintain the lowest power consumption.
The device exits Deep Sleep mode only locally, either by NSLEEP or HDC pins (see 6.3.3.2 and 6.3.3.3).

6.4 Auto Sleep mode

Auto sleep mode is enabled either by pulling the NAUTO_SLEEP pin low or by clearing *REG_6[5].*
The last action prevails.
When enabled, the SIG102 automatically enters into Sleep mode when no Transmission or reception to/from the powerline (DC-BUS idle) for more than the *AutoSleep-timeout* setting.
The SIG102 exits sleep mode in case of NSLEEP/HDC pin toggling, or by *WUM* detection (see 6.3.3).

Table 15 describes the *AutoSleep-timeout* configuration options.

Table 15 - *AutoSleep-timeout* configuration

REG_6[3:2]	AutoSleep-timeout [Seconds]
00	Auto Sleep mode disabled
01	2
10	4
11	6 (default)

6.5 Sleep modes Examples

6.5.1.1 Sleep Example 1 - Enter by NSLEEP, Exit Sleep mode by *NSLEEP & WUM*

Figure 16 depicts entering sleep by NSLEEP and exit sleep by NSLEEP pin (Node A) and WUM detection (Node B).
In this example, the ECU wakes-up device Node A by raising the NSLEEP pin, causing the INH pin to raise, and a WUM is transmitted over the powerline (*Auto-WUM* is enabled) to wake-up Node B.
While transmitting the WUM, device Node A asserts HDO pin low. After completion of WUM transmission, the HDO pin is raised again (can be used as signal/interrupt to ECU). At the Node B side, during its sensing period (e.g. *SLP1),* the WUM is detected, and the INH pin rises while switching to Standby mode. Node B HDO pin is asserted low for the reaming duration of WUM reception. Then, ECU Node B raises the NSLEEP pin and the device switches to Normal mode.

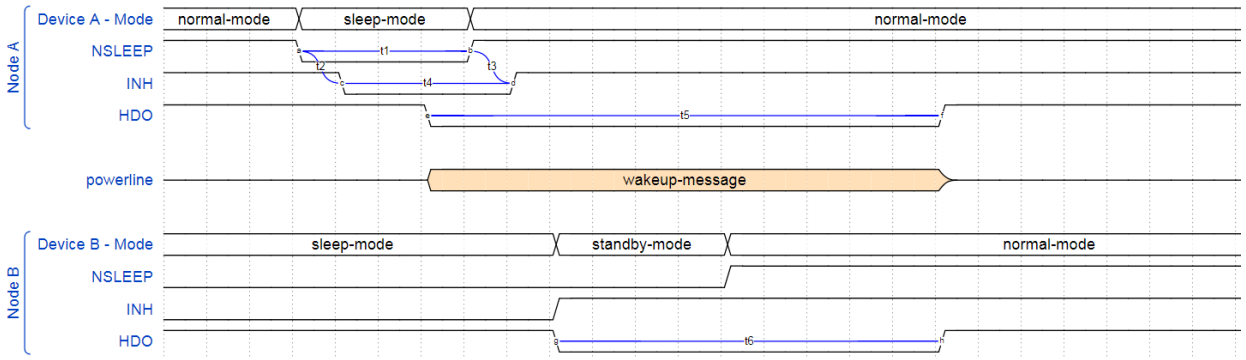


Figure 16 - Enter sleep by NSLEEP, Exit sleep by *NSLEEP & WUM*

6.5.1.2 Sleep Example 2 - Enter sleep by control register bit, exit sleep by HDC

Figure 17 depicts entering sleep by setting *REG_6[7]* high and exiting Sleep mode by toggling the HDC pin.
In this example, ECU configured *REG_6[7]* high using Command mode, the device enters Sleep mode, and INH pin drops. After a while, ECU toggle HDC pin low to high, and the device exits Sleep mode without transmitting the WUM, raising the INH pin and switching to Normal mode again.

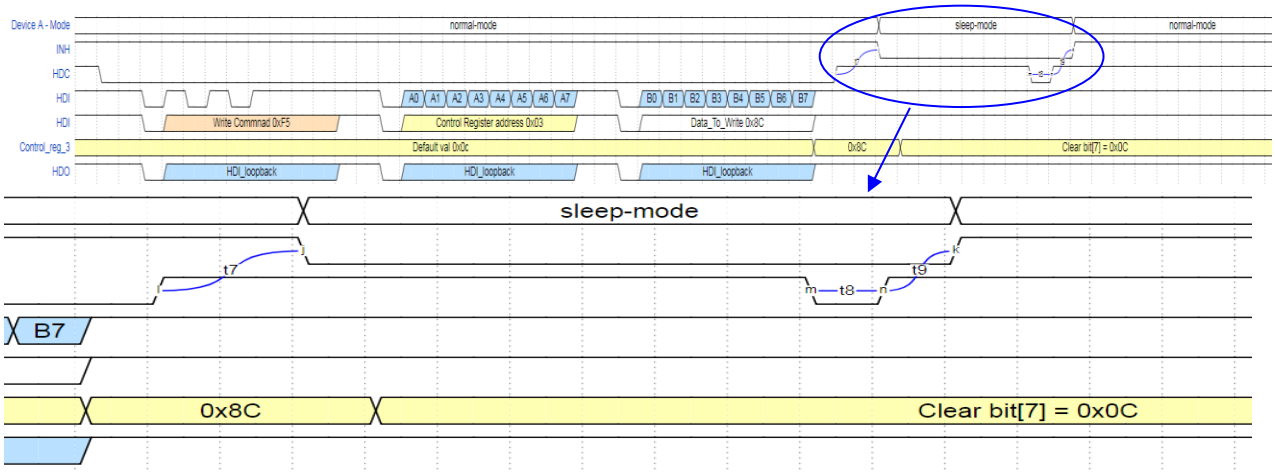


Figure 17 - Enter sleep by control register bit, Exit sleep by *HDC*

7 SIG102 Control Registers

The SIG102 internal control registers are used for configuration and status checks. Each register is accessible from its ECU for *Read* and *Write* operations. This section elaborates on the registers and their default values after power-up/reset. See section 7.14 for more details about the registers configuration method.

Table 16 - Registers summary table

Register name	Addr.	Description
REG_0 - 'Device Control 0'	0x00	Bitrate selection, Loopback, nAuto_freq_change
REG_1 - 'Device Control 1'	0x01	Transmit level control
REG_2 - 'Frequency Main select'	0x02	Main Carrier frequency selection
Reg_3 - 'Frequency ALT1 select'	0x03	Alternate frequency 1 selection
REG_4 - 'Frequency ALT2 select'	0x04	Alternate frequency 2 selection
REG_5 - 'Active frequency'	0x05	Read only – read the active frequency - Main/Alt1/Alt2
REG_6 - 'Sleep control'	0x06	Sleep mode selection and functionality
REG_37 - SIG102 UUID[47:40]	0x37	Read only - UUID[47:40]
REG_38 - SIG102 UUID[39:32]	0x38	Read only - UUID[39:32]
REG_39 - SIG102 UUID[31:24]	0x39	Read only - UUID[31:24]
REG_3A - SIG102 UUID[23:16]	0x3A	Read only - UUID[23:16]
REG_3B - SIG102 UUID[15:8]	0x3B	Read only - UUID[15:8]
REG_3C - SIG102 UUID[7:0]	0x3C	Read only - UUID[7:0]

7.1 REG_0 - 'Device Control 0' (Address 0x00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R	R/W[0]	R/W [1]	R/W [0]	R/W [1]	R/W [0]	R/W [1]	R/W [0]
Reserved	0	nLoopBack	Remote loopback	nAuto_Freq _change	Bitrate_sel[2:0]		

Bit [2:0] - Bitrate selection (see 3.3).
Bit [3] - nAuto_freq_change: '0' enables auto frequency change mode (see 3.3.3).
Bit [4] - Enable remote loopback mode (see 3.3.5).
Bit [5] - nLoopBack -Set this bit to disables loopback between HDI to HDO (see 3.3.4).
Bit [6] - Must be written as '0'
Bit [7] - Reserved

R - Readable bit, W - Writeable bit [x] - Value on power-up. '1' - bit is set; '0' - bit is cleared

7.2 REG_1 - 'Device Control 1' (Address 0x01)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W [0]	R/W [0]	R/W [0]	R/W [1]	R/W [1]	R/W [1]	R/W [1]	R/W [1]
Enable TXO high power	0	0	TX signal level	1	1	1	1

Bit [3:0] - Must be written as '1111'
Bit [4] - TX signal level control at TXO pin: '0' - 1Vpp, '1'- 2Vpp (see 2.5.7).
Bit [6:5] - Must be written as '00'
Bit [7] - Enable TXO high power. Set this bit to enable maximal TXO drive of 66mA, clear this bit for maximal TXO drive of 33mA (see 2.5.7).

R - Readable bit, W - Writeable bit [x] - Value on power-up. '1' - bit is set; '0' - bit is cleared

7.3 REG_2 - 'Main Frequency Select' (Address 0x02)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W [0]	R/W [1]	R/W [0]	R/W [1]	R/W [0]	R/W [0]	R/W [0]	R/W [0]
Main Carrier Frequency Configuration							

Bit [7:0] - Main Carrier Frequency configuration. The default configuration is 13MHz [1].

[1] After REG_2 configuration no other internal register configuration is allowed for 1ms. It is recommended to place the carrier frequency configuration last during multiple registers configuration and wait at least 1ms after HDC is released (See section 3.3.2.1).

7.4 REG_3 - 'ALT 1 Frequency Select' (Address 0x03)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]
Alternate Carrier Frequency 1 Configuration – ALT1							

Bit [7:0] - Alternate Carrier Frequency 1 configuration. Default configuration is 5MHz (See section 3.3.2.1).

7.5 REG_4 - 'ALT 2 Frequency Select' (Address 0x04)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W [1]	R/W [0]	R/W [1]	R/W [0]	R/W [1]	R/W [0]	R/W [1]	R/W [0]
Alternate Carrier Frequency 2 Configuration – ALT2							

Bit [7:0] - Alternate Carrier Frequency 2 configuration. Default configuration is 22MHz (See section 3.3.2.1).

7.6 REG_5 - 'Active Frequency Select' (Read-Only, Address 0x05)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R	R	R	R	R	R	R	R
Current Active Carrier Frequency Configuration							

Bit [7:0] - Current Active Carrier Frequency (See section 3.3.2.1).

7.7 REG_6 - 'Sleep Control' (Address 0x06)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W [0]	R/W [1]	R/W [1]	R/W [1]	R/W [1]	R/W [1]	R/W [0]	R/W [0]
Enter Sleep mode	Auto WUM	nAutoSleep	Long WUM	AutoSleep-timeout		Sleep modes selection	

Bit [1:0] '00' - Enhanced Sleep mode [*SLP1*],
'01' -Fast wake-up Sleep mode [*SLP2*],
'10' - Low-power sleep mode [*SLP3*],
'11' - Deep Sleep mode [*SLP4*] (see section6.3).

Bit [3:2] - *AutoSleep-timeout* - The time before entering into sleep mode (when AutoSleep mode is enabled). The duration is in seconds x 2 (i.e. default 6 sec), see 6.4.

Bit [4] - Wake-up message duration over the powerline (see Table 13).

Bit [6] - Auto wake-up message (WUM): '0' disables transmission of WUM upon NSLEEP pin wakeup.

Bit [7] - Enter Sleep mode reg. Activates the Sleep mode as selected in Bit [1:0] by setting bit[7]. Upon entering Sleep mode, bit [7] is automatically cleared to '0'.

R - Readable bit, W - Writeable bit [x] - Value on power-up. '1' - bit is set; '0' - bit is cleared

7.8 REG_37 – UUID[47:40] (Address 0x37)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R	R	R	R	R	R	R	R
UUID[47:40]							

Bits [7:0] - UUID[47:40]

R - Readable bit, W - Writeable bit [x] - Value on power-up. '1' - bit is set; '0' - bit is cleared

7.9 REG_38 – UUID[39:32] (Address 0x38)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R	R	R	R	R	R	R	R
UUID[39:32]							

Bits [7:0] - UUID[39:32]

R - Readable bit, W - Writeable bit [x] - Value on power-up. '1' - bit is set; '0' - bit is cleared

7.10 REG_39 – UUID[31:24] (Address 0x39)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R	R	R	R	R	R	R	R
UUID[31:24]							

Bits [7:0] - UUID[31:24]

R - Readable bit, W - Writeable bit [x] - Value on power-up. '1' - bit is set; '0' - bit is cleared

7.11 REG_3A – UUID[23:16] (Address 0x3A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R	R	R	R	R	R	R	R
UUID[23:16]							

Bits [7:0] - UUID[23:16]

R - Readable bit, W - Writeable bit [x] - Value on power-up. '1' - bit is set; '0' - bit is cleared

7.12 REG_3B – UUID[15:8] (Address 0x3B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R	R	R	R	R	R	R	R
UUID[15:8]							

Bits [7:0] - UUID[15:8]

R - Readable bit, W - Writeable bit [x] - Value on power-up. '1' - bit is set; '0' - bit is cleared

7.13 REG_3C – UUID[7:0] (Address 0x3C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R	R	R	R	R	R	R	R
UUID[7:0]							

Bits [7:0] - UUID[7:0]

R - Readable bit, W - Writeable bit [x] - Value on power-up. '1' - bit is set; '0' - bit is cleared

7.14 Registers configuration (Command mode)

The Command mode allows the ECU to access the SIG102 internal registers for write and read operations.
Enter the Command mode by lowering the HDC pin. During Command mode, the SIG102 is in *Soft-Reset* state. The device's powerline communication is disabled. Every register configuration is kept until the next power-up/reset event.
During command mode, the SIG102 will automatically learn the Host bitrate regardless of SIG102 configured bitrate. When exiting the command mode to normal mode, the SIG102 returns to its configured bitrate. This way, the host does not need to switch to SIG102 bitrate during configuration mode.
For example, upon hard-reset/ power-up , the default SIG102 bitrate is 19.2kbit/s. Host bitrate is set to 115.2 kbit/s. The host can configure the SIG102 bitrate REG_0[2:0] using 115.2kbit/s bitrate during configuration. When returning to normal mode, the SIG102 will be configured to 115.2kbit/s until the next hard-reset/power-cycle.

7.14.1 WRITE-REG command

Write register command consists of three bytes as described in Table 17.

Table 17 - WRITE-REG command structure

1st Byte	2nd Byte	3rd Byte
0xF5	**Register address**	**Data to write**

The 1st byte, 0xF5, is the write command byte.

The 2nd byte is the designated register address to write to.

The 3rd byte is the data byte value to be written.

For example, writing 0x34 to REG_3 (address 0x03) preformed as follows:

1. Lower the HDC pin (Enter Command mode).
2. Wait at least 100nsec
3. Transfer 3 bytes: [0xF5][0x03][0x34] - The value 0x34 is written to REG_3.
4. Wait for at least 100ns.
5. Raise the HDC pin (Exit Command mode to Normal mode).

7.14.1.1 Example 1 - *WRITE-REG* command

Figure 18 depicts a *WRITE-REG* command sequence. First, the HDC is pulled low and the device enters the Command mode. The ECU sends the write command with the 1st byte of 0xF5, followed by the control register address byte (A[7:0]) and the data byte to be written (B[7:0]). After completing the write sequence, the HDC pin is pulled high and the device returns to Normal mode.

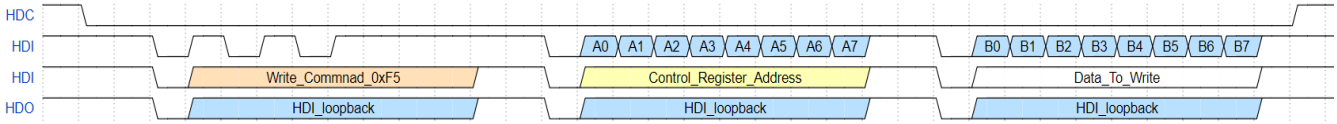


Figure 18- WRITE-REG command sequence

7.14.2 READ-REG command

A READ-REG command consists of 2 bytes as described in Table 18.

Table 18 - READ-REG command structure

1st Byte	2nd Byte
0xFD	Register address

The 1st byte, 0xFD, is the Read command byte.

The 2nd byte is the designated register address to read from.

Following the second byte, the SIG102 outputs the register value to ECU.

For example, reading from REG_5 (address 0x05) is performed as follows:

1. Lower the HDC pin (Enter Command mode).
2. Wait at least 100nsec
3. Transfer 2 bytes: [0xFD][0x05]
4. Wait for the SIG102 to output the value of REG_5.
5. Wait for at least 100ns.
6. Raise the HDC pin (Exit Command mode to Normal mode).

7.14.2.1 Example 2 - *READ-REG* command

Figure 19 depicts a *READ-REG* command sequence. First, the HDC is pulled low and the device enters the Command mode. The ECU sends the read command with the 1st byte of 0xFD, followed by the control register address byte (A[7:0]). Then the ECU receives the register internal value (B[7:0]). The HDC pulled back to high and the device returns to Normal mode.

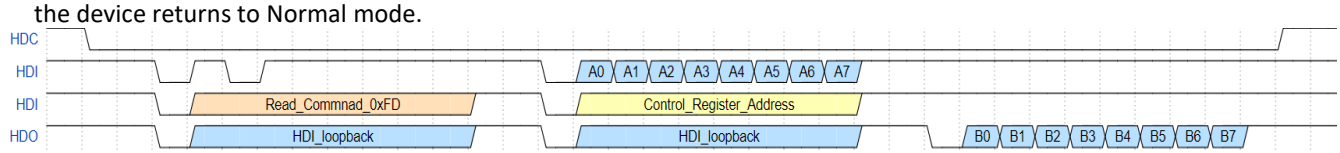


Figure 19 – READ-REG command sequence

8 Specifications

Table 19 - Absolute maximal rating

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
Input voltage, DC	V_{im}		-0.6	3.3	3.9	V
Output voltage, DC	V_{om}		-0.6	3.3	3.9	V
Ambient temperature	T_{am}		-40		125	°C
Storage temperature	T_{sm}		-55		150	°C

Table 20 - Recommended operation conditions

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DVCC} V_{AVCC}		3.0	3.3	3.6	V
Supply Voltage ripple	V_{CC_RIP} A_{VCC_RIP}	Max 2.5MHz, waveform type of triangular		50m		V-p-p
Ambient operating temperature range	T_A		-40		105	°C
Minimum high-level input voltage	V_{IH}		2			V
Maximum low-level input voltage	V_{IL}				0.8	V
Minimum high-level output voltage	V_{OH}		2.4			V
Maximum low-level output voltage	V_{OL}				0.4	V
Maximal output current	I_{out}	see Table 1				
Maximum input current	I_{IN}		-1		1	µA

Table 21 - Device characteristics

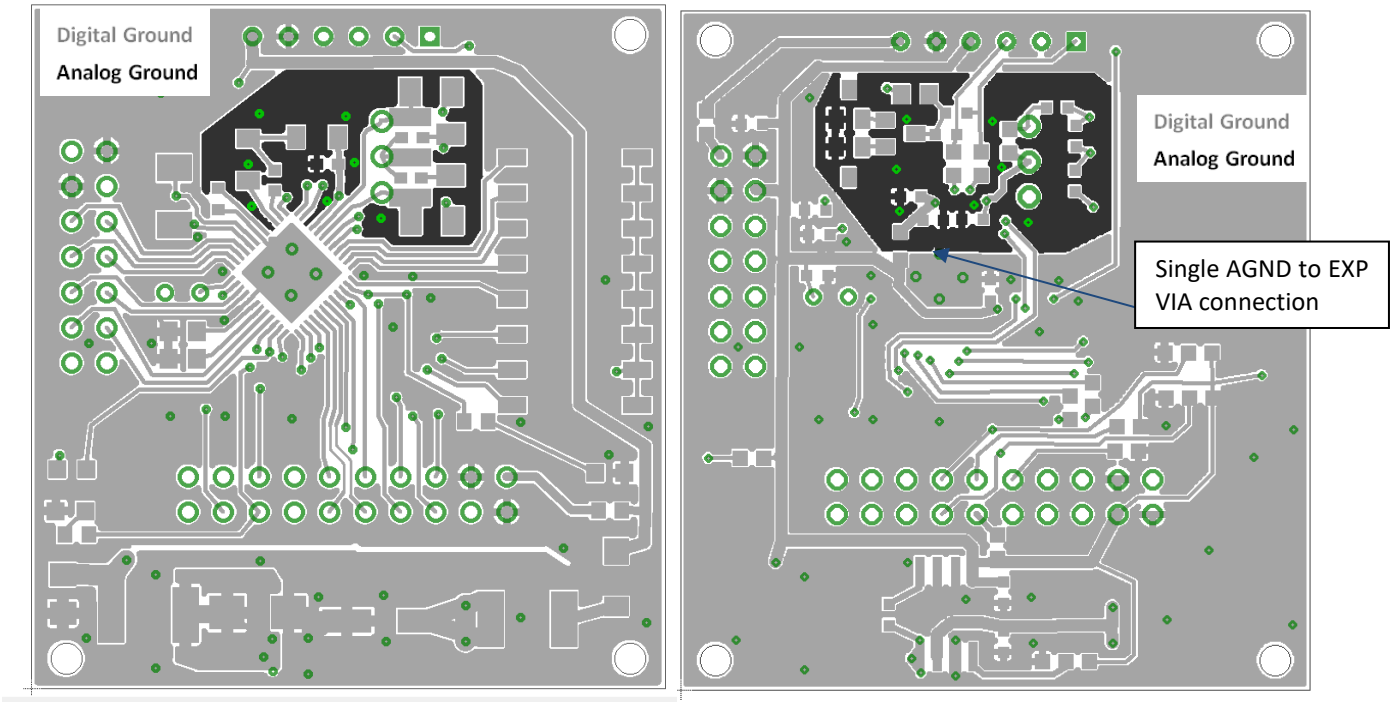
Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
External components requierments						
Powerline coupling capacitor	$C_{coupling}$	Capacitor rate should be selected with respect to powerline voltage		2.2		nF
Protection diodes capacitance	D_{protec}			10		pF
Capacitor at VCAP	V_{cap}		1	4.7		µF
Capacitor at PLLCAP	PLL_{cap}		1			µF
Capacitor at VREF	$VREF_{cap}$		1			µF
Inductor at L1	L1	see 2.5.4		3.3 / 18		µH
Inductor at L2	L2			15		µH
L1 pin input capacitance					1	pF
Crystal frequency	$Xtal_{\_freq}$	see 2.5.3		16		MHz
Crystal frequency tolerance	$Xtal_{\_ppm}$				50	±ppm
AC signals characteristics						
Tx signal at TXO	TXO_{lev_1}	TXON high (transmission is active) see 2.5.7		1		V-p-p
	TXO_{lev_2}			2		V-p-p
TXO input impedance	TXO_{In}	TXON low (transmission is not active)	5.3k			Ω
TXO output impedance	TXO_{out}	TXON high (transmission is active)		18		Ω
TXO driving strength	I_{TXO}	TXON high (transmission is active)	33		66	mA

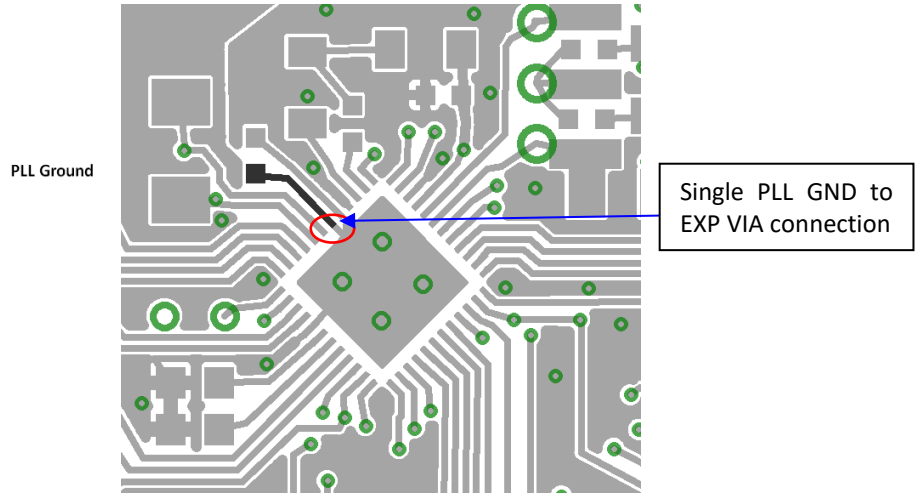
Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
Rx signal at RXI	RXI_{lev}		10m		3.3	V-p-p
RXI input impedance	RXI_{In}		5.1k			Ω
Carrier Frequency in-band (channels selection)	F_c	Selection resolution is 100kHz, a total of 251 carrier frequencies, see 3.3.2.1	5		30	MHz
Adjacent channels spacing	F_{adj}	The space between two adjacent channels operating over the same powerline.	1			MHz
Timing requierments of prtocols interfaces						
UART bitrate	$UART_{br}$	Host UART bitrate, see 3.3	9.6		115.2	kbit/s
Powerline latency	T_{RX_delay}	The delay from host start bit transmission to host start bit reception.		2.5		T_{bit}
Powerline byte-field length	T_{pl_byte}			10		T_{bit}
IO Characteristics						
ADC sample rate				50		Ksps
ADC resolution				9	12	bit
Analog pin source impedance		To guarantee a conversion error of less than that 0.5LSB			45	kΩ
PWM Frequency			0.1225		31.37	kHz
Timing of device operation modes						
Power-cycle/ hard-reset	T_{init}	Initialization time after power-cycle or hard-reset event.		2		ms
Carrier frequency change	T_{freq_cng}	Carrier frequency change process time. During this period no-host operation is allowed.		1		ms
Register configuration	$T_{hdc\_to\_hdi}$	The minimal wait time from HDC drop/rise to HDI drop.	250			ns
Current Consumtption @ 3.3V						
Normal TX mode – low power	I_{Tx_lp}	TXON high (transmission is active)		60		mA
Normal TX mode – high power	I_{Tx_hp}			80		mA
Normal RX mode	I_{RX}	TXON low (transmission is not active)		30		mA
Enhanced sleep (SLP1)	I_{slp1}	see 6.3		120		µA
Fast wake-up (SLP2)	I_{slp2}	see 6.3		1000		µA
Low-power (SLP3)	I_{slp3}	see 6.3		85		µA
Deep Sleep (SLP4)	I_{slp4}	see 6.3		65		µA

9 SIG102 PCB layout recommendation

Note: Analog ground layer and GND PLL should be connected to the digital ground near the Exp pad.

TOP **Bottom**





- ✓ VCC and DGND layout traces should be as wide as possible. Connect a 0.1uF capacitor between each VCC and DGND pins, as close as possible to the pins.
- ✓ It is recommended to keep the traces connecting the 3.3V power supply to VCC pins as short as possible with wide PCB traces.
- ✓ Connect AGND to EXP with a single short trace.
- ✓ Connect PLL_GND to EXP with a single short trace.
- ✓ Connect L1, L2, C3, C5, C7, C8, C11, and C12 as close as possible to their pins.
- ✓ Connect R1 as close as possible to the RXI pin.
- ✓ Connect all filtering caps as close as possible to their pins.
- ✓ Connect crystal and its capacitors close to OSCI and OSCO pins. Keep DGND plan around them.

10 Package, Mechanical

The SIG102 package in QFN 48 7mm x 7mm.

10.1 Mechanical Drawing

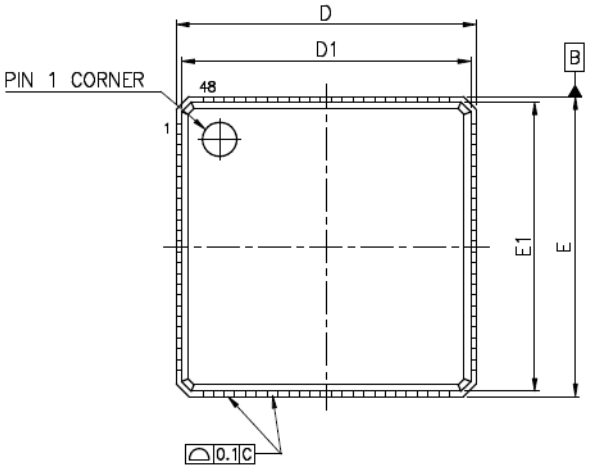
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.65 REF.	
A3		0.203 REF.	
b	0.18	0.25	0.30
c	0.24	0.42	0.60
D	6.90	7.00	7.10
D1	6.65	6.75	6.85
E	6.90	7.00	7.10
E1	6.65	6.75	6.85
e		0.50 BSC.	
K	0.20	—	—
L	0.30	0.40	0.50
θ°	0.00	—	12.00

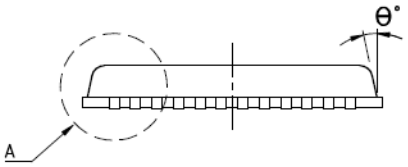
UNIT : mm

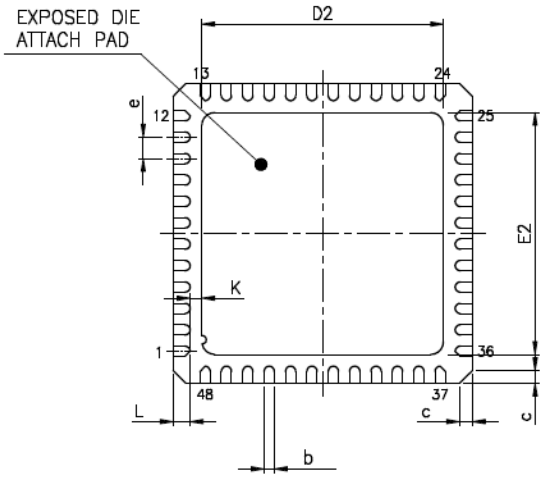
	D2			E2		
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
157X157MIL	3.40	3.60	3.80	3.40	3.60	3.80
213X213MIL	5.00	5.20	5.40	5.00	5.20	5.40
9 208X208MIL	4.90	5.10	5.30	4.90	5.10	5.30

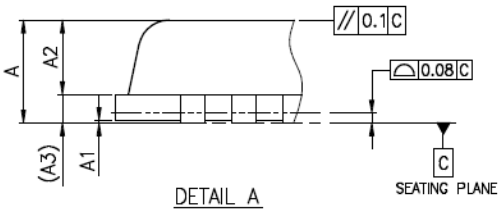
UNIT : mm

NOTES :
1. JEDEC : MO-220 VKKD-2.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (0.012 INCHES MAXIMUM).
3. DIMENSION "b" APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. THE PIN #1 IDENTIFIER EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
7. DIMENSION "A1" APPLIED ONLY TO TERMINALS.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

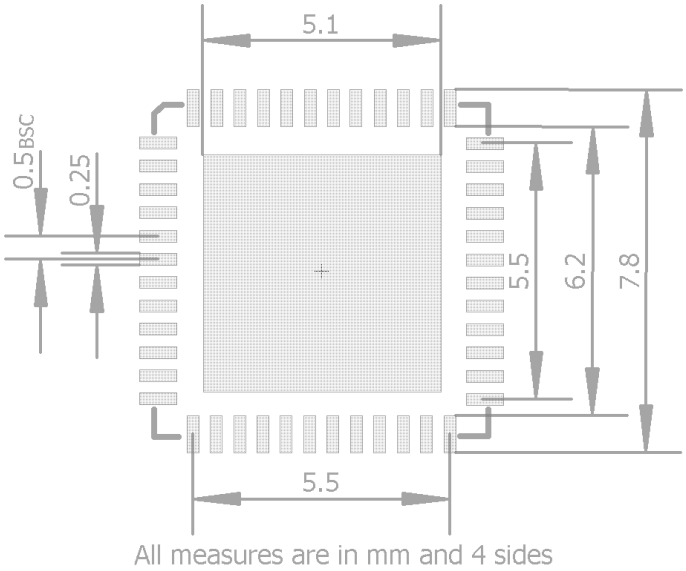








10.2 PCB Drawing



10.3 Soldering profile

Soldering reflow profile is according to IPC/JEDEC J-STD-020 (MSL3).

- The peak temperature (TP) is 260°C.
- Holding time is between 60 sec to 120 sec between TH min 150°C to TH max 200°C.
- Liquidus temperature (TL) is 217 °C. Liquidus time is between 60 sec to 150 sec.
- TL to TP max ramp-up is 3°C/sec.
- TP to TL max cooldown rate is 6°C/sec.
- Max time above 255°C (Tp) is 30 sec.

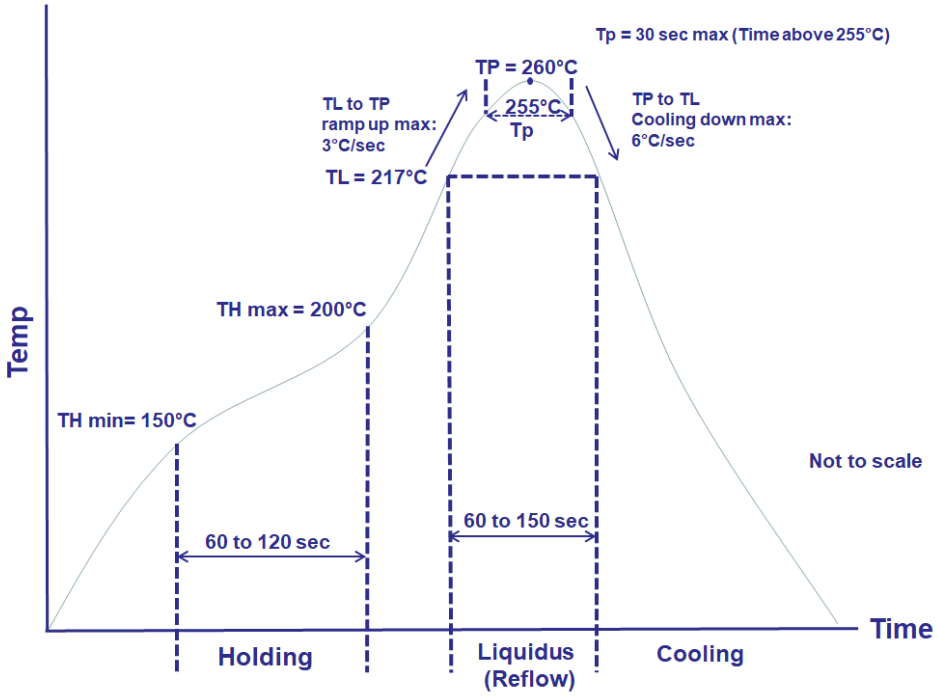


Figure 20 – Representation of IPC/JEDEC J-STD-020 (MSL3) profile

11 Test Environment

Figure 21 depicts the DC-BUS Test environment that allows testing the SIG102 devices in the emulated lab DC powerline environment.

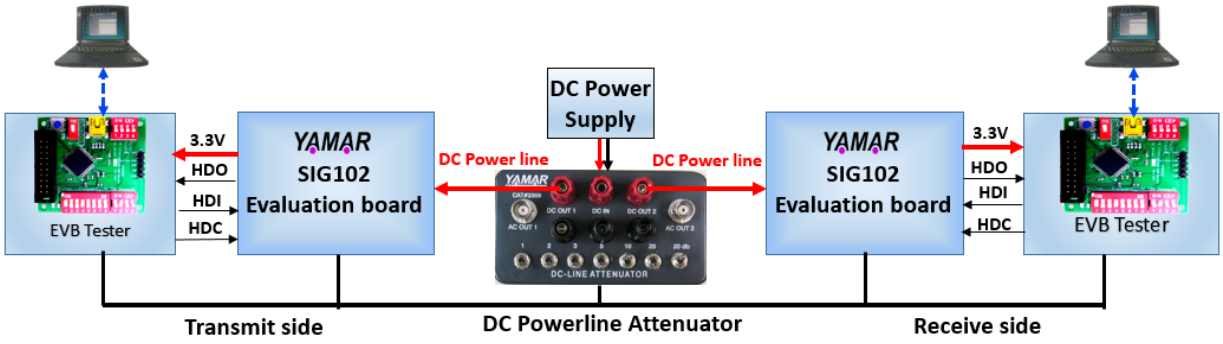


Figure 21 – SIG102 communication test environment

This test environment consists of two SIG102 evaluation boards (EVB), two EVB Testers, and a PC Test Program. The DC-powerline attenuator is optional. There are possibilities to perform the tests as shown in Figure 21 – SIG102 communication test environment.

11.1 Communication tests

At the transmitting side, the EVB Tester generates repeatedly a predefined test message [a b c ...x y z] saving the need for a second PC. At the receiver side, the test message is transferred from the EVB through the USB interface to a PC. The Test program analyzes the received predefined messages, and perform BER statistics including error byte, miss byte, and noise byte counting indications.

The DC-powerline attenuator is used to test the communication in variable attenuation levels (0-61dB), emulating a DC powerline environment. When connecting the EVB directly to a power supply, it is recommended to add in serial to the power supply an inductor (>22uH) to avoid strong attenuation due to the power supply input filtering capacitors.

11.2 Remote I/O test

The PC program is capable to generate I/O commands to a remote SIG102 device. The SIG102 EVB has an I/O connector that can be interfaced to the user's application.

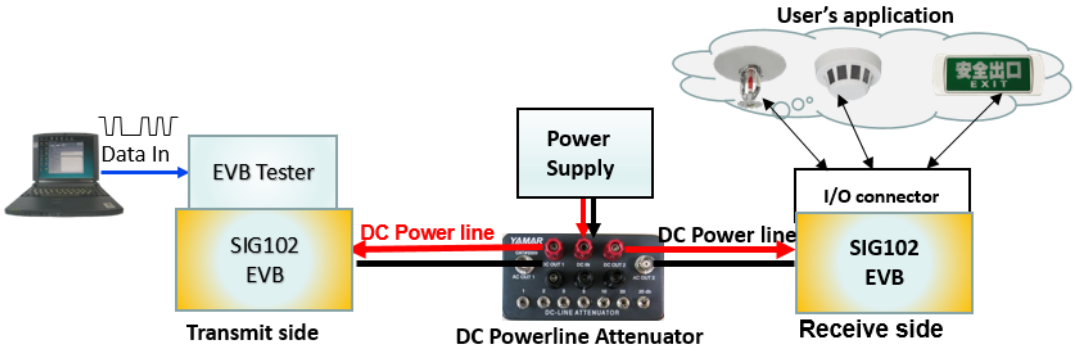


Figure 22 - Remote I/O testing

Revision History

Rev.	Date	Description
0.74	01/08/2019	Initial preliminary revision.
0.75	08/09/2019	Update schematic, Table 20.
0.76	23/09/2019	Editing.
0.77	02/10/2019	Update Table 3 and Figure 7.
0.78	14/11/2019	Update Figure 5 and NSLEEP pin description.
0.79	19/01/2020	Update Table 3.
0.80	19/02/2020	Update clause 2.5.3. Add UUID clause 3.3.6. Update clause 7 with UUID REGs.
0.81	21/04/2020	Add soldering profile description in section 10.3.
0.82	01/08/2020	Update 2.5.3, 2.5.5 and Table 21.
0.83	15/09/2020	Update section 10.2 dimension.
0.84	18/11/2020	Update section 3.3.2.1 description.
0.85	01/12/2020	Update Table 2.
0.86	12/01/2021	Editing.
0.87	31/08/2021	Update Figure 4, Figure 5, and section 5.2.1.2

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