

Features

- ESD protection for one line with uni-direction
- Provide transient protection for one line to IEC 61000-4-2 (ESD) ±30kV (air/contact)
 IEC 61000-4-4 (EFT) 80A (5/50ns)
 IEC 61000-4-5 (Lightning) 140A (8/20μs)
- Suitable for, 20V and below, operating voltage applications
- 2.0mm x 1.8mm DFN package saves board space
- High surge protection
- Protect one I/O line or one power line
- Fast turn-on and low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- Green part

Applications

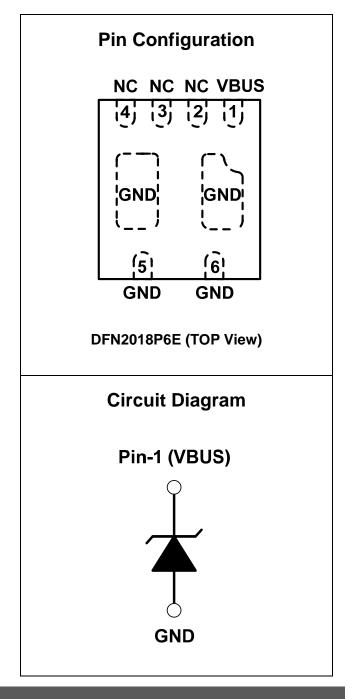
- Power supply protection
- USB VBUS protection
- · Cellular handsets and accessories
- Panel modules
- Portable devices
- Touch panels
- Notebooks and handhelds
- Peripherals

Description

AZ4920-01F is a design which includes a uni-directional surge rated clamping cell to protect one power line, one control line, or one low-speed data line in an electronic system. The AZ4920-01F has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage caused by Electrostatic Discharging (ESD), Electrical Fast Transient (EFT), Lightning, and Cable Discharge Event (CDE).

AZ4920-01F is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line, control lines, or data lines, protecting any downstream component.

AZ4920-01F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).





Specifications

Absolute Maximum Ratings (T _A = 25°C, unless otherwise specified)				
Parameter	Symbol	Rating	Unit	
Peak Pulse Current (t _p =8/20μs)	I _{PP} (Note 1)	140	Α	
Operating Voltage (Pin-1 to GND)	V_{DC}	21	V	
ESD per IEC 61000-4-2 (Air)	V _{ESD-1}	±30	kV	
ESD per IEC 61000-4-2 (Contact)	$V_{\text{ESD-2}}$	±30	kV	
Lead Soldering Temperature	T _{SOL}	260 (10 sec.)	°C	
Operating Temperature	T _{OP}	-55 to +125	°C	
Storage Temperature	T _{STO}	-55 to +150	°C	

Electrical Characteristics						
Parameter	Symbol	Condition	Min	Тур	Max	Unit
Reverse Stand-Off	V_{RWM}	Pin-1 to GND, T = 25 °C.			20	V
Voltage	▼ RWM	FIII-1 to GND, 1 – 25 °C.			20	V
Reverse Leakage	I_{Leak}	V _{RWM} = 20V, T = 25 °C, pin-1 to GND.			0.5	μΑ
Current	Leak	V _{RWM} - 20V, 1 - 25 C, piii-1 to GND.			0.5	μΑ
Reverse Breakdown	V_{BV}	I_{BV} = 1mA, T = 25 °C, pin-1 to GND.	21.8		24.5	V
Voltage	∧ B∧	I _{BV} = IIIIA, I = 25 C, piii-1 to GND.			24.5	V
Forward Voltage	V_{F}	$I_F = 15$ mA, T = 25 °C, GND to pin-1.	0.5		1	V
	$V_{\text{CL-surge}}$	$I_{PP} = 5A$, $t_p = 8/20 \mu s$, $T = 25 ^{\circ}C$,		24	26	V
Overes Olemenia		pin-1 to GND.				
Surge Clamping		$I_{PP} = 100A$, $t_p = 8/20\mu s$, $T = 25$ °C,		32	35	V
Voltage (Note 1)		pin-1 to GND. $I_{PP} = 140A$, $t_p = 8/20\mu s$, $T = 25 °C$,				
		pin-1 to GND.		36	39	V
ESD Clamping	$V_{\text{CL-ESD}}$	IEC 61000-4-2 +8kV (I _{TLP} = 16A), T =		23.5		V
Voltage (Note 2)	V CL-ESD	25 °C, contact mode, pin-1 to GND.		23.5		V
ESD Dynamic	D	IEC 61000-4-2 0~+8kV, T = 25 °C,	0.04			Ω
Turn-on Resistance	$R_{dynamic}$	contact mode, pin-1 to GND.		0.04		
Channel Input	C	V _{IN} = 0V, f = 1MHz, T = 25 °C,	650 800		nE	
Capacitance	C _{IN}	pin-1 to GND.		050		pF

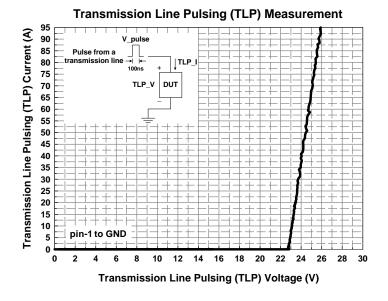
Note 1: The Peak Pulse Current measured conditions: t_p = 8/20 μ s, 2Ω source impedance.

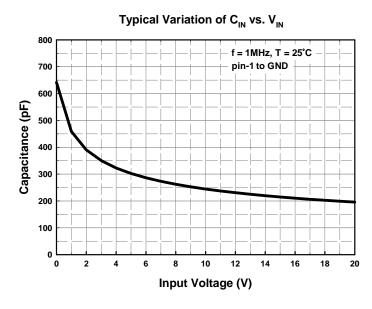
Note 2: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

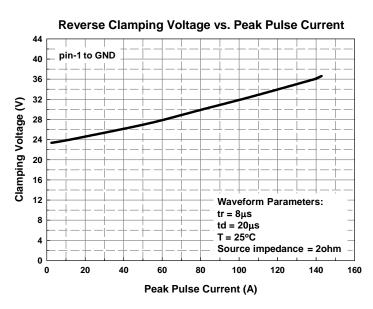
TLP conditions: $Z_0 = 50\Omega$, $t_p = 100$ ns, $t_r = 1$ ns.

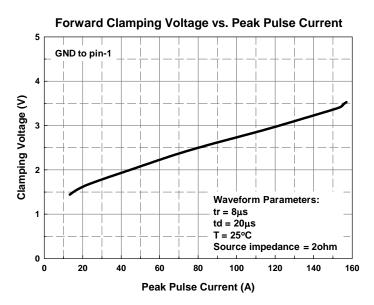


Typical Characteristics











Application Information

The AZ4920-01F is designed to protect one line against system ESD/EFT/Lightning pulses by clamping them to an acceptable reference.

The usage of the AZ4920-01F is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected to pin-1. The pin-5, pin-6 and center tabs should be connected directly to a ground plane on the board. All path lengths connected to the pins of AZ4920-01F should be kept as short as possible to minimize parasitic inductance in the board traces.

In order to obtain enough suppression of ESD induced transient, a good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ4920-01F.
- Place the AZ4920-01F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

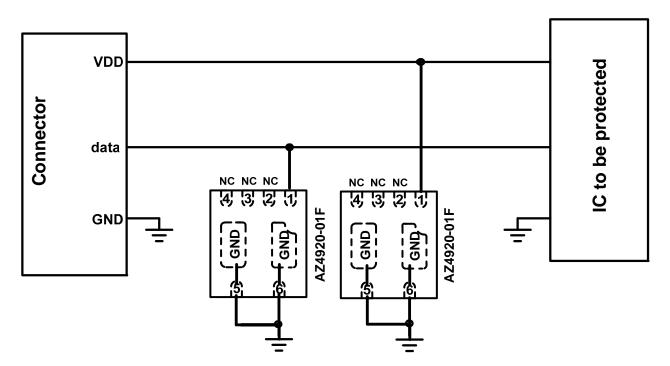


Fig. 1

Fig. 2 shows another simplified example of using AZ4920-01F to protect the control lines,

low-speed data lines, and power lines from ESD transient stress.

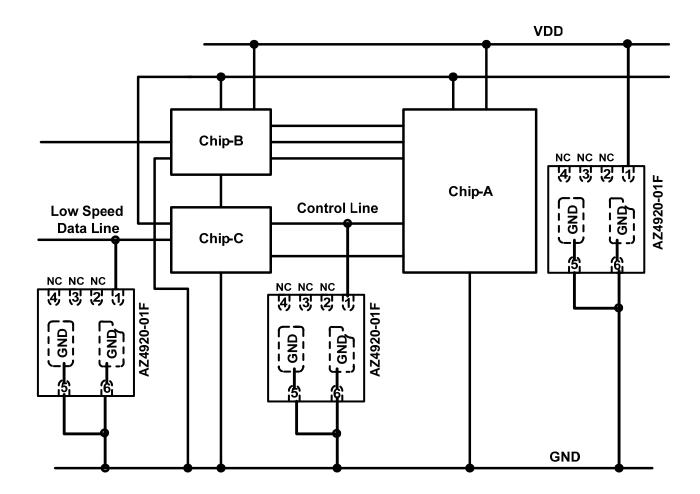


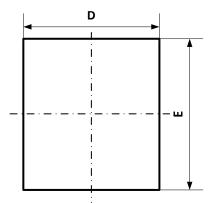
Fig. 2



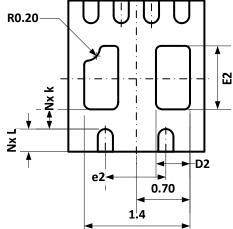
Mechanical Details

DFN2018P6E Package Diagrams

TOP VIEW



BOTTOM VIEW

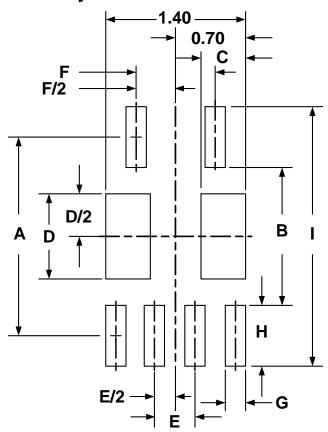


SIDE VIEW

Package Dimensions

Symbol	Millimeters				
	Min.	Nom.	Max.		
Α	0.51	0.55	0.60		
A 1	0.00	0.02	0.05		
b	0.15	0.20	0.25		
D	1.70	1.80	1.90		
E	1.90	2.00	2.10		
D2	0.30	0.45	0.55		
E2	0.69	0.84	0.94		
L	0.25	0.30	0.35		
k	0.20	-	-		
e1	0.40 BSC				
e2	0.80 BSC				
N	6				

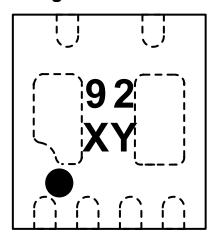
Land Layout



Dimensions			
Index	Millimeter		
Α	1.95		
В	1.35		
С	0.45		
D	0.84		
E	0.40		
F	0.80		
G	0.20		
Н	0.60		
I	2.55		

Notes: This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

Marking code



92 = Device Code X = Date Code; Y = Control Code

Part Number	Marking Code		
AZ4920-01F.R7G	92		
(Green Part)	XY		

Note: Green means Pb-free, RoHS, and Halogen free compliant.



Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ4920-01F.R7G	Green	T/R	7 inch	3,000/reel	4 reels = 12,000/box	6 boxes = 72,000/carton

Revision History

Revision	Modification Description			
Revision 2021/05/25	Formal Release.			