DPDT SWITCH GaAs MMIC

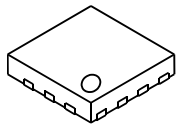
■ GENERAL DESCRIPTION

The NJG1657MD7 is a GaAs DPDT switch featured low insertion loss, high isolation and small size package, and suited for mobile terminal applications.

The NJG1657MD7 switches a path between common RF port and five RF ports by three bit control signal from 1.7V of logical high voltage. In addition, this switch includes ESD protection circuits for good ESD tolerance.

The NJG1657MD7 is available in a very small, lead-free, halogen-free, 1.6mm x 1.6mm x 0.397 mm, 14-pin EQFN14-D7 package.

■ PACKAGE OUTLINE



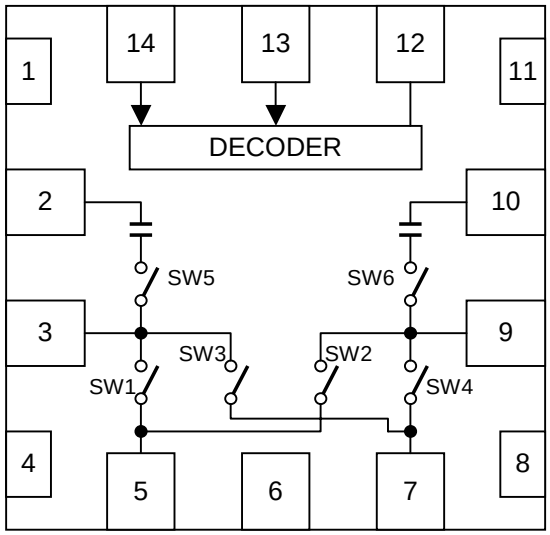
NJG1657MD7

■ FEATURES

● Low insertion loss	0.3dB typ. @f=0.9GHz, P_{IN}=30dBm
● High isolation	32dB typ. @f=0.9GHz, P_{IN}=30dBm
● High power handling	$P_{-0.1dB}$=33dBm min. @f=0.9GHz, V_{DD}=2.85V
● Package	EQFN14-D7 (Package size: 1.6x1.6x0.397mm typ.)

■ PIN CONFIGURATION

EQFN14-D7
(Top view)



Pin connection

1. GND	8. GND
2. GND	9. P2
3. P1	10. GND
4. GND	11. GND
5. P3	12. VDD
6. GND	13. CTL1
7. P4	14. CTL2

*Exposed PAD: GND

■ TRUTH TABLE

"High"=$V_{CTL(H)}$, "Low"=$V_{CTL(L)}$

PATH	CTL1	CTL2	SW1	SW2	SW3	SW4	SW5	SW6
P1-P3	Low	Low	ON	OFF	OFF	ON	OFF	ON
P1-P4	High	Low	OFF	ON	ON	OFF	OFF	ON
P2-P3	Low	High	OFF	ON	ON	OFF	ON	OFF
P2-P4	High	High	ON	OFF	OFF	ON	ON	OFF

NOTE: Please note that any information on this catalog will be subject to change.

■ ABSOLUTE MAXIMUM RATINGS

T_a=+25°C, Z_s=Z_l=50 ohm

PARAMETER	SYMBOL	CONDITIONS	CONDITIONS	UNITS
RF Input Power	P_{IN}	V_{DD}=2.85V, V_{CTL}=0/2.6V	36	dBm
Supply Voltage	V_{DD}	VDD terminal	5.0	V
Control Voltage	V_{CTL}	CTL1, CTL2 terminal	5.0	V
Power Dissipation	P_D	4-layer FR4 PCB with through-hole (74.2x74.2mm), T_j=150°C	1300	mW
Operating Temp.	T_{opr}		-40~+95	°C
Storage Temp.	T_{stg}		-55~+150	°C

■ ELECTRICAL CHARACTERISTICS1 (DC CHARACTERISTICS)

General conditions: V_{DD}=2.85V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=2.6V, T_a=+25°C, Z_S=Z_l=50 ohm, with application circuit

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage	V_{DD}		2.5	2.85	4.5	V
Operating Current	I_{DD}	P_{IN}=30dBm	-	50	100	μA
Control Voltage (LOW)	$V_{CTL(L)}$		0	-	0.5	V
Control Voltage (HIGH)	$V_{CTL(H)}$		1.7	2.6	4.5	V
Control Current	I_{CTL}		-	5	10	μA

■ **ELECTRICAL CHARACTERISTICS2** (RF CHARACTERISTICS)

General conditions: V_{DD}=2.85V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=2.6V, T_a=+25°C, Z_S=Z_l=50 ohm, with application circuit

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Loss 1	LOSS1	f=0.9GHz, P_{IN}=30dBm	-	0.30	0.45	dB
Insertion Loss 2	LOSS2	f=1.9GHz, P_{IN}=30dBm	-	0.40	0.55	dB
Isolation 1	ISL1	f=0.9GHz, P_{IN}=30dBm	30	32	-	dB
Isolation 2	ISL2	f=1.9GHz, P_{IN}=30dBm	24	26	-	dB
0.1dB Compression input power	$P_{-0.1dB}$	f=0.9GHz	33	35	-	dBm
2nd Harmonic Suppression	2fo	f=0.9GHz, P_{IN}=30dBm	-	-75	-60	dBc
3rd Harmonic Suppression	3fo	f=0.9GHz, P_{IN}=30dBm	-	-75	-60	dBc
VSWR (PC, P1, P2)	VSWR	f=0.9GHz, ON State	-	1.2	1.4	
Switching time	T_{SW}		-	2	5	μs

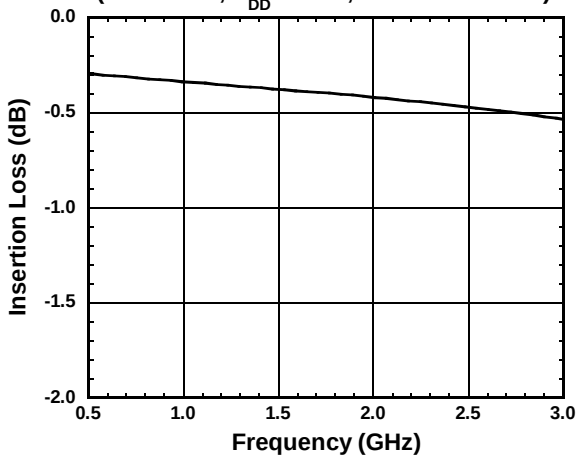
■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
1,2,4,6,8, 10,11	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
3	P1	RF input / output port. External capacitor is required to block the DC bias voltage of internal circuit.
5	P3	RF input / output port. External capacitor is required to block the DC bias voltage of internal circuit.
7	P4	RF input / output port. External capacitor is required to block the DC bias voltage of internal circuit.
9	P2	RF input / output port. External capacitor is required to block the DC bias voltage of internal circuit.
12	VDD	A supply voltage terminal (+2.5~+4.5V). Please place a bypass capacitor between this and GND for avoiding RF noise from outside.
13	CTL1	Control port. “High level” is DC +1.7V~4.5V, “Low level” is DC 0~+0.5V.
14	CTL2	

■ **ELECTRICAL CHARACTERISTICS** (With Application circuit, Loss of external circuit are excluded)

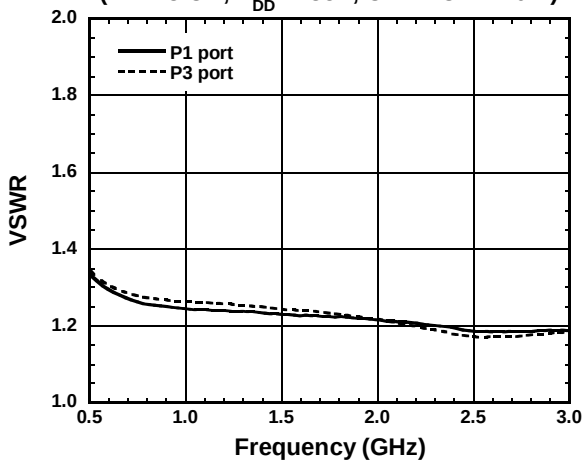
Insertion Loss vs. Frequency

(P1-P3 ON, V_{DD}=2.85V, CTL1=CTL2=0V)



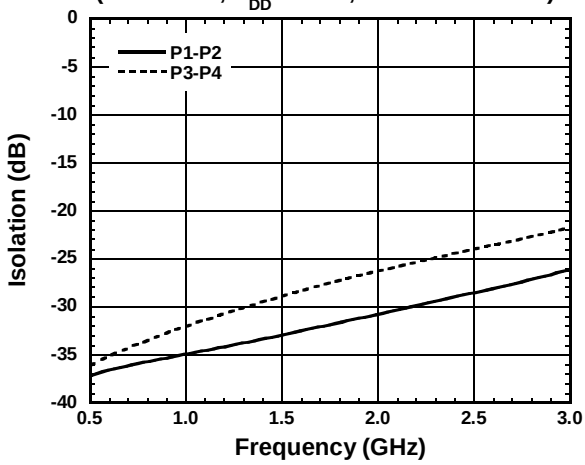
VSWR vs. Frequency

(P1-P3 ON, V_{DD}=2.85V, CTL1=CTL2=0V)



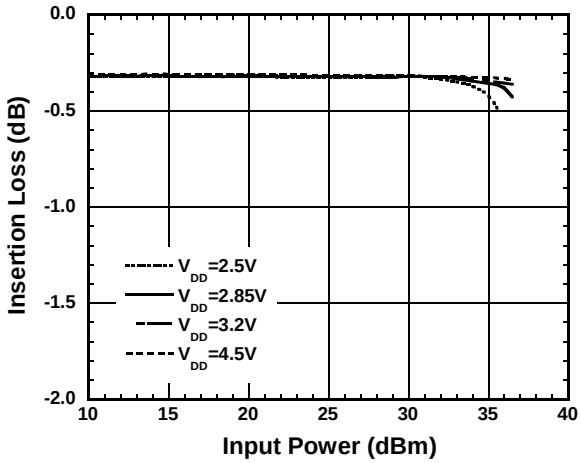
Isolation vs. Frequency

(P1-P3 ON, V_{DD}=2.85V, CTL1=CTL2=0V)



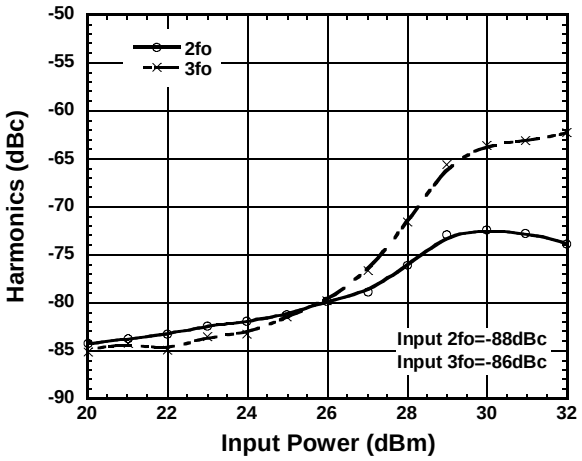
Insertion Loss vs. Input Power

(f=0.9GHz, P1-P3 ON, CTL1=CTL2=0V)



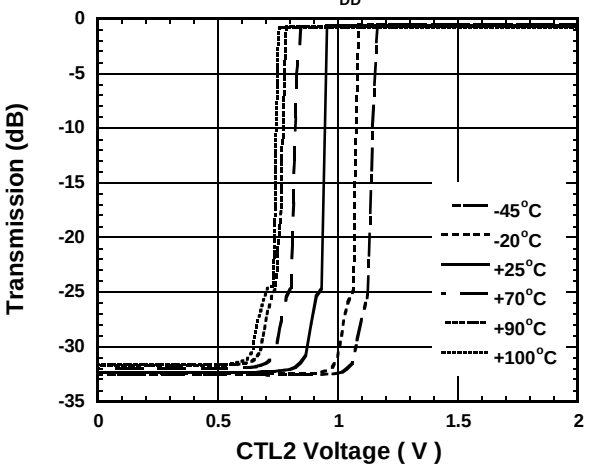
Harmonics vs. Input Power

(f=900MHz, P1-P3 ON, CTL1=CTL2=0V)



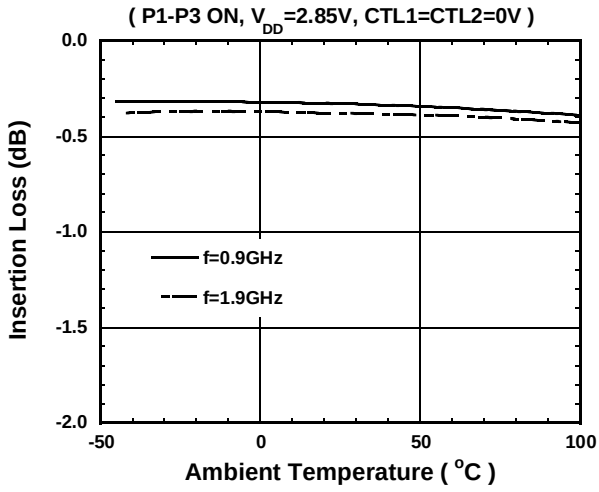
Transmission vs. Control Voltage

(P2-P4 ON, f=900MHz, V_{DD}=2.85V, CTL1=2.6V)

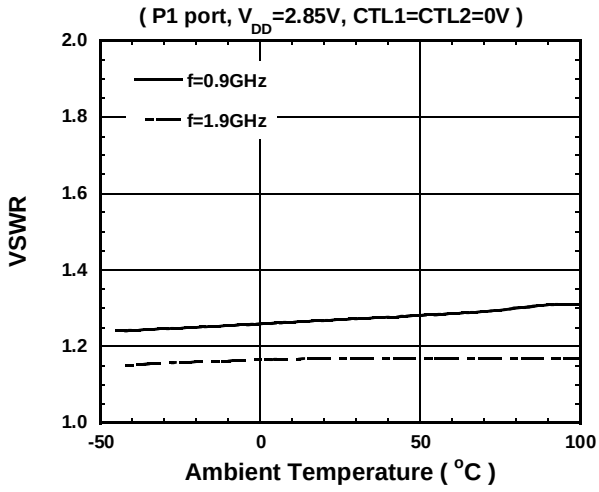


■ **ELECTRICAL CHARACTERISTICS** (With Application circuit, Loss of external circuit are excluded)

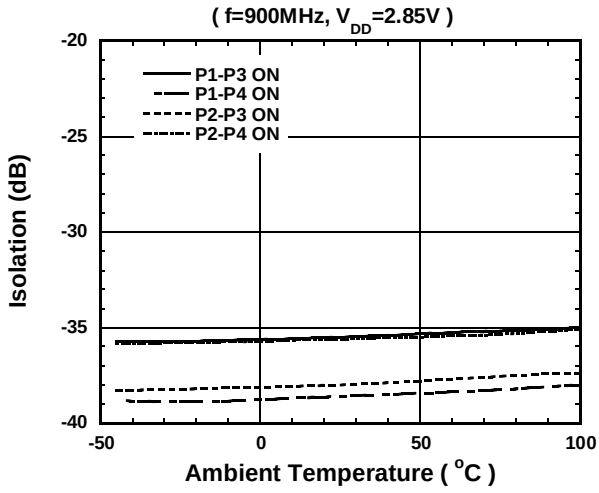
Insertion Loss vs. Ambient Temperature



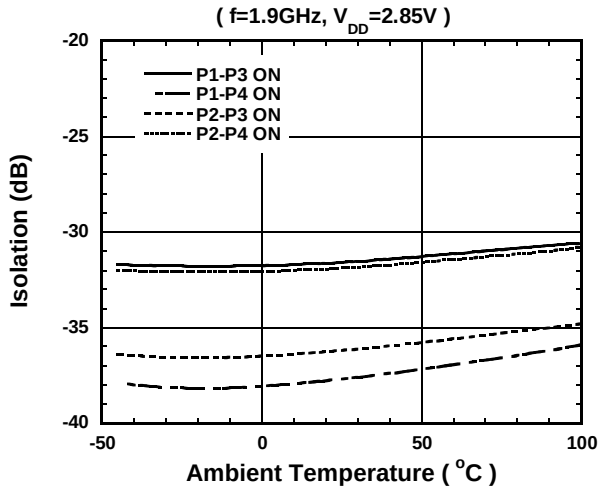
VSWR vs. Ambient Temperature



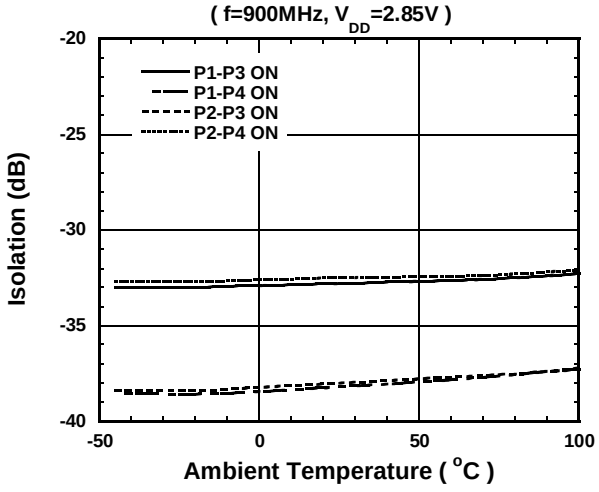
P1-P2 Isolation vs. Ambient Temperature



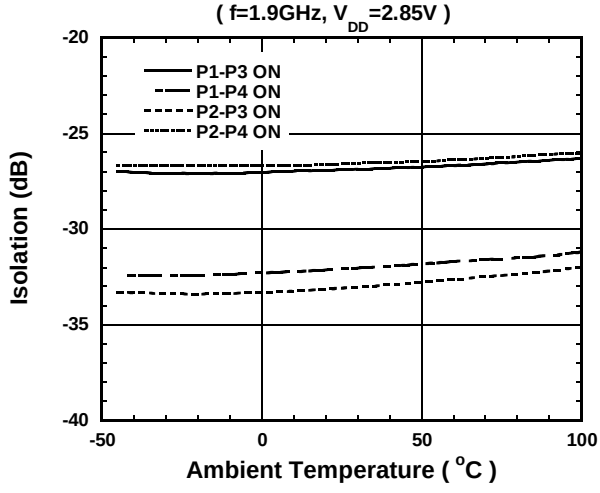
P1-P2 Isolation vs. Ambient Temperature



P3-P4 Isolation vs. Ambient Temperature



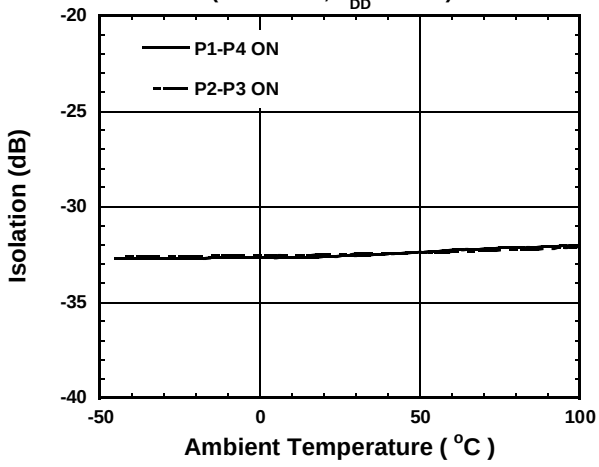
P3-P4 Isolation vs. Ambient Temperature



■ **ELECTRICAL CHARACTERISTICS** (With Application circuit, Loss of external circuit are excluded)

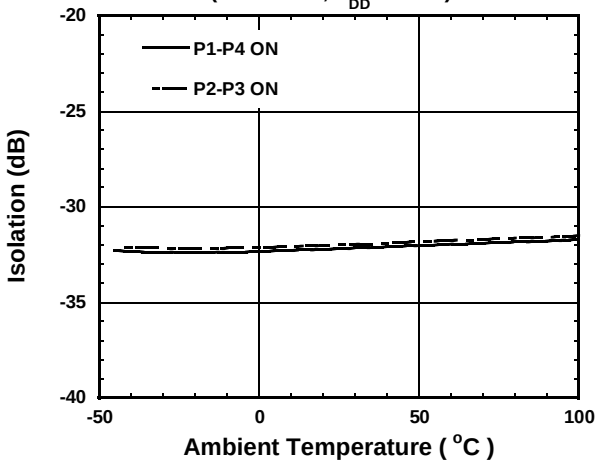
P1-P3 Isolation vs. Ambient Temperature

(f=900MHz, V_{DD}=2.85V)

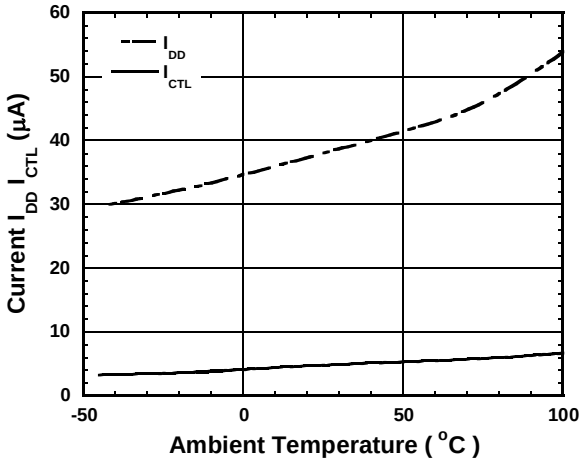


P2-P4 Isolation vs. Ambient Temperature

(f=900MHz, V_{DD}=2.85V)

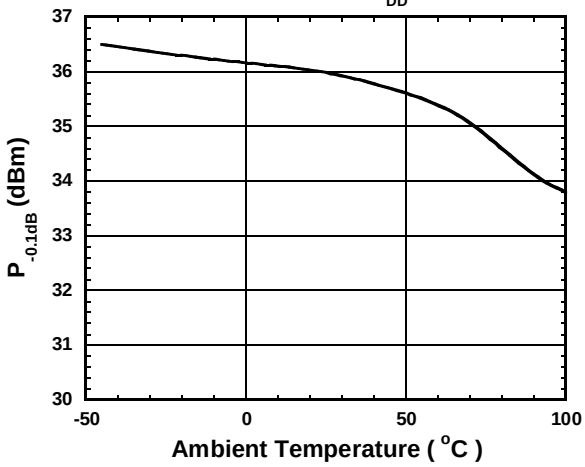


I_{DD}, I_{CTL} vs. Ambient Temperature



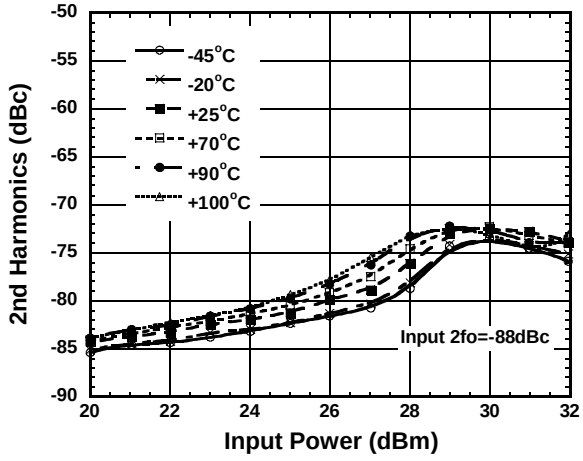
$P_{-0.1dB}$ vs. Ambient Temperature

(f=0.9GHz, P1-P3 ON, V_{DD}=2.85V)



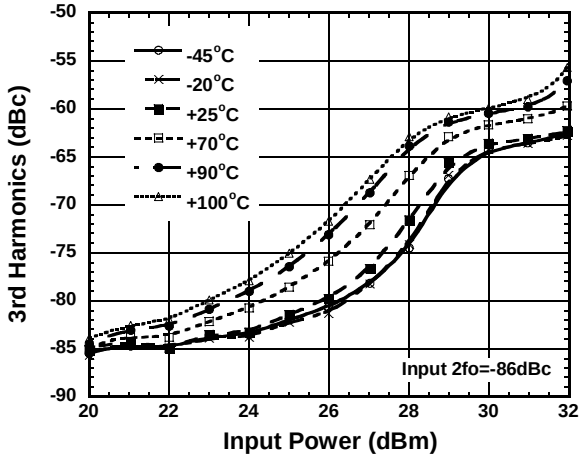
2nd Harmonics vs. Input Power

(f=900MHz, P1-P3 ON, CTL1=CTL2=0V)



3rd Harmonics vs. Input Power

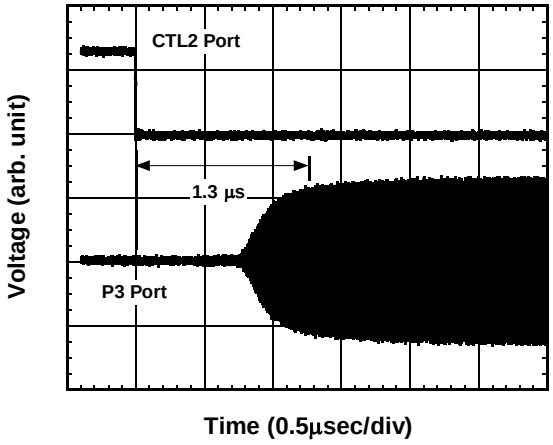
(f=900MHz, P1-P3 ON, CTL1=CTL2=0V)



■ **ELECTRICAL CHARACTERISTICS** (With Application circuit, Loss of external circuit are excluded)

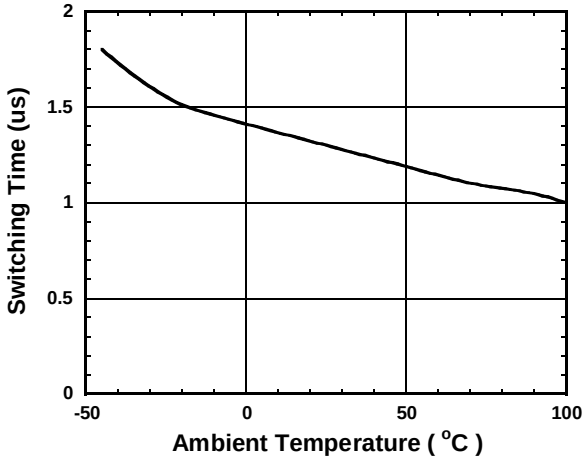
Switching Time

(V_{DD}=2.85V, CTL1=0V)



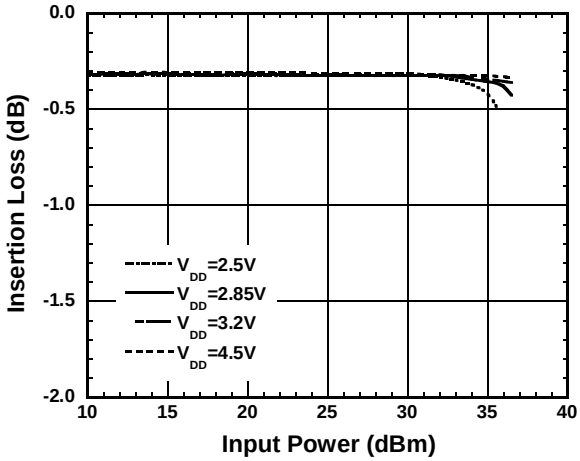
Switching Time vs. Ambient Temperature

(V_{DD}=2.85V)



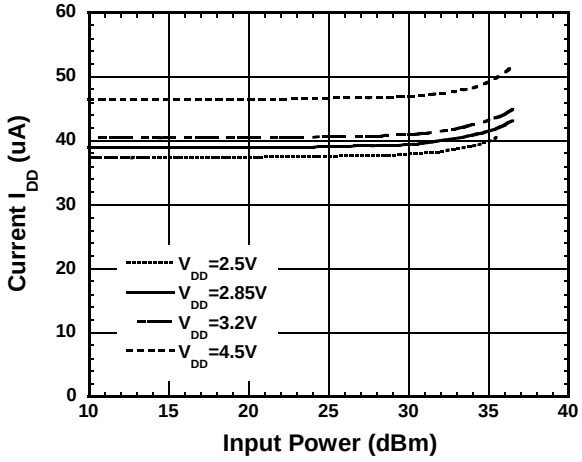
Insertion Loss vs. Input Power

(f=0.9GHz, P1-P3 ON, CTL1=CTL2=0V)

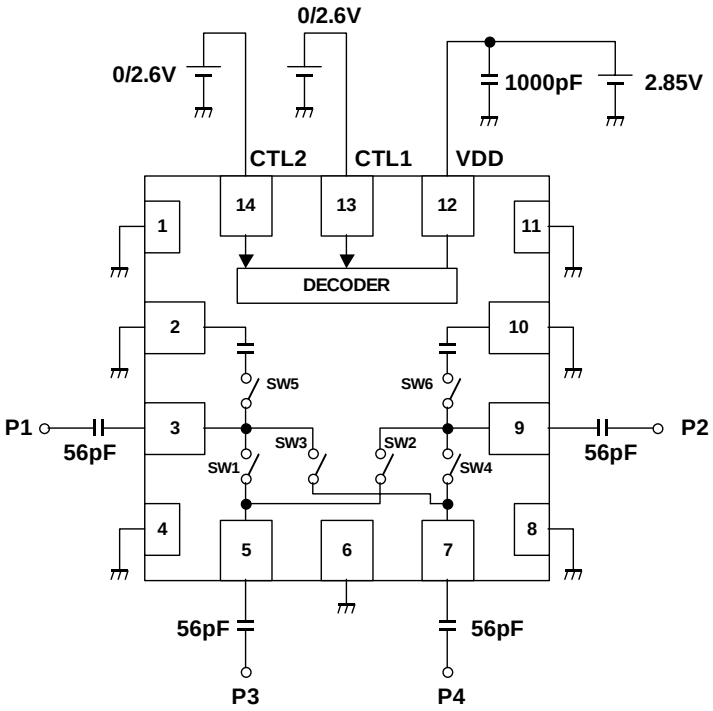


Current I_{DD} vs. Input Power

(f=0.9GHz, P1-P3 ON, CTL1=CTL2=0V)

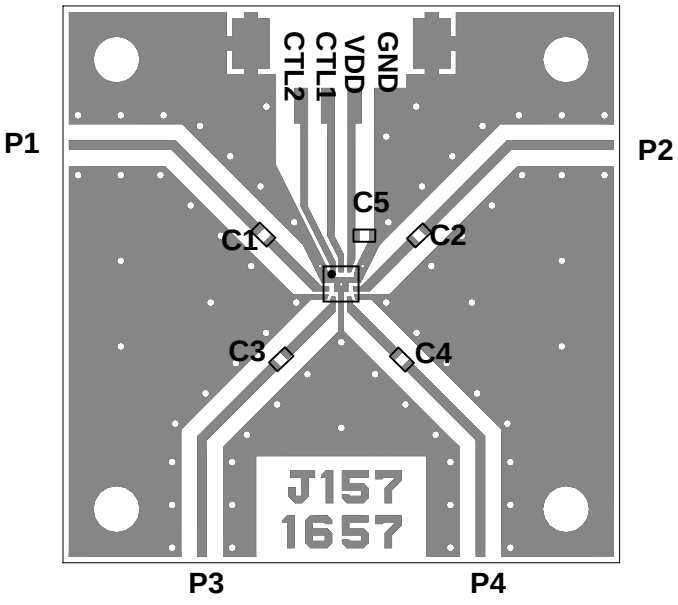


■ APPLICATION CIRCUIT



■ TEST PCB LAYOUT

(TOP VIEW)



PCB: FR-4, t=0.2mm

Capacitor size: 1005

Strip Line Width: 0.4mm

PCB size: 26 x 26mm

Losses of PCB, capacitors and connectors

Frequency (GHz)	Loss (dB)
0.9	0.30
1.9	0.49

PARTS LIST

PART ID	Value	COMMENT
C1~C4	56pF	MURATA (GRM15)
C5	1000pF	

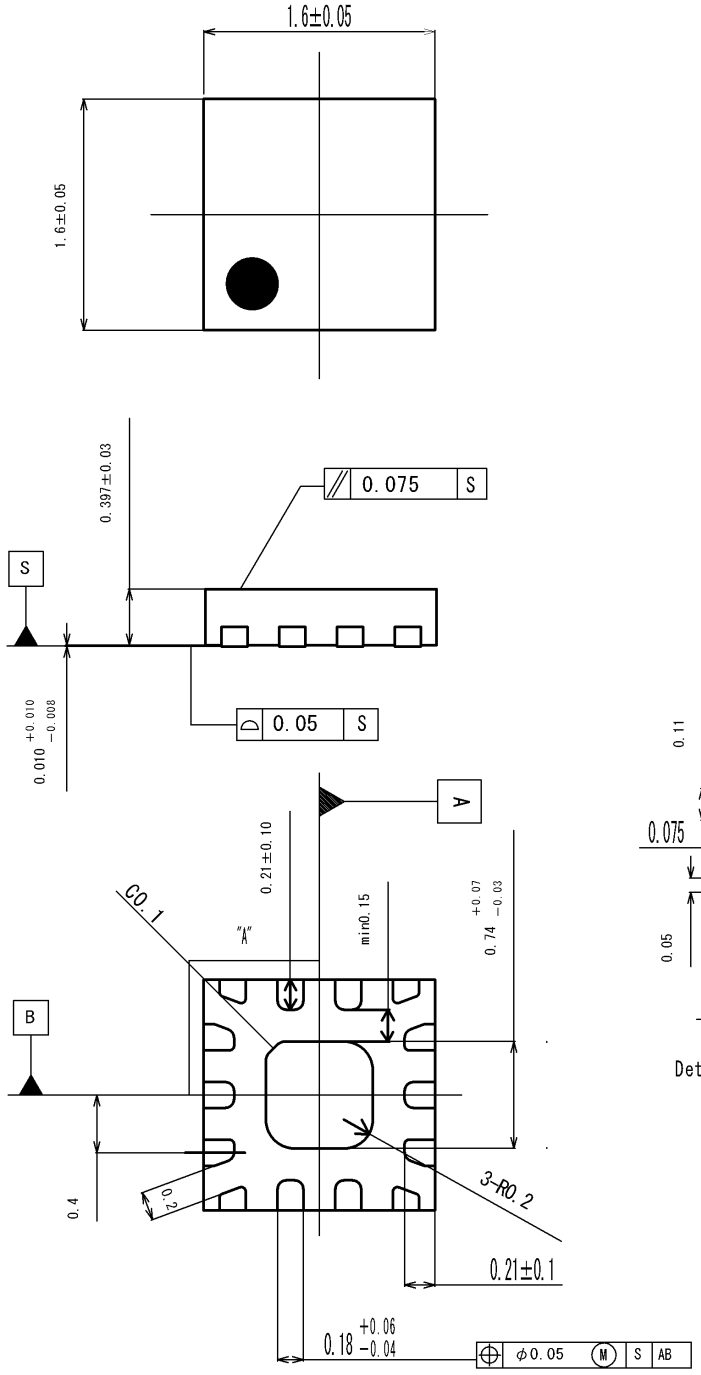
PRECAUTIONS

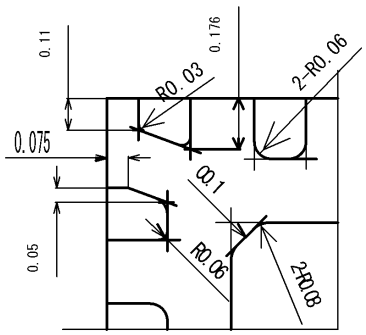
[1]The DC blocking capacitors have to be placed at RF terminal of P1, P2, P3, P4 and PC. Please choose appropriate capacitance values to the application frequency.

[2]To reduce strip line influence on RF characteristics, please locate bypass capacitors(C5) as close as possible to each terminals.

[3]For good isolation, the GND terminal must be connected to the ground plane of substrate, and through-holes for GND should be placed near by the pin connection.

■ PACKAGE OUTLINE (EQFN14-D7)





Details of"A" part (× 2)

UNIT : mm

SUBSTRATE MATERIAL : Copper
TERMINAL FINISH : Sn-Bi plating
MOLDE MATERIAL : Epoxy resin
MASS (TYP.) : 0.0034 (g)

Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.