

SPECIFICATION

PART NO. : TOD9M0053-Y-E-V1



This specification maybe changed without any notice in order to improve performance or quality etc.

Please contact TRULY Semiconductors LTD. OLED R&D department for update specification and product status before design for this product or release the order.

PRODUCT CONTENTS

- PHYSICAL DATA
- ABSOLUTE MAXIMUM RATINGS
- EXTERNAL DIMENSIONS
- ELECTRICAL CHARACTERISTICS
- TIMING OF POWER SUPPLY
- ELECTRO-OPTICAL CHARACTERISTICS
- INTERFACE PIN CONNECTIONS
- COMMAND TABLE
- INITIALIZATION CODE
- SCHEMATIC EXAMPLE
- RELIABILITY TESTS
- OUTGOING QUALITY CONTROL SPECIFICATION
- CAUTIONS IN USING OLED MODULE

TRU	/LY®信利	Customer	
Written by	Hujiabin	App	roved by
Checked by	Zhangweicang		
Approved by	Sujunhai		

REVISION HISTORY

Rev.	Contents	Date
0.0	Preliminary	2008-7-26



■ PHYSICAL DATA

No.	Items:	Specification:	Unit
1	Diagonal Size	1.6	Inch
2	Resolution	128(H) x 64(V)	Lines
3	Active Area	36.45 (W) x 18.21(H)	mm
4	Outline Dimension (Panel)	46.83 (W) x 28.77(H)	mm
5	Pixel Pitch	0.285 (W) x 0.285 (H)	mm
6	Pixel Size	0.255 W) x 0.255(H)	mm
7	Driver IC	SSD1325T6R1	-
8	Display Color	Yellow	-
9	Grayscale	4	Bit
10	Interface	Parallel	-
11	IC package type	TCP	-
12	Thickness	2.1±0.1	mm
13	Weight	TBD	g
14	Duty	1/64	-

■ ABSOLUTE MAXIMUM RATINGS

Unless otherwise specified, $V_{SS} = 0V$

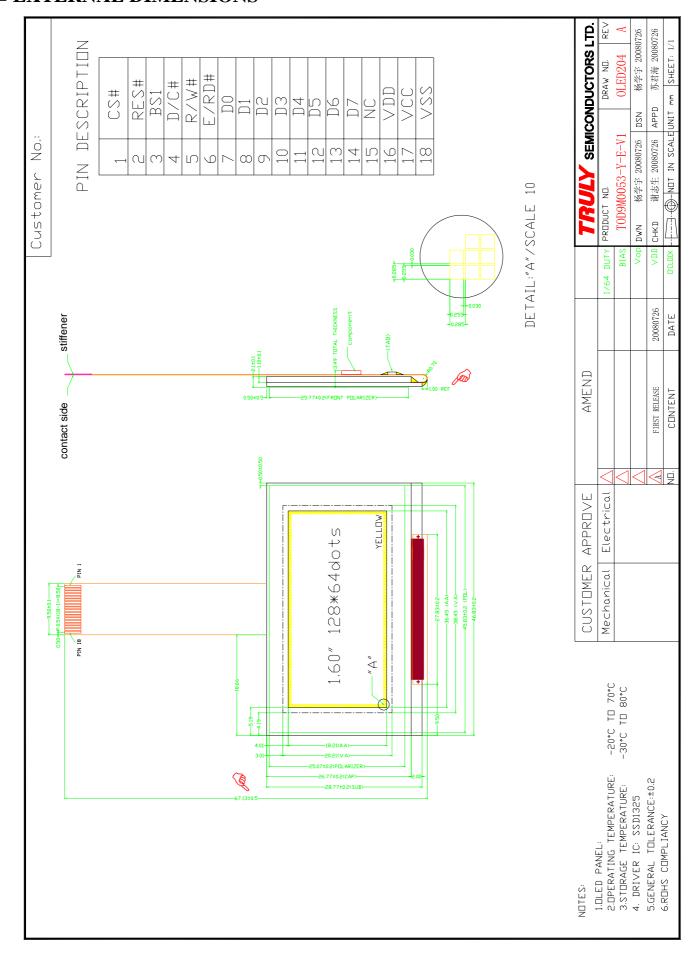
 $(Ta = 25^{\circ}C)$

Ite	ems	Symbol	Min	Тур.	Max	Unit
Supply	Logic	$V_{ m DD}$	-0.3	-	4.0	V
Voltage	Driving	V_{CC}	0	-	17.0	V
Operating Temperatur	re	Тор	-20	-	70	${\mathbb C}$
Storage Te	mperature	Tst	Tst -30 -		80	${\mathbb C}$
Humidity		-	-	-	90	%RH

NOTE:

Permanent device damage may occur if **ABSOLUTE MAXIMUM RATINGS** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ EXTERNAL DIMENSIONS



■ ELECTRICAL CHARACTERISTICS

♦DC Characteristics

Unless otherwise specified, $V_{SS} = 0V$, $V_{DD} = 2.4V$ to 3.5V (Ta = 25°C)

	Items	Symbol	Min	Typ.	Max	Unit
Supply	Logic	$V_{ m DD}$	2.4	3.0	3.5	V
Voltage	Operating	V_{CC}	8.0	13.0	16.0	V
Input	High Voltage	V_{IH}	$0.8 \times V_{DD}$	-	$ m V_{DD}$	V
Voltage	Low Voltage	V_{IL}	V_{SS}	-	$0.2 \times V_{DD}$	V
Output	High Voltage	V_{OH}	0.9 x V _{DD}	-	$V_{ m DD}$	V
Voltage	Low Voltage	V_{OL}	V_{SS}	-	0.1 x V _{DD}	V



◆AC Characteristics

Use 8080/6800-Series MPU Parallel Interface 1:6800 Series MPU Parallel Interface

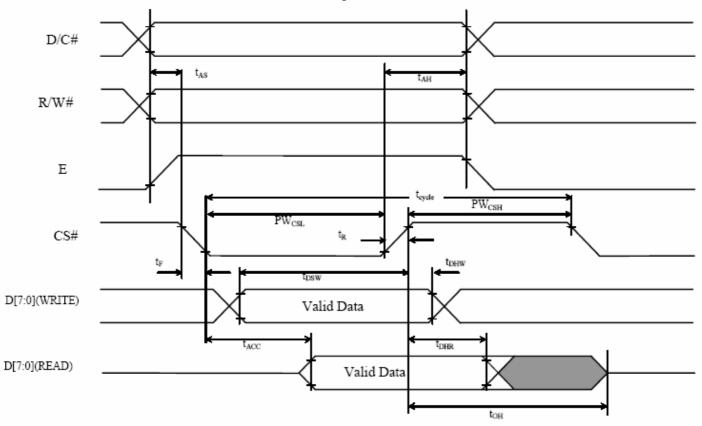
Conditions:

$$V_{DD} \sim V_{SS} = 2.4$$
 to $3.5V$
 $T_A = 25$ °C

6800-Series MPU Parallel Interface Timing Characteristics

Symbol	Parameter	Min	Тур	Max	Unit
t _{cycle}	Clock Cycle Time	300	-	-	ns
tAS	Address Setup Time	0	-	-	ns
t _{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
tDHR	Read Data Hold Time	20	-	-	ns
toH	Output Disable Time	-	-	70	ns
t _{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read)	120	-	-	ns
	Chip Select Low Pulse Width (write)	60			
PWcsh	Chip Select High Pulse Width (read)	60	-	-	ns
	Chip Select High Pulse Width (write)	60			
t_R	Rise Time	-	-	15	ns
tF	Fall Time	-	-	15	ns

6800-series MPU parallel interface characteristics



Jul.26, 2008

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2:8080 Series MPU Parallel Interface

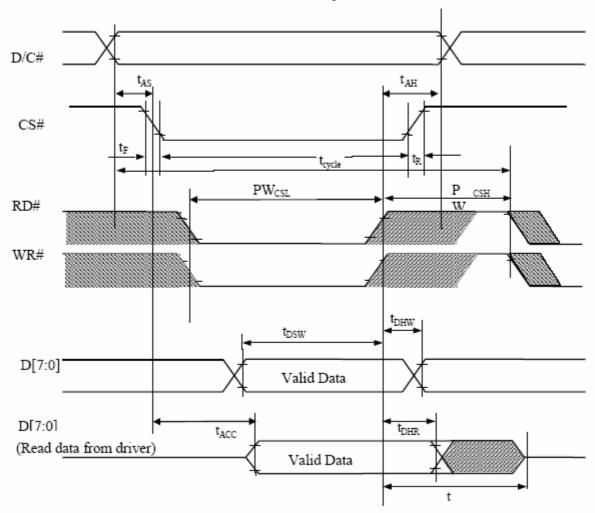
Conditions:

$$V_{DD} \sim V_{SS} = 2.4$$
 to $3.5V$
 $T_A = 25$ °C

8080-Series MPU Parallel Interface Timing Characteristics

Symbol	Parameter	Min	Тур	Max	Unit
t _{cycle}	Clock Cycle Time	300	-	-	ns
t _{AS}	Address Setup Time	0	-	-	ns
t _{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
tDHR	Read Data Hold Time	20	-	-	ns
t _{OH}	Output Disable Time	-	-	70	ns
tACC	Access Time	-	-	140	ns
PWcsl	Chip Select Low Pulse Width (read)	120	-	-	ns
	Chip Select Low Pulse Width (write)	60			
PW_{CSH}	Chip Select High Pulse Width (read)	60	-	-	ns
	Chip Select High Pulse Width (write)	60			
t_R	Rise Time	-	-	15	ns
tF	Fall Time	-	-	15	ns

8080-series MPU parallel interface characteristics





■ TIMING OF POWER SUPPLY

The following figures illustrate the recommended power ON and power OFF sequence of SSD1325. Power ON sequence:

- Power ON V_{DD}
- 2. After VDD become stable, set RES# pin LOW (logic LOW) for at least 3us (t1) and then HIGH (logic HIGH).
- After set RES# pin LOW (logic LOW), wait for at least 3us (t2). Then Power ON VCC.
- 4. After VCC become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}) .

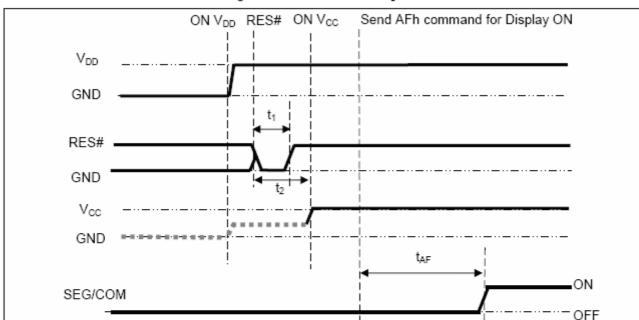


Figure 1 : The Power ON sequence

Power OFF sequence:

- Send command AEh for display OFF.
- 2. Wait until panel discharges completely. 3. Power OFF $V_{\text{CC.}}^{(1),\,(2)}$
- Wait for t_{OFF}. Power OFF V_{DD}. (where Minimum t_{OFF}=0ms, Typical t_{OFF}=100ms)

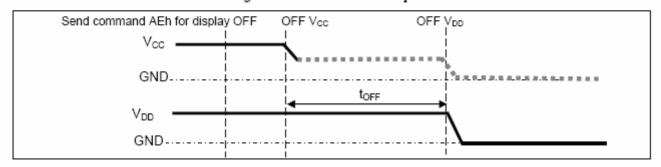


Figure 2: The Power OFF sequence

Note:

 $^{(1)}$ Since an ESD protection circuit is connected between V_{DD} and V_{CC} , V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 1 and Figure 2.

(2) VCC should be kept float when it is OFF.

■ ELECTRO-OPTICAL CHARACTERISTICS (Ta=25°C)

Items		Symbol	Min.	Тур.	Max.	Unit	Remark	
Operating Lum	ninance	L	70	80*	-	cd/m ²	Yellow	
Power Consur	nption	P	_	80	100	mW	30% pixels ON	
	r · ·						L=80cd/m ²	
Frame Frequ	ency	Fr	-	100	-	Hz		
Color Coordinate	YELLOW	CIE x	0.41	0.46	0.51	CIE1931	Darkroom	
Color Coordinate	I ELLO W	CIE y	0.46	0.51	0.56	CIE1931	Darkfoolii	
Dognongo Timo	Rise	Tr	-	-	0.02	ms	-	
Response Time	Decay	Td	-	-	0.02	ms	-	
Contrast Ra	tio*	Cr	10000:1	-	-		Darkroom	
Viewing Angle U	niformity	Δ θ	160	_	-	Degree	-	
Operating Life	Time*	Тор	100,000	-	-	Hours	L=80cd/m ²	

Note:

- 1. **80cd/m²** is base on V_{DD} =3.0V, V_{PP} =13.0V, contrast command setting 0x40;
- 2. Contrast ratio is defined as follows:

Contrast ratio = Photo – detector output with OLED being "white"

Photo – detector output with OLED being "black"

3. **Life Time** is defined when the Luminance has decayed to less than 50% of the initial Luminance specification. (30% pixels scrolling display on)

(The initial value should be closed to the typical value after adjusting.)



■ INTERFACE PIN CONNECTIONS

No	Symbol	Description							
1	CS#	The chip select pin. Low is enabled							
2	RES#	This pin is reset signal input.							
3	BS1	It is the MPU interface switched pad(L:6800; H:8080)							
4	D/C#	Data/Command data control pin							
5	W/R#	MCU interface input pin							
6	E/RD#	MCU interface input pin							
7	D0								
8	D1								
9	D2								
10	D3	Data has (Danallal Intenface)							
11	D4	Data bus (Parallel Interface)							
12	D5								
13	D6								
14	D7								
15	NC	No connecting							
16	VDD	Logic voltage supply for IC							
17	VCC	High voltage supply for OLED panel							
18	VSS	Ground							

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■ COMMAND TABLE

(D/C# = 0, R/W# (WR#) = 0, E (RD#) = 1) unless specific setting is stated

Fund	amental	Co	mm	and	Tab	le					
D/C	Hex	D 7	D6	D5	D4	D3	D2	D1	$\mathbf{D}0$	Command	Description
0	15	0	0	0	1	0	1	0	1	Set Column Address	Second command A[5:0] sets the column start address
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		from 0-63, POR = 00h
0	B[5:0]	*	*	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		Third command B[5:0] sets the column end address from 0-63, RESET = 3Fh
0	75	0	1	1	1	0	1	0	1	Set Row address	Second command A[6:0]sets the row start address from
0	A[6:0]	*					A_2				0-79, RESET = 00h
0	B[6:0]	*	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		Third command B[6:0] sets the row end address from 0- 79, RESET = 4Fh
0	81	1	0	0	0	0	0	0	1	Set Contrast Current	Double byte command to select 1 out of 128 contrast
0	A[6:0]	*	A_6	A_5	A_4	A3	A_2	A_1	A ₀		steps. Contrast increases as level increase
											The level is set to 40h after RESET
0	84~86	1	0	0	0	0	1	X_1	X_0	Set Current Range	84h = Quarter Current Range (RESET)
											85h = Half Current Range
											86h = Full Current Range
0	A0	1	0	1	0	0	0	0	0	Set Re-map	A[0]=0, Disable Column Address Re-map (RESET)
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0	_	A[0]=1, Enable Column Address Re-map
											A[1]=0, Disable Nibble Re-map (RESET)
											A[1]=1, Enable Nibble Re-map
											A[2]=0, Horizontal Address Increment (RESET)
											A[2]=1, Vertical Address Increment
											A(4)=0 Disable COM Be area disable (BESET)
											A[4]=0, Disable COM Re-map disable (RESET) A[4]=1, Enable COM Re-map
											A[+j-1, Enable COM Re-map
											A[5]=0, Reserved (RESET)
											A[5]=1, Reserved
											A[6]=0, Disable COM Split Odd Even (RESET)
											A[6]=1, Enable COM Split Odd Even
0	A1	1	0	1	0	0	0	0	1	Set Display Start Line	Set display RAM display start line register from 0-79
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	ı		Display start line register is reset to 00h after RESET
0	A2	1	0	1	0	0	0	1	0	Set Display Offset	Set vertical scroll by COM from 0-79
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		The value is reset to 00H after RESET
0	A4~A7	1	0	1	0	0	X_2	X_1	\mathbf{X}_0	Set Display Mode	A4h = Normal Display (RESET)
											A5h = Entire Display ON,



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D/C	Hex	D7	D 6	D5	D4	D3	D2	Dl	D0	Command	Description
											all pixels turns ON in GS level 15
											A6h = Entire Display OFF, all pixels turns OFF
											A7h = Inverse Display
0	A8 A[6:0]	1 *	0 A ₆	1 A ₅	0 A4	1 A ₃	0 A ₂	0 A ₁	ı	Set Multiplex Ratio	The next command determines multiplex ratio N from 16MUX-80MUX, A[6:0] = 15 represents 16MUX A[6:0] = 16 represents 17MUX
											A[6:0] = 78 represents 79MUX A[6:0] = 79 represents 80MUX
0	AD A[1:0]	1 *	0	1 *	0	1 *	1 *	0		Set Master Configuration	A[0] = 0, Select external V _{CC} supply A[0] = 1, Reserved (RESET)
											Note (1) Bit A[0] must be set to 0b after RESET. (2) The setting will be activated after issuing Set Displa ON command (AFh)
0	AE	1	0	1	0	1	1	1	0	Set Display ON	AEh = Display OFF (Sleep mode) (RESET)
0	AF	1	0	1	0	1	1	1	1	Set Display OFF	AFh = Display ON
0	В0	1	0	1	1	0	0	0		Set Pre-charge Compensation Enable	A[5:0] = 08h (RESET)
0	A[5:0]	*	*	A5	A4	A ₃	A ₂	Aı	ı		A[5:0] = 28h, Enable pre-charge compensation
0	B1 A[3:0]	1	0	1	1	0	0	0	ı	Set Phase Length	A[3:0] = P1, phase 1 period of 1-15 DCLKs, RESET = 3DCLKS = 3h
0	A[5:0] A[7:4]		A ₆		A_4	A ₃	*	A ₁	A ₀		A[7:4] = P2, phase 2 period of 1-15 DCLKs, RESET = 5DCLKS = 5h
											Note ⁽¹⁾ 0 DCLK is invalid in phase 1 & phase 2
0	B2 A[7:0]	1 A ₇	0 A ₆	1 A ₅	1 A ₄	0 A ₃	0 A ₂	1 A ₁	ı	Set Row Period (set frame frequency)	The next command sets the number of DCLKs, K, per row between 2-158 DCLKS RESET = 37DCLKS = 25h The K value should be set as K = P1+P2+GS15 pulse width (RESET: 3+5+29DCLKS)
0 0 0	B3 A[3:0] A[7:4]		0 * A ₆	1 * A ₅	1 * A4	0 A ₃ *	0 A ₂ *	1 A ₁ *	A_0	Set Display Clock Divide Ratio / Oscillator Frequency	The lower nibble (A[3:0]) of the next command define the divide ratio (D) of display clock (DCLK) Divide ratio (D)=A[3:0]+1 (A[3:0]RESET is 0001b, i.e. divide ratio (D) = 2)



D/C	amental Hex					D3	D2	ים	DΛ	Command	Diti
D/C	Hex	D 7	D6	D5	D4	D3	D2	DΙ	D0	Command	Description
											The higher nibble (A[7:4]) of the next command sets
											the Oscillator Frequency
											Oscillator Frequency increases with the value of A[7:4] and vice versa
											Range: 0000b~1111b
											RESET= 0100b represents 655KHz,
											typical step value: 5% of previous value
											yp-a
0	B4	1	0	1	1	0	1	0	0	Set Pre-charge	A[2:0] = 0 (RESET)
0	A[2:0]	*	*	*	*	*	A_2	A_1	A_0	Compensation Level	A[2:0] = 3h, Recommended level
	. ,						_	•	,	•	
0	B8	1	0	1	1	1	0	0	0	Set Gray Scale Table	The next eight bytes of command set the gray scale leve
0	A[2:0]	*	*	*	*	*	A_2	A_1	A_0		of GS1-15 as below:
0	B[2:0]	*	*	*	*	*	B_2	B_1	\mathbf{B}_0		A[2:0] = Gray scale level of GS1, RESET=1
0	B[6:4]	*	B ₆	B ₅	B ₄	*	*	*	*		B[2:0] = Gray scale level of GS2, RESET=1
0	C[2:0]	*	*	*	*	*	C_2	C_1	C ₀		B[6:4] = Gray scale level of GS3, RESET=1
0	C[6:4]	*	C ₆	C ₅	C ₄	*	*	*	*		C[2:0] = Gray scale level of GS4 RESET=1
0	D[2:0]	*	*	*	*	*		D_1	D_0		C[6:4] = Gray scale level of GS5, RESET=1
- 1	1	*				*	D ₂	ν ₁	±0		D[2:0] = Gray scale level of GS6, RESET=1
0	D[6:4]		D ₆		D ₄						D[6:4] = Gray scale level of GS7, RESET=1
0	E[2:0]	*	*	*	*	*	E_2	E ₁	E ₀		E[2:0] = Gray scale level of GS8, RESET=1
0	E[6:4]	*	E_6	E_5	E ₄	*	*	*	*		E[6:4] = Gray scale level of GS9, RESET=1
0	F[2:0]	*	*	*	*	*	F_2	F_1	F_0		F[2:0] = Gray scale level of GS10, RESET=1 F[6:4] = Gray scale level of GS11, RESET=1
0	F[6:4]	*	F_6	F_5	F ₄	*	*	*	*		G[2:0] = Gray scale level of GS11, RESET=1
0	G[2:0]	*	*	*	*	*	G_2	G_1	G_0		G[6:4] = Gray scale level of GS13, RESET=1
0	G[6:4]	*	G ₆	G ₅	G ₄	*	*	*	*		H[2:0] = Gray scale level of GS14, RESET=1
0	H[2:0]	*	*	*	*	*	H_2	H_1	H_0		H[6:4] = Gray scale level of GS15, RESET=1
0	H[6:4]	*	H ₆	H ₅	H ₄	*	*	*	*		
Ĭ	11[0.1]		0	,							
0	BC	1	0	1	1	1	1	0	0	Sat Pracharga Voltaga	Second command A[7:0] sets the precharge voltage
- 1		_	_	- 1	I -	_	-	-	_	Set Frecharge Voltage	level.
0	A[7:0]	A/	Αo	AD	A4	Аэ	A.Z	ΑI	ΑU		A[7:0] 1xxxxxxx connects to V _{COMH} (RESET)
											001xxxxx 1.0 * V _{REF}
											00000000 0.51* V _{REF}
											00000001 0.52* V _{REF}
											00011111 0.84* V _{REF}
_			_		_	_	_		_		
0	BE	1	0	1	1	1	1	1		Set V _{COMH} Voltage	Second command A[4:0] sets the V _{COMH} voltage level
0	A[4:0]	*	*	0	A4	A3	A2	A1	A0		A[4:0] 00000 0.51*V _{REF} 00001 0.52* V _{REF}
											00001 0.32 V REF
											11101 0.81* V _{REF} (RESET)
											11110 0.82* V _{REF} (RESE1)
											11111 0.84* V _{REF}
											- PAR
0	BF	1	0	1	1	1	1	1	1	Set Segment Low	Second command A[3:0] sets the VSL voltage as
0	A[3:0]	*	*	*	*	A	Αa	Αı	A٥	Voltage (VSL)	follow:
-	-[]					,	2	1		- , ,	A[3:0] = 0010 kept VSL pin NC
											A[3:0] = 1110 (RESET) connect a capacitor between
											VSL pin and V _{SS}
_		_	_		_	_	_		_	1.0P	
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No Operation

Rev: 0.0 Jul.26, 2008

♦ Read command table

(D/C#=0, R/W#(WR#)=1, E(RD#)=1 for 6800 or E(RD#)=0 for 8080)

(D/O#=0, N/V#(VVN#)=1, E(ND#)=1 101 0000 01 E(ND#)=0 101 0000)				
D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀	Status Register Read	D7 = 0:reserved		
		D7 = 1:reserved		
		D6 = 0:indicates the display is ON		
		D6 = 1:indicated the display is OFF		
		D5 = 0:reserved		
		D5 = 1:reserved		
		D4 = 0:reserved		
		D4 = 1:reserved		

Note: Patterns other than that given in Command Table are prohibited to enter to the chip as a command; Otherwise, unexpected result will occur

■ INITIALIZATION CODE

```
Void init oled()
  W COMMAND(0x15); //SET COLUMN ADDRESS
   W COMMAND(0x00);
   W COMMAND(0x3F);
   W COMMAND(0x75); //SET ROW ADDRESS
   W COMMAND(0x00);
   W COMMAND(0x3F);
   W COMMAND(0x81); //SET CONTRAST CURRENT
   W COMMAND(0x40);
  W COMMAND(0x86); //SET CURRENT RANGE
  W COMMAND(0xA0); //SET RE MAP
   W COMMAND(0x52);
  W COMMAND(0xA1); //SET DISPLAY START LINE
  W COMMAND(0x00);
  W COMMAND(0xA2); //SET DISPLAY OFFSET
  W COMMAND(0x40);
  W COMMAND(0xA4); //SET DISPLAY MODE(A4:NORMAL,A5:ENTIRE ON,A6:ENTIRE
                         OFF, A7: INVERSE)
  W COMMAND(0xA8); //SET MULTIPLEX RATIO
   W COMMAND(0x3F); //16--80
  W COMMAND(0xAD); //SET MASTER CONFIGURATION
   W COMMAND(0x02); //select external vcc supply
  W COMMAND(0xB0); //SET PRE-CHARGE COMPENSATION ENABLE
   W COMMAND(0x28); //28,ENABLE PRE-CHARGE COMPENSATION
   W COMMAND(0xB1); //SET PHASE LENGTH
   W COMMAND(0x23);
   W COMMAND(0xB2); //SET ROW PERIOD(FRAME FREQUENCY)
   W COMMAND(0x46); //K=P1+P2+GS15 PULSE WIDTH
  W COMMAND(0xB3); //SET DISPLAY CLOCK DIVIDE RATIO/OSCILLATOR FREQUENCY
   W COMMAND(0x40); \frac{1}{655}KHz,D=2
   W COMMAND(0xB4); //SET PRE-CHARGE COMPENSATION LEVEL
   W COMMAND(0x03);
   W COMMAND(0xB8); //SET GRAY SCALE TABLE
   W COMMAND(0x01); //GS1
   W COMMAND(0x11); //GS3GS2
   W COMMAND(0x22); //GS5GS4
```

```
W_COMMAND(0x32); //GS7GS6
W_COMMAND(0x43); //GS9GS8
W_COMMAND(0x54); //GS11GS10
W_COMMAND(0x65); //GS13GS12
W_COMMAND(0x76); //GS15GS14

W_COMMAND(0xBC); //SET PRE-CHARGE VOLTAGE
W_COMMAND(0x1F);

W_COMMAND(0xBE); //SET VCOMH VOLTAGE
W_COMMAND(0x13);

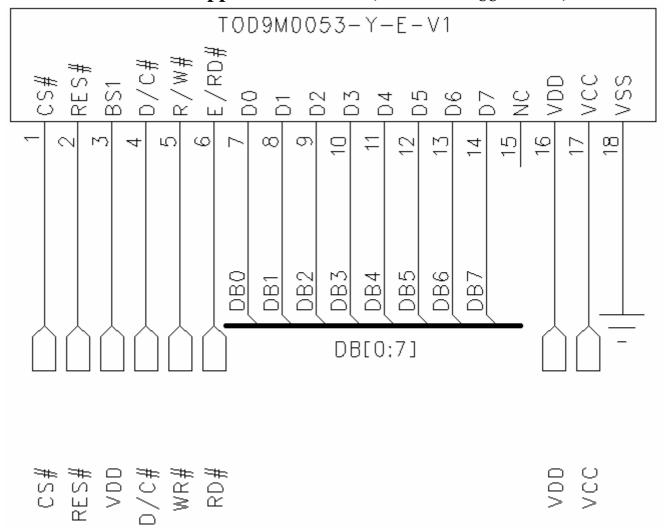
W_COMMAND(0xBF); //SET SEGMENT LOW VOLTAGE(VSL)
W_COMMAND(0x0E);

W_COMMAND(0xAF); //DISPLAY ON
```

}

■ SCHEMATIC EXAMPLE

\spadesuit8080 Series Interface Application Circuit(External V_{CC} =13.0V):



NOTE:

- 1. Pins connected to MPU interface: CS#、RES#、D/C#、WR#、RD#、D0~D7;
- 2. Pins connected to external Power supply: VDD, VCC



■ RELIABILITY TESTS

Item		Condition	Criterion	
High Temperature Storage (HTS)		80±2°C, 200 hours	 After testing, the function test is ok. After testing, no addition to the defect. 	
High Temperature Operating (HTO)		70±2°C, 96 hours	3. After testing, the change of luminance should be within +/- 50% of initial value.	
Low Temperature Storage (LTS)		-30±2°C, 200 hours	4. After testing, the change for the mono and area color must be within (+/-0.02, +/-	
Low Temperature Operating (LTO)		-20±2°€, 96 hours	0.02) and for the full color it must be within (+/-0.04, +/-0.04) of initial value based on	
High Temperature / High Humidity Storage (HTHHS)		50±3°C, 90%±3%RH, 120 hours	1931 CIE coordinates. 5. After testing, the change of total current consumption should be	
Thermal Shock (Non-operation) (TS)		-20±2°C ~ 25°C ~ 70±2°C (30min) (5min) (30min) 10cycles	within +/- 50% of initial value.	
Vibration (Packing)	10~55~10Hz,amplitu de 1.5mm, 1 hour for each direction x, y, z	1. One box for each test.		
Drop (Packing)	Height: 1 m, each time for 6 sides, 3 edges, 1 angle	2. No addition to the cosmetic and the electrical defects.		
ESD (finished product housing)	±4kV (R: 330Ω C: 150pF , 10times, air discharge)	 After testing, cosmetic and electrical defects should not happen. In case of malfunction or defect caused by ESD damage, it would be judged as a good part if it would be recovered to normal state after resetting. 		

Note: 1) For each reliability test, the sample quantity is 3, and only for one test item.

- 2) The HTHHS test is requested the Pure Water(Resistance>10M Ω).
- 3) The test should be done after 2 hours of recovery time in normal environment.



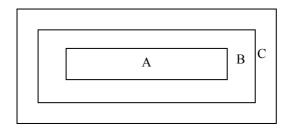
■OUTGOING QUALITY CONTROL SPECIFICATION

♦Standard

According to GB/T2828.1-2003/ISO 2859-1: 1999 and ANSI/ASQC Z1.4-1993, General Inspection Level II.

◆Definition

- 1 Major defect: The defect that greatly affect the usability of product.
- 2 Minor defect: The other defects, such as cosmetic defects, etc.
- 3 Definition of inspection zone:



Zone A: Active Area

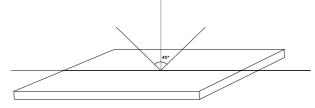
Zone B: Viewing Area except Zone A

Zone C: Outside Viewing Area

Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble of quality and assembly to customer's product.

◆Inspection Methods

1 The general inspection: under 20W x 2 or 40W fluorescent light, about 30cm viewing distance, within 45° viewing angle, under 25±5°C.



2 The luminance and color coordinate inspection: By PR705 or BM-7 or the equal equipments, in the dark room, under 25 ± 5 °C.

♦Inspection Criteria

1 Major defect: AOL= 0.65

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Item	Criterion			
F D	1. No display or abnormal display is not accepted			
Function Defect	2. Open or short is not accepted.			
	3. Power consumption exceeding the spec is not accepted.			
Outline Dimension	Outline dimension exceeding the spec is not accepted.			
Glass Crack Glass crack tends to enlarge is not accepted.				

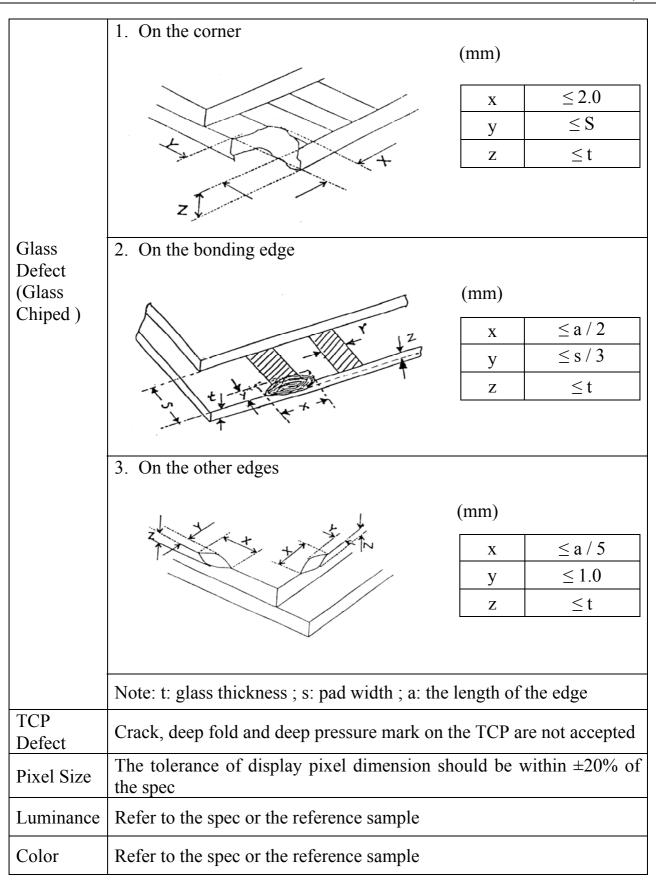
2 Minor Defect : AQL= 1.5



TRULY®信利 TRULY SEMICONDUCTORS LTD.

Item	Criterion					
Spot Defect (dimming and lighting spot)	Size (mm)		Accepted Qty			
	, ,		Area A + Area B	Area C		
		Φ≤0.10	Ignored			
	Y	$0.10 < \Phi \le 0.15$	3	Ignored		
		0.15<Φ≦0.20	1			
		0.20<⊕	0			
	Note: $\Phi = (x + y) / 2$					
Line Defect (dimming and lighting	L (Length): mm	W (Width): mm	Area A + Area B	Area C		
	/	$W \leq 0.03$	Ignored	•		
	L≦3.0	$0.03 < W \le 0.05$	2			
	L≦2.0	$0.05 < W \le 0.08$	1	Ignored		
line)	/	0.08 <w< td=""><td>As spot defect</td><td></td></w<>	As spot defect			
Remarks: The total of spot defect and line defect shall not exceed 4 pcs.						
Polarizer	Polarizer Stain which can be wiped off lightly with a soft cloth or similar					
Stain	cleaning is accepted, otherwise, according to the Spot Defect and the Line Defect.					
	1. If scratch can be seen during operation, according to the criterions					
	of the Spot Defect and the Line Defect.					
	2. If scratch can be seen only under non-operation or some special					
Polarizer Scratch	angle, the criterion is as below:					
	L (Length): mm	$W ext{ (Width) : mm}$	Area A + Area B	Area C		
	/ 50 / 1 / 100	$W \leq 0.03$	Ignore			
	5.0 <l≦10.0< td=""><td>$0.03 < W \le 0.05$</td><td>2</td><td rowspan="2">Ignore</td></l≦10.0<>	$0.03 < W \le 0.05$	2	Ignore		
	L≦5.0	$0.05 < W \le 0.08$	1			
	/	0.08 < W	0			
Polarizer Air Bubble	Size		Area A + Area B	Area C		
		Φ≦0.20	Ignored			
		$0.20 < \Phi \leq 0.50$	2	Ignored		
		$0.50 < \Phi \le 0.80$	1			
		0.80<Ф	0			





Jul.26, 2008

■ CAUTIONS IN USING OLED MODULE

◆Precautions For Handling OLED Module:

- 1. OLED module consists of glass and polarizer. Pay attention to the following items when handling:
 - i. Avoid drop from high, avoid excessive impact and pressure.
 - ii. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead.
 - iii. If the surface becomes dirty, breathe on the surface and gently wipe it off with a soft dry cloth. If it is terrible dirty, moisten the soft cloth with Isopropyl alcohol or Ethyl alcohol. Other solvents may damage the polarizer. Especially water, Ketone and Aromatic solvents.
 - iv. Wipe off saliva or water drops immediately, contact the polarizer with water over a long period of time may cause deformation.
 - v. Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peeling-off may occur with high temperature and high humidity.
 - vi. Condensation on the surface and the terminals due to cold or anything will damage, stain or dirty the polarizer, so make it clean as the way of iii.
- 2. Do not attempt to disassemble or process the OLED Module.
- 3. Make sure the TCP or the FPC of the Module is free of twisting, warping and distortion, do not pull or bend them forcefully, especially the soldering pins. On the other side, the SLIT part of the TCP is made to bend in the necessary case.
- 4. When assembling the module into other equipment, give the glass enough space to avoid excessive pressure on the glass, especially the glass cover which is much more fragile.
- 5. Be sure to keep the air pressure under 120 kPa, otherwise the glass cover is to be cracked.
- 6. Be careful to prevent damage by static electricity:
 - i. Be sure to ground the body when handling the OLED Modules.
 - ii. All machines and tools required for assembling, such as soldering irons, must be properly grounded.
 - iii. Do not assemble and do no other work under dry conditions to reduce the amount of static electricity generated. A relative humidity of 50%-60% is recommended.
 - iv. Peel off the protective film slowly to avoid the amount of static electricity generated.
 - v. Avoid to touch the circuit, the soldering pins and the IC on the Module by the body.
 - vi. Be sure to use anti-static package.
- 7. Contamination on terminals can cause an electrochemical reaction and corrade the terminal circuit, so make it clean anytime.
- 8. All terminals should be open, do not attach any conductor or semiconductor on the terminals.
- 9. When the logic circuit power is off, do not apply the input signals.
- 10. Power on sequence: $V_{DD} \rightarrow V_{CC}$, and power off sequence: $V_{CC} \rightarrow V_{DD}$.
- 11. Be sure to keep temperature, humidity and voltage within the ranges of the spec, otherwise shorten Module's life time, even make it damaged.
- 12. Be sure to drive the OLED Module following the Specification and datasheet of IC controller, otherwise something wrong may be seen.

Rev: 0.0 Jul.26, 2008

13. When displaying images, keep them rolling, and avoid one fixed image displaying more than 30 seconds, otherwise the residue image is to be seen. This is the speciality of OLED.

◆Precautions For Soldering OLED Module:

- 1. Soldering temperature : $260^{\circ}\text{C} \pm 10^{\circ}\text{C}$.
- 2. Soldering time: 3-4 sec.
- 3. Repeating time: no more than 3 times.
- 4. If soldering flux is used, be sure to remove any remaining flux after finishing soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended to protect the surface with a cover during soldering to prevent any damage due to flux spatters.

♦ Precautions For Storing OLED Module:

- 1. Be sure to store the OLED Module in the vacuum bag with dessicant.
- 2. If the Module can not be used up in 1 month after the bag being opened, make sure to seal the Module in the vacuum bag with dessicant again.
- 3. Store the Module in a dark place, do not expose to sunlight or fluorescent light.
- 4. The polarizer surface should not touch any other objects. It is recommended to store the Module in the shipping container.
- 5. It is recommended to keep the temperature between 0°C and 30°C, the relative humidity not over 60%.

♦ Limited Warranty

Unless relevant quality agreements signed with customer and law enforcement, for a period of 12 months from date of production, all products (except automotive products) TRULY will replace or repair any of its OLED modules which are found to be functional defect when inspected in accordance with TRULY OLED acceptance standards (copies available upon request). Cosmetic/visual defects must be returned to TRULY within 90 days of shipment. Confirmation of such date should be based on freight documents. The warranty liability of TRULY is limited to repair and/or replacement on the terms above. TRULY will not be responsible for any subsequent or consequential events.

♦ Return OLED Module Under Warranty:

- 1. No warranty in the case that the precautions are disregarded.
- 2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects.

♦PRIOR CONSULT MATTER

- 1. ①For TRULY standard products ,we keep the right to change material ,process ... for improving the product property without any notice on our customer.
 - ②For OEM products ,if any change needed which may affect the product property , we will consult with our customer in advance.
- 2. If you have special requirement about reliability condition, please let us know before you start the test on our samples.