Small PKG Half Bridge Driver

■ GENERAL DESCRIPTION

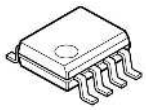
The NJW4801 is a general purpose, half bridge power driver capable of supplying ±450mA current.

The internal gate driver drives high-side/low-side power MOSFET, therefore, it has fast switching.

Additionally, it has protection features such as over current protection and thermal shutdown. And in the case of failure, it can output a fault flag.

It is suitable for power switching applications of DSP/micro controller.

■ PACKAGE OUTLINE



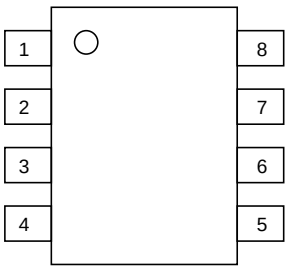
NJW4801R

■ FEATURES

- Output Switch Current ±450mA
- Operating Voltage 8.0V to 35V
- High-side and Low-side SW is available independently-function
- Up to 700kHz Switching Frequency
- Thermal Shut Down
- Over Current Protection
- Under Voltage Lockout
- Fault Indicator Output
- Stand-by Current I_{QSTBY} =3μA (typ.)
- Package Outline MSOP8 (VSP8)*

* MEET JEDEC MO-187-DA

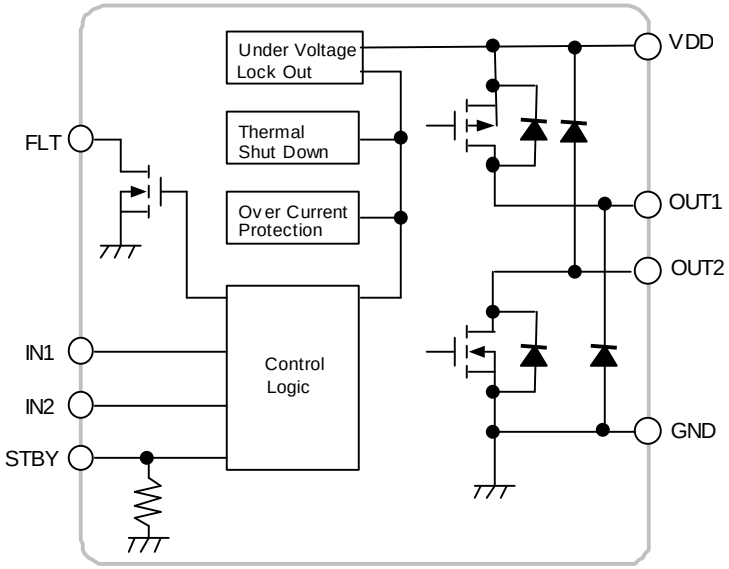
■ PIN CONFIGURATION



1. STBY
2. IN1
3. IN2
4. FLT
5. GND
6. OUT2
7. OUT1
8. VDD

NJW4801R

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
Supply Voltage	V^+	40	V	VDD-GND Pin
Input Voltage	V_{STBY}	–0.3 to 6	V	STBY-GND Pin
Input Voltage	V_{IN1} V_{IN2}	–0.3 to 6	V	IN1/2-GND Pin
FLT pin Voltage	V_{FLT}	–0.3 to 6	V	FLT-GND Pin
Power Dissipation	P_D	595 (*1) 805 (*2)	mW	–
Operating Junction Temperature	Tj	–40 to +150	°C	–
Operating Temperature Range	T_{opr}	–40 to +85	°C	–
Storage Temperature Range	T_{stg}	–50 to +150	°C	–

(*1): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

(*2): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers),
internal Cu area: 74.2×74.2mm

■ RECOMMENDED OPERATING CONDITIONS (Ta=25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARKS
Operating Voltage	V_{opr}	8	–	35	V	VDD-GND Pin
Output Switch Current	I_{OM}	0	–	450	mA	OUT-GND Pin
Input Voltage	V_{STBY}	0	–	5.5	V	STBY-GND Pin
Input Voltage	V_{IN1}, V_{IN2}	0	–	5.5	V	IN1/2-GND Pin
FLT pin Voltage	V_{FLT}	0	–	5.5	V	FLT-GND Pin

■ THERMAL CHARACTERISTICS (Ta=25°C)

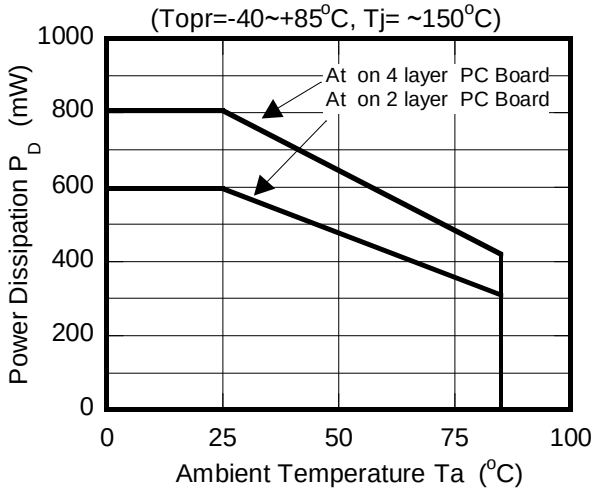
PARAMETER	SYMBOL	THERMAL RESISTANCE	UNIT
Thermal Resistance between Tj and Ta	θja	210 (*1) 155 (*2)	°C/W
Thermal Resistance between Tj and T_{C1}	ψjt	33 (*1) 25 (*2)	°C/W

(*1): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

(*2): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers),
internal Cu area: 74.2×74.2mm

Power Dissipation vs. Ambient Temperature

(Topr=-40~+85°C, Tj= ~150°C)



■ ELECTRICAL CHARACTERISTICS (Unless other noted, V^+=12V, V_{STBY}=0V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
General Characteristics						
Quiescent Current 1 (Operating)	I_{Q1}	V_{IN1}=V_{IN2}=0V	–	1	1.4	mA
Quiescent Current 2 (Switching)	I_{Q2}	V_{IN1}=V_{IN2}=0 to 3V, f_{PWM1}=f_{PWM2}=700kHz, 50% Duty Cycle	–	3	4	mA
Quiescent Current 3 (Standby)	I_{QOFF}	V_{STBY}=5V, V_{IN1}=V_{IN2}=0V	–	2.9	4	μA
Output Block						
High-side SW ON Resistance (OUT1)	R_{DSH}	$I_{OSOURCE}$=450mA	–	0.65	1	Ω
Low-side SW ON Resistance (OUT2)	R_{DSL}	I_{OSINK}=450mA	–	0.65	1	Ω
Over Current Limit	I_{LIMIT}	High-side and Low-side	600	1200	1800	mA
Turn-on Time	tr	V_{IN1}=V_{IN2}=0 to 3V, OUT1-OUT2 pin is short	–	5	–	ns
Turn-off Time	tf	V_{IN1}=V_{IN2}=0 to 3V, OUT1-OUT2 pin is short	–	5	–	ns
Dead Time	Dt	V_{IN1}=V_{IN2}=0 to 3V, OUT1-OUT2 pin is short	–	50	–	ns
Output Rise Propagation Delay Time	t_{d_ON}	V_{IN1}=V_{IN2}=0 to 3V, OUT1-OUT2 pin is short	–	100	–	ns
Output Fall Propagation Delay Time	t_{d_OFF}	V_{IN1}=V_{IN2}=0 to 3V, OUT1-OUT2 pin is short	–	100	–	ns
OUT1–VDD pin voltage Difference	V_{PDOV}	I_{ORH}=450mA	–	0.87	1.22	V
GND–OUT2 pin Voltage Difference	V_{PDGO}	I_{ORL}=450mA	–	0.82	1.15	V
OUT2–VDD pin Voltage Difference	V_{RDOV}	I_{ORH}=450mA	–	0.96	1.25	V
OUT1–GND pin Volatge Difference	V_{RDGO}	I_{ORL}=450mA	–	1.13	1.46	V
OUT1 Pin Leak Current	I_{OLEAK1}	V^+=35V, V_{IN1}=0V, V_{OUT1}=0V	–	–	1	μA
OUT2 Pin Leak Current	I_{OLEAK2}	V^+=35V,V_{IN2}=3V,V_{OUT2}=35V	–	–	1	μA
Input Circuit Block						
STBY pin High Voltage (Standby Mode)	V_{IHSTBY}		2.4	–	5.5	V
STBY pin Low Voltage(Operating Mode)	V_{ILSTBY}		0	–	0.4	V
STBY Pin Sink Current	I_{ISTBY}	V_{STBY}=1V	1	2	4	μA
IN1/IN2 Pin High Voltage	V_{IHIN1}, V_{IHIN2}		2.4	–	5.5	V
IN1/IN2 Pin Low Voltage	V_{ILIN1}, V_{ILIN2}		0	–	0.9	V
IN1/IN2 Pin Sink Current	I_{IIN1}, I_{IIN2}	V_{IN1}, V_{IN2}=5.5V	–	–	1	μA
Under Voltage Lockout (UVLO) Block						
UVLO Release Voltage	V_{UVLO2}		6.4	7.1	7.8	V
UVLO Operation Voltage	V_{UVLO1}		6	6.7	7.4	V
UVLO Hysteresis Voltage	ΔV_{UVLO}	V_{UVLO2}-V_{UVLO1}	–	0.4	–	V
FLT Function (FLT pin)						
Low Level Output Voltage	V_{LFLT}	I_{FLT}=500μA	–	0.25	0.5	V
OFF Leak Current	$I_{OLEAKFLT}$	V_{FLT}=5.5V	–	–	1	μA

■ PIN OPERATION TABLE

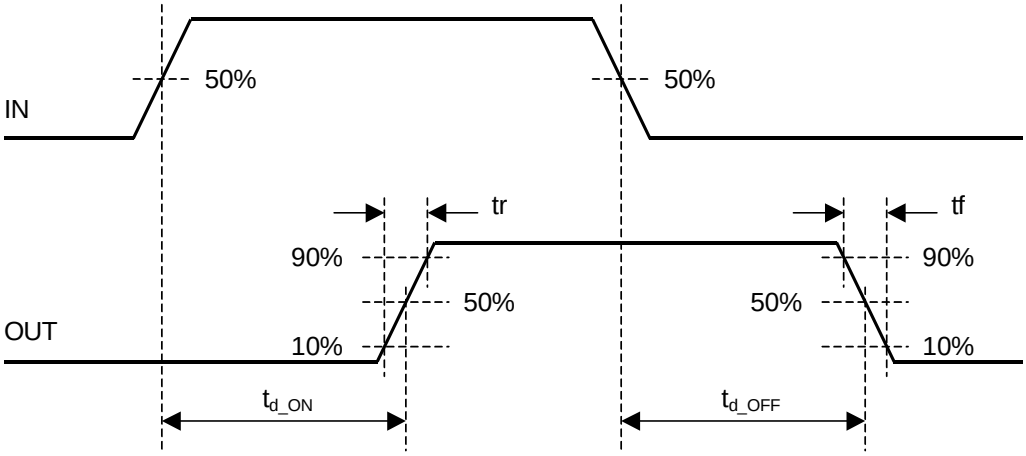
INPUT		OUTPUT	
IN1	IN2	High-side SW (OUT1)	Low-side SW (OUT2)
L	L	OFF	ON
L	H	OFF	OFF
H	L	ON	ON
H	H	ON	OFF

INPUT			OUTPUT			Mode
IN1, IN2	STBY	VDD	FLT	High-side SW (OUT1)	Low-side SW (OUT2)	
L or H	L	$V^+ \geq V_{RUVLO}$	ON	OFF or ON	OFF or ON	Active
L or H	H	–	OFF	OFF	OFF	Stand-by
L or H	L	$V^+ < V_{DUVLO}$	OFF	OFF	OFF	UVLO

INPUT		OUTPUT			Mode
Tj	I_{OUT}	FLT	High-side SW (OUT1)	Low-side SW (OUT2)	
Tj >150°C	–	OFF	OFF	OFF	TSD
–	$I_{OUT} \geq I_{LIMIT}$	OFF	OFF	OFF	OCP

■ TIMING CHART

Fig1. Turn-on/Turn-off Time, Output Rise/Fall Propagation Delay Time



■ TEST CIRCUIT

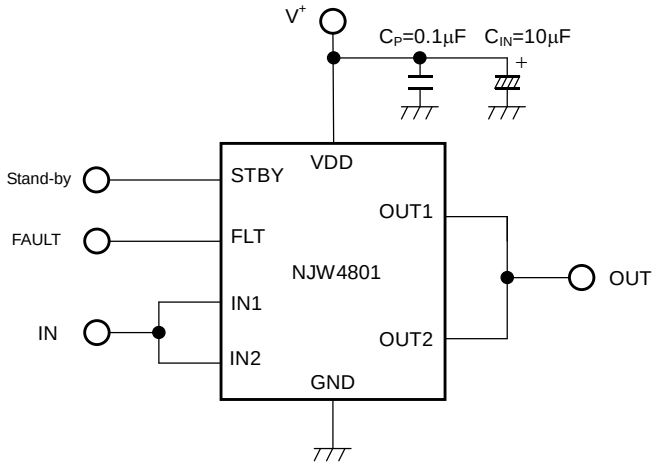
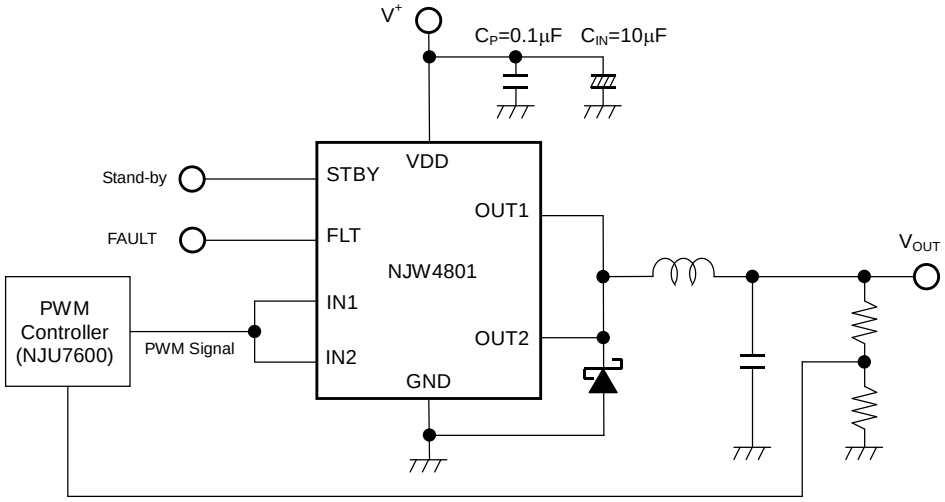
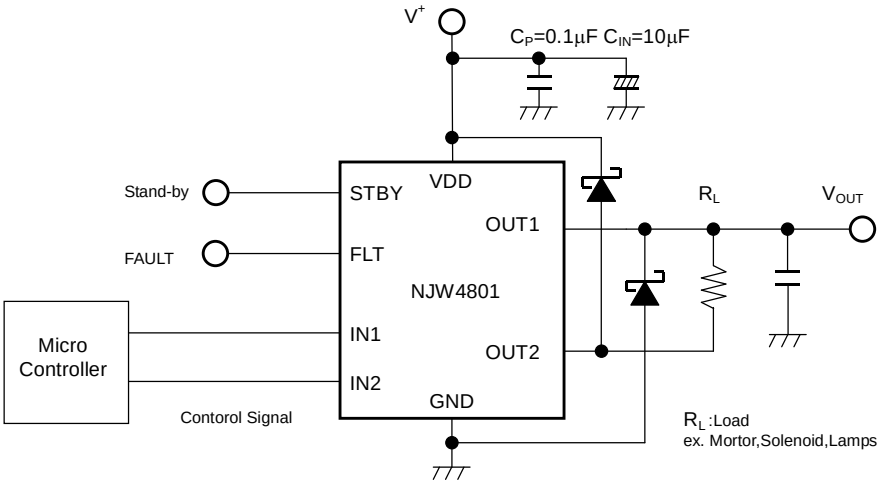


Fig2. Switching time Measurement Circuit

■ TYPICAL APPLICATIONS

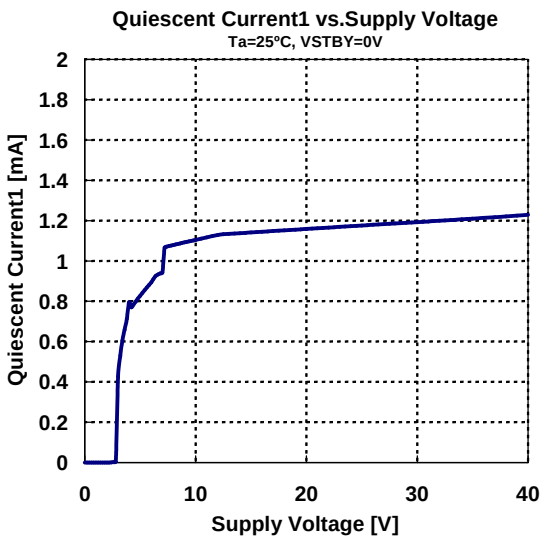


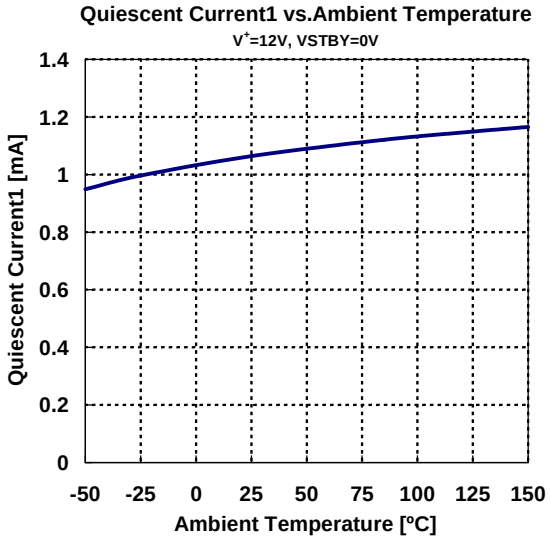
Synchronous PWM step down switching regulator

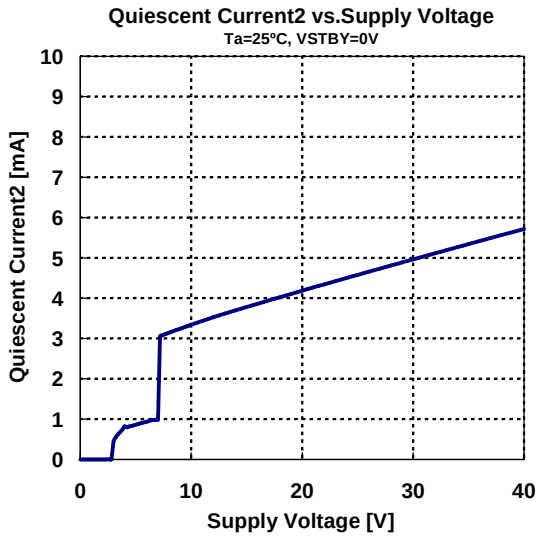


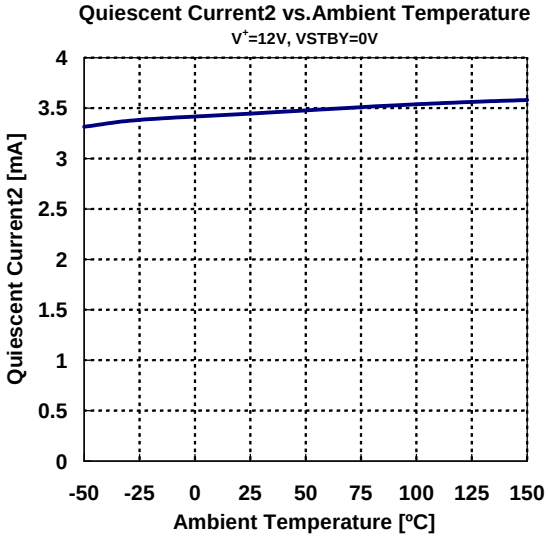
High Side SW and Low Side SW application

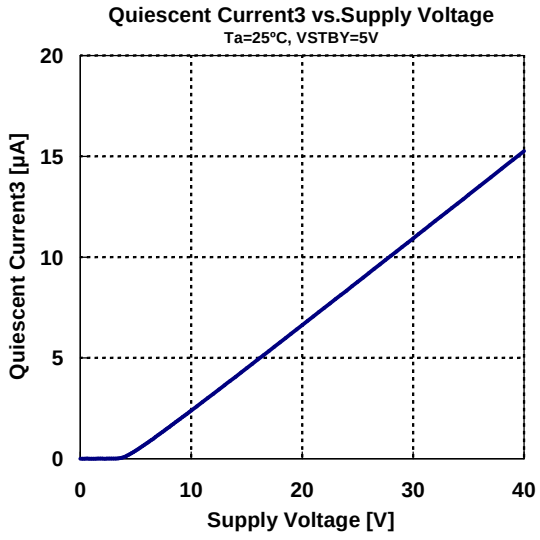
■ CHARACTERISTICS

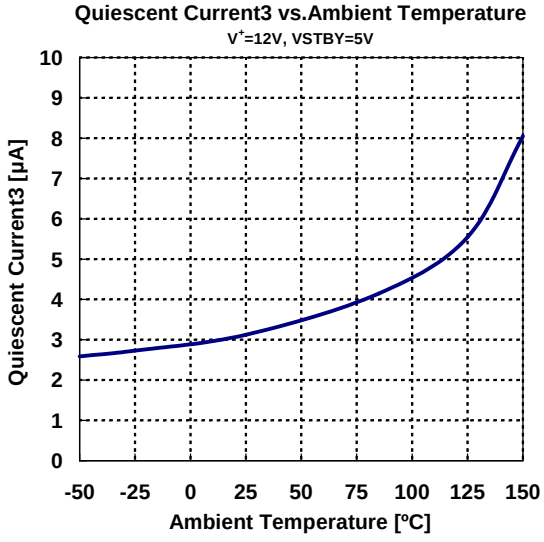






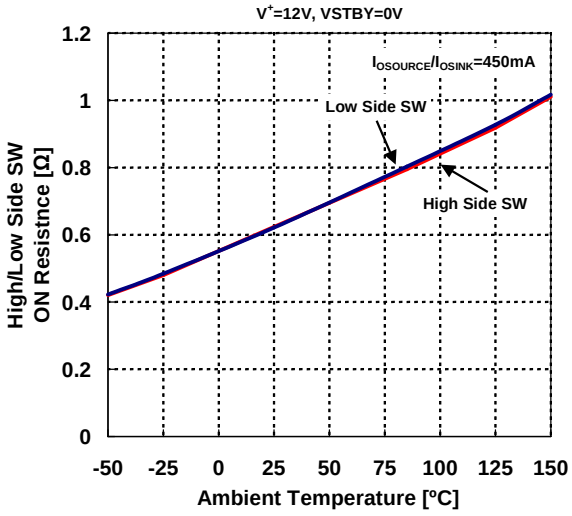




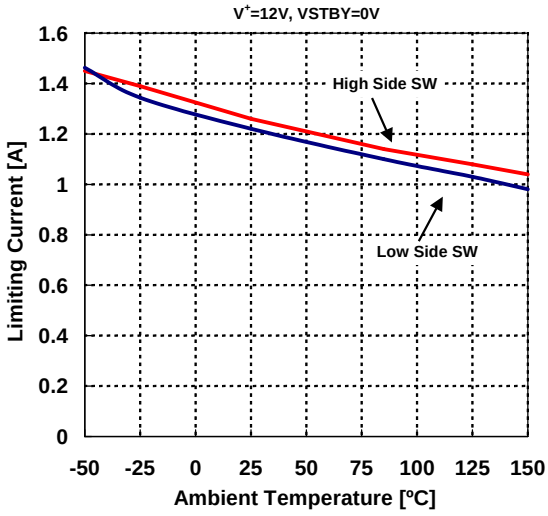


■ CHARACTERISTICS

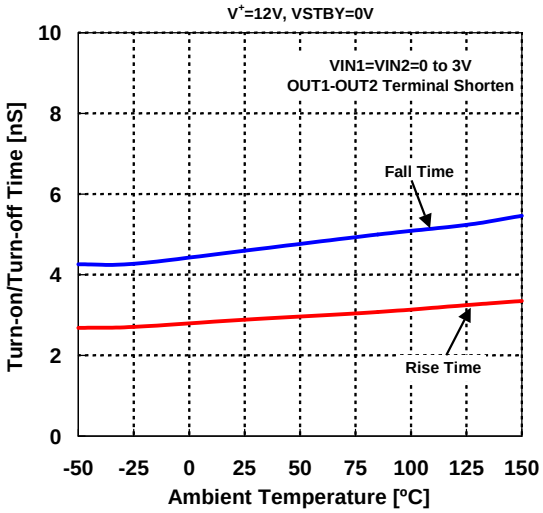
High/Low Side SW ON Resistnce
vs. Ambient Temperature
V+=12V, VSTBY=0V



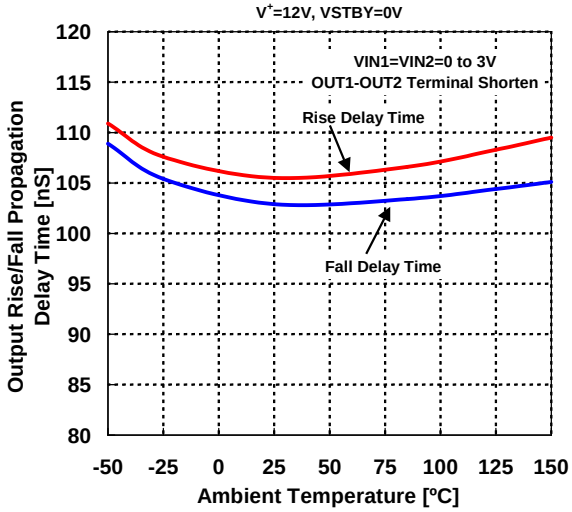
Over Current Limit
vs. Ambient Temperature
V+=12V, VSTBY=0V



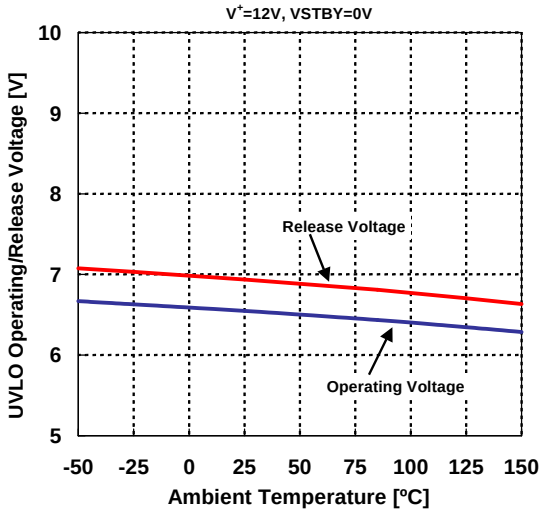
Turn-on/Turn-off Time
vs. Ambient Temperature
V+=12V, VSTBY=0V



Output Rise/Fall Propagation Delay Time
vs. Ambient Temperature
V+=12V, VSTBY=0V



UVLO Operating/Release Voltage
vs. Ambient Temperature
V+=12V, VSTBY=0V



■ PIN DESCRIPTION

PIN NUMBER	PIN NAME	FUNCTION
1	STBY	Standby Pin NJW4801 becomes standby status by High Level NJW4801 operates by Low Level
2	IN1	Signal Input Pin for High-side SW High-side SW turns on at High level and High-side SW turns off at Low level. IN1 and IN2 operate with inverse logic.
3	IN2	Signal Input Pin for Low-side SW Low-side SW turns off at High level and Low-side SW turns on at Low level. IN1 and IN2 operate with inverse logic.
4	FLT	Fault Signal Output Pin. It is Open Drain Output Type. You should connect through Pull-up Resister to External Power Supply. It outputs Low Level under normal operating condition and outputs High Level under Abnormal Conditions.
5	GND	Ground Pin
6	OUT2	Output Pin The Low-side Switch are Limited to 1.2A (typ.) by Over Current Protection Circuit.
7	OUT1	Output Pin The High-side Switch are Limited to 1.2A (typ.) by Over Current Protection Circuit.
8	VDD	Power Supply Pin You should connect capacitor (AL and MLCC) for reducing Input Impedance.

■ FUNCTIONAL EXPLANATION

● High-side, Low-side Switch

The OUT1 pin is High-side SW output. The OUT2 pin is Low-side SW output. These SW are controlled by IN1 and IN2, so it can be operated independently.

The High-side SW turns on when IN1 pin voltage is more than 2.4V and turns off when IN1 pin voltage is less than 0.9V. The Low-side SW turns off when IN2 pin voltage is more than 2.4V and turns on when IN2 pin voltage is less than 0.9V.

Because IN1 and IN2 are inverse logic input, the half bridge application with one input signal can be easily composed.

In this case, OUT1 and OUT2 pin can be used as short-circuit.

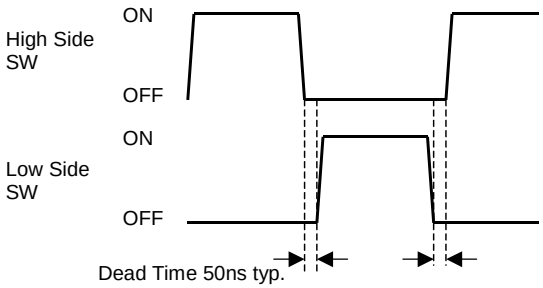


Fig3. Relation of SW Function and Dead Time

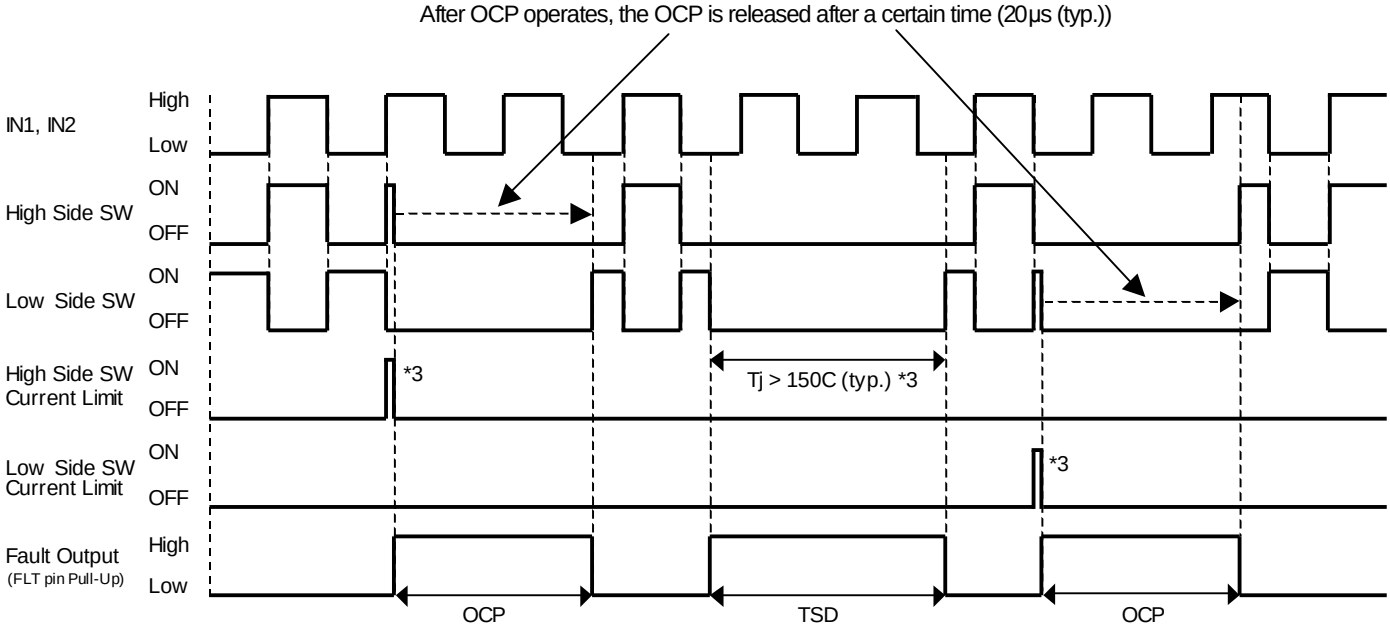
NJW4801 has dead time to prevent the short circuit at the time of operation change of the high side and the low side SW. (ex. Fig3) The dead time typical value is 50ns. This can be used for the application of the switching regulator that needs the high frequency. As for input frequency, you should make less than 700kHz.

● Over Current Protection Function

The internal over-current protection circuit monitors the flow currents of both the high-side and low-side switches. The over-current protection circuit operates at 1.2A (typ.) and stops the both SW operation. The FLT detection signal is output from FLT pin at the same time. The overcurrent protection operation is released after certain time (20μs (typ)), after overcurrent protection operates. (Ex. Fig4)

If OUT pin is shorted directly to GND, a large surge current is flowing for fast current change and may exceed current limit. Because that time big electric power consumption occurs instantaneously in NJW4801, you should design sufficient heat dissipation.

When a load condition is inductive property, a reverse direction current flows to the high-side and low-side SW body diode by inductive kickback. The built-in over-current protection circuit has not aimed at protection against the inductive kickback. Therefore, an external diode should be considered usage against reverse-current regeneration according to the kind of the application.



*3: When the thermal shutdown protection or the over current protection operates, both High-side and Low-side SW are turned off.

Fig4. Timing Chart of High-side/Low-side Switch at Over Current Protection Operating

(In case of IN1 and IN2 signal are same)

● Thermal Shut Down Function

When NJW4801 chip temperature exceeds the 170°C (*4), internal thermal shutdown circuit operates and SW function is stopped. The Fault signal is output simultaneously from the FLT pin. In order to return switching operation, you should need to junction temperature: Tj below the 150°C (*4).
This function is a circuit to prevent IC at the high temperature from malfunctioning and is not something that urges positive use. You should make sure to operate inside the junction temperature range rated. (*4 Design value)

● Under Voltage Lockout(UVLO)

The UVLO circuit operating is released above V^+=7.1V (typ.) and IC operation starts. When power supply voltage is low, because the UVLO circuit operates, IC does not operate. There is 0.4V (typ.) width hysteresis voltage at rise and decay of power supply voltage. Hysteresis prevents the malfunction at the time of UVLO operating and releasing.

● FAULT Signal Output

When NJW4801 function is abnormal, an error signal is output from FLT Pin. This Pin is Open Drain Output Type. You should connect through Pull-up Resister to External Power Supply. It outputs Low Level under normal operating condition and outputs High Level under Abnormal Conditions.

The following information is output as FAULT signal.

- Stop Operation at Under Voltage Lockout (UVLO)
- Over Current Protection Function
- Thermal Shut Down

At the time of standby state, it outputs High Level.

● Standby Function

NJW4801 stops the operating and becomes standby status when 2.4V or more is supplied to STBY pin.
You should connect the pin with GND level to prevent the malfunction by a noise when you do not use this function.

■ APPLICATION TIPS

In the application that does a high-speed switching of NJW4801, because the current flow corresponds to the input frequency, the substrate (PCB) layout becomes an important.

NJW4801 is driving the High-side/Low-side SW gate with high speed to reduce switching losses. The transient voltage is generated by parasitic inductance and a high-speed current change of high side and low side SW.

You should attempt the transition voltage decrease by making a current loop area minimize as much as possible. Therefore, you should make a current flowing line thick and short as much as possible.

Moreover, you should insert a bypass capacitor between VDD pin and GND pin to prevent malfunction by generating over voltage and/or exceed maximum input voltage rating. The recommended bypass capacitor is 0.1μF or more high frequency capacitor.

A 10μF aluminum electrolysis capacitor is recommended for smoothing condenser. However, you should use larger capacitor by sufficient evaluation (assessment) due to load condition and/or application use environment. (There is a possibility that the supply voltage rises by inductive kickback when the supply current of the inductive load is large.)
The bypass capacitors should be connected as much as possible near VDD pin.

MEMO

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