HIGH POWER DPDT SWITCH GaAs MMIC

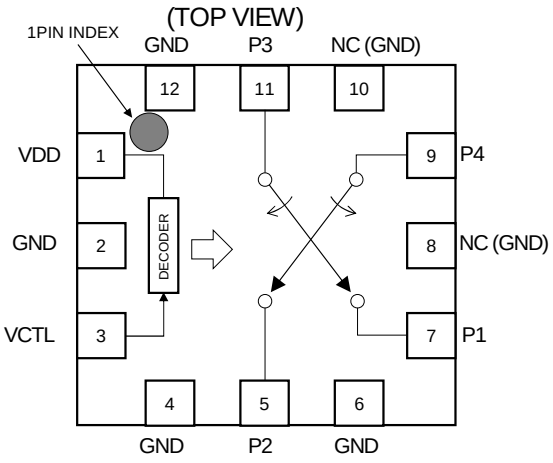
■ FEATURES

- AEC-Q100 grade 2 qualified
- Low voltage operation V_{DD} = 2.7 V typ.
- Logic control voltage V_{CTL}(H) = 1.35 to 5.0 V
- Low insertion loss
  0.25 dB typ. @ f = 900 MHz, P_{IN} = +35 dBm
  0.35 dB typ. @ f = 1900 MHz, P_{IN} = +33 dBm
  0.45 dB typ. @ f = 2700 MHz, P_{IN} = +27 dBm
- Low harmonics
  2fo = -89 dBm typ. @ f = 786.5 MHz, P_{IN} = +23 dBm
  3fo = -89 dBm typ. @ f = 710 MHz, P_{IN} = +23 dBm
- High power handling
  $P_{-0.1dB}$ = +36 dBm min.
- Package with wettable flank EQFN12-ET
  (2.0 x 2.0 x 0.78 mm typ., pin pitch 0.5 mm)
- RoHS compliant and Halogen Free, MSL1

■ APPLICATION

- eCall
- Telematics
- Antenna swapping, general purpose switching applications
- LTE, UMTS, CDMA, GSM systems

■ BLOCK DIAGRAM (EQFN12-ET)



■ GENERAL DESCRIPTION

The NJG1812AMET-A is a GaAs DPDT switch MMIC suitable for antenna swapping of LTE/UMTS/CDMA/GSM applications.

This switch features very low insertion loss, low distortion and excellent linearity performance with 1.8 V 1bit control voltage at high frequency up to 3 GHz.

Integrated ESD protection device on each port achieves excellent ESD robustness. No DC blocking capacitors are required for all RF ports unless DC is biased externally.

EQFN12-ET package with wettable flank structure corresponds to Automated Optical Inspection (AOI).

■ TRUTH TABLE

"H" = V_{CTL}(H), "L" = V_{CTL}(L)

V_{CTL}	Path
L	P1-P4 P2-P3
H	P1-P3 P2-P4

■ PIN CONFIGURATION

PIN NO.	SYMBOL	DESCRIPTION
1	VDD	Voltage supply terminal
2	GND	Ground terminal
3	VCTL	Control signal input terminal.
4	GND	Ground terminal
5	P2	RF input/output
6	GND	Ground terminal
7	P1	RF input/output
8	NC (GND)	No connected terminal (Connect to ground)
9	P4	RF input/output
10	NC (GND)	No connected terminal (Connect to ground)
11	P3	RF input/output
12	GND	Ground terminal
Exposed pad	GND	Ground terminal

■ PRODUCT NAME INFORMATION

NJG1812A MET -A (TE1)

Part number	Package	Automotive	Taping form

■ ORDERING INFORMATION

PART NUMBER	PACKAGE OUTLINE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs.)
NJG1812AMET-A	EQFN12-ET	Yes	Yes	SnBi	1812 A A	8.5	3,000

■ ABSOLUTE MAXIMUM RATINGS

(General conditions: T_a = 25°C, Z_s = Z_l = 50 Ω)

PARAMETER	SYMBOL	RATINGS	UNIT
RF Input Power	P_{IN}	+38(1)	dBm
Supply Voltage	V_{DD}	5.0	V
Control Voltage	V_{CTL}	5.0	V
Power Dissipation(2)	P_D	1400	mW
Operating Temperature	T_{opr}	-40 to +105	°C
Storage Temperature	T_{stg}	-55 to +150	°C

(1): V_{DD} = 2.7 V, ON port

(2): Four-layer FR4 PCB with through-hole (101.5 x 114.5 mm), Tj = 150°C

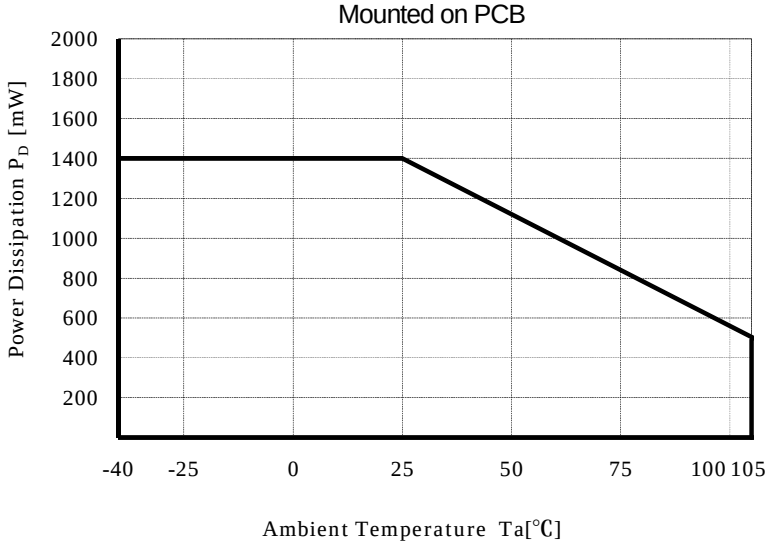
■ POWER DISSIPATION VS.AMBIENT TEMPERATURE

Please, refer to the following Power Dissipation and Ambient Temperature.

(Please note the surface mount package has a small maximum rating of Power Dissipation [P_D], a special attention should be paid in designing of thermal radiation.)

Power Dissipation－Ambient Temperature Characteristic

Mounted on PCB



■ ELECTRICAL CHARACTERISTICS 1 (DC CHARACTERISTICS)

(General conditions: T_a = 25°C, Z_s = Z_l = 50 Ω, with application circuit)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.4	2.7	5.0	V
Operating Current	I_{DD}	No RF input	-	90	180	μA
Control Voltage (LOW)	V_{CTL}(L)		0	-	0.45	V
Control Voltage (HIGH)	V_{CTL}(H)		1.35	1.8	5.0	V
Control Current	I_{CTL}	V_{CTL}(H) = 1.8V	-	4	10	μA

■ ELECTRICAL CHARACTERISTICS 2 (RF CHARACTERISTICS)

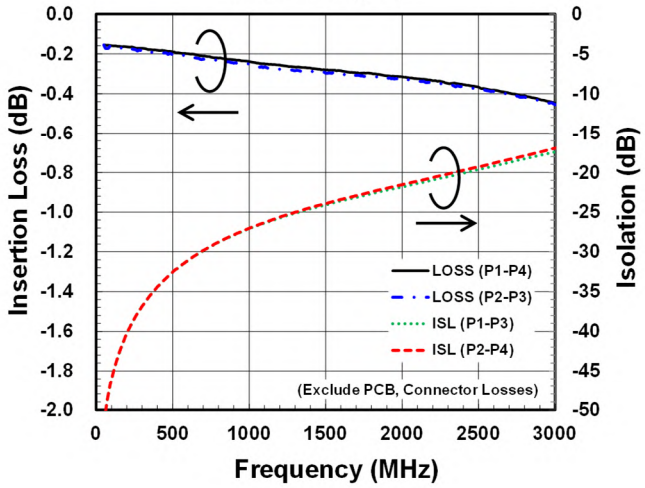
(General conditions: T_a = +25°C, Z_s = Z_l = 50 Ω, V_{DD} = 2.7 V, V_{CTL}(H) = 1.8V, V_{CTL}(L) = 0 V, with application circuit)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Insertion Loss	LOSS	f = 900 MHz, P_{IN} = +35 dBm	-	0.25	0.45	dB
		f = 1900 MHz, P_{IN} = +33 dBm	-	0.35	0.55	
		f = 2700 MHz, P_{IN} = +27 dBm	-	0.45	0.65	
Isolation	ISL	f = 900 MHz, P_{IN} = +35 dBm	23	25	-	dB
		f = 1900 MHz, P_{IN} = +33 dBm	18	20	-	
		f = 2700 MHz, P_{IN} = +27 dBm	15	17	-	
Input Power at 0.1dB Compression Point	$P_{-0.1dB}$	f = 2700 MHz	+36	-	-	dBm
2nd Harmonics	2fo	f = 900 MHz, P_{IN} = +33 dBm	-	-	-40	dBm
		f = 1900 MHz, P_{IN} = +30 dBm	-	-	-40	
		f = 2700 MHz, P_{IN} = +23 dBm	-	-	-60	
		f = 786.5 MHz, P_{IN} = +23 dBm	-	-89	-81	
3rd Harmonics	3fo	f = 900 MHz, P_{IN} = +33 dBm	-	-	-40	dBm
		f = 1900 MHz, P_{IN} = +30 dBm	-	-	-40	
		f = 2700 MHz, P_{IN} = +23 dBm	-	-	-60	
		f = 710 MHz, P_{IN} = +23 dBm	-	-89	-81	
		f = 786.5 MHz, P_{IN} = +23 dBm	-	-89	-81	
2nd order intermodulation	IMD2	f_{TX} = 835 MHz, P_{TX} = +20 dBm, f_{jam} = 1715 MHz,P_{jam} = -15 dBm, f_{meas} = 880 MHz	-	-110	-105	dBm
3rd order intermodulation	IMD3	f_{TX} = 835 MHz, P_{TX} = +20 dBm, f_{jam} = 790 MHz, P_{jam} = -15 dBm, f_{meas} = 880 MHz	-	-110	-105	dBm
Triple Beat Ratio	TBR	$f_{TX}1$ = 835.5 MHz, $P_{TX}1$ = +21.5 dBm, $f_{TX}2$ = 836.5 MHz, $P_{TX}2$ = +21.5 dBm, f_{jam} = 881.5 MHz, P_{jam} = -30 dBm, f_{meas} = 881.5±1 MHz	-	93	-	dBc
VSWR	VSWR	P1 to P4 Terminal, f = 2700 MHz	-	1.1	1.5	-
Switching time	T_{SW}	50% V_{CTL} to 10/90% RF	-	1	5	μs

■ **ELECTRICAL CHARACTERISTICS** (With application circuit, loss of external circuit are excluded.)

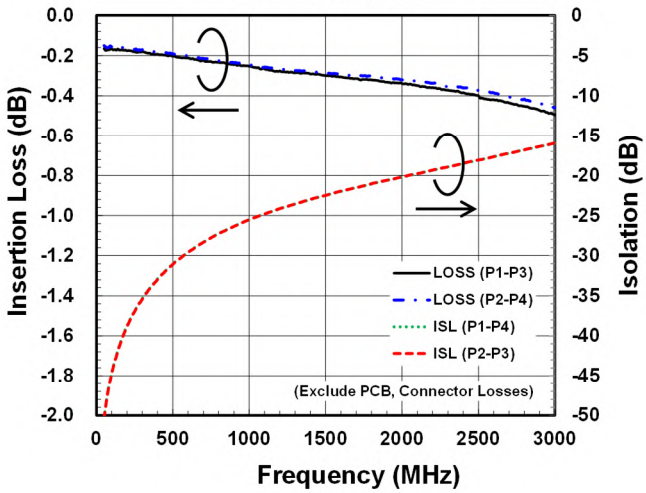
LOSS, ISL vs. Frequency

(V_{DD}=2.7V, $V_{CTL(L)}$=0V)



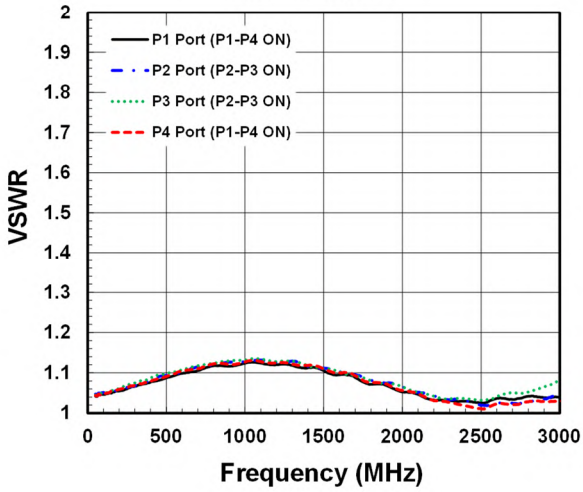
LOSS, ISL vs. Frequency

(V_{DD}=2.7V, $V_{CTL(H)}$=1.8V)



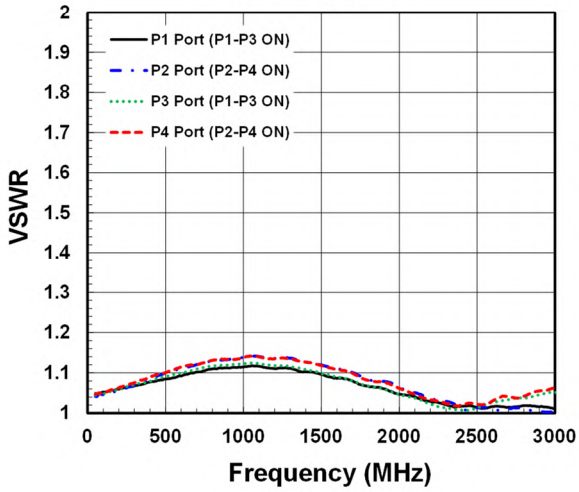
VSWR vs. Frequency

(V_{DD}=2.7V, $V_{CTL(L)}$=0V)



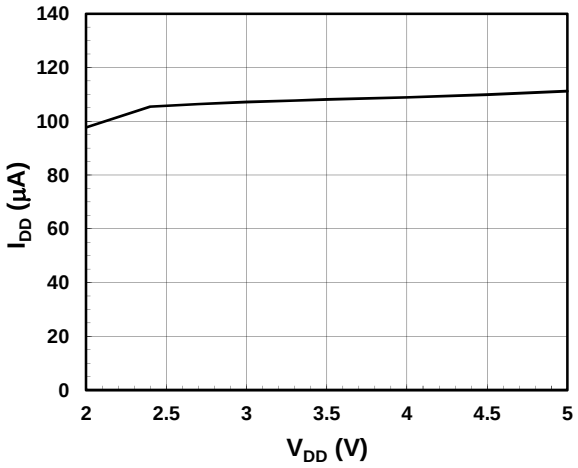
VSWR vs. Frequency

(V_{DD}=2.7V, $V_{CTL(H)}$=1.8V)



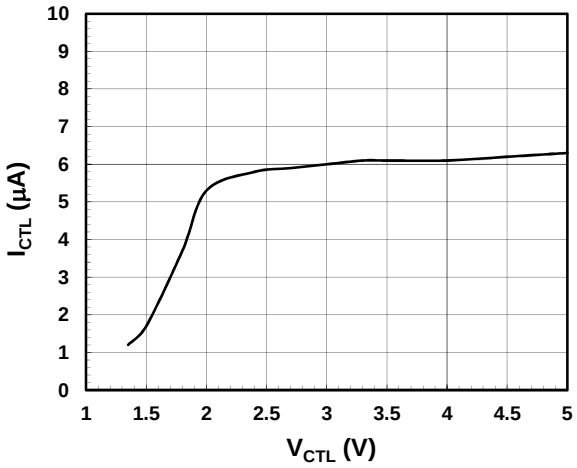
I_{DD} vs. V_{DD}

(No RF Input, $V_{CTL(L)}$=0V)

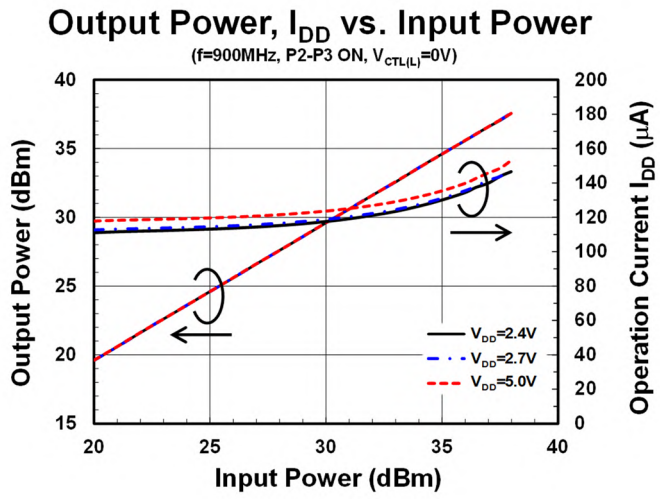


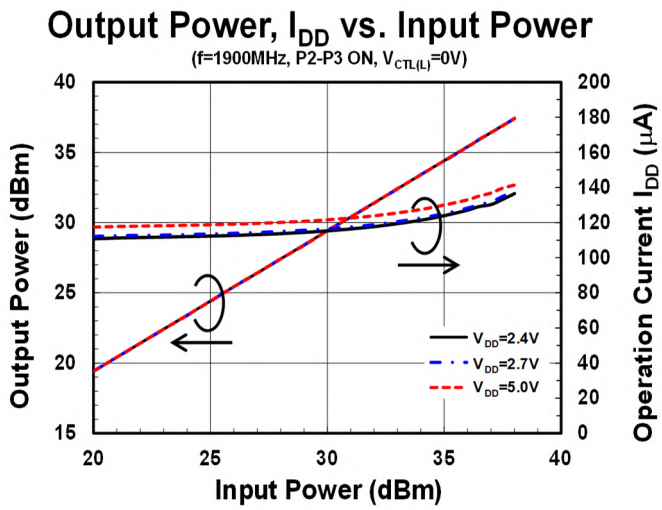
I_{CTL} vs. V_{CTL}

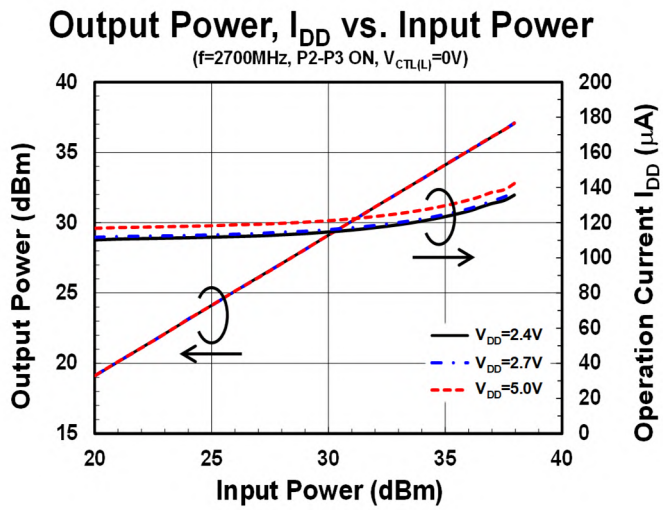
(No RF Input, V_{DD}=2.7V)

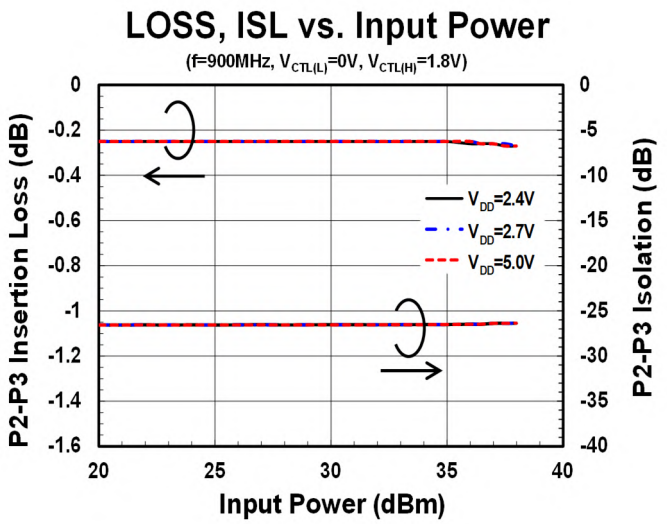


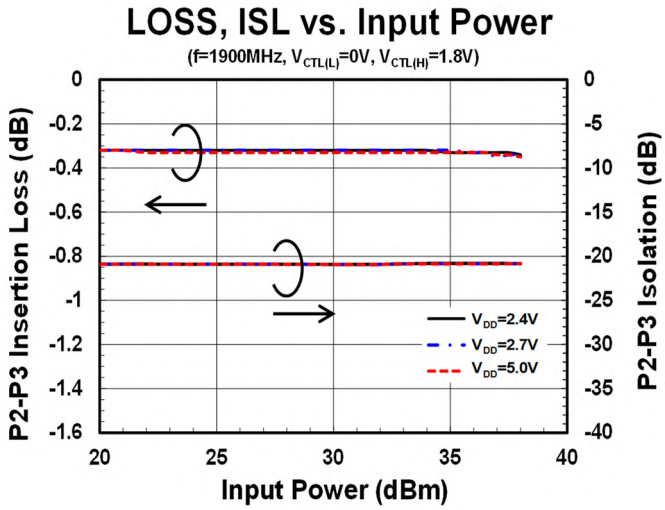
■ **ELECTRICAL CHARACTERISTICS** (With application circuit, loss of external circuit are excluded.)

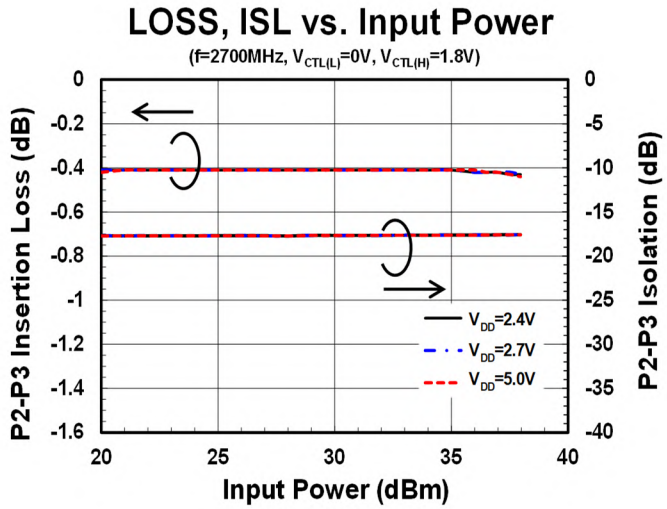








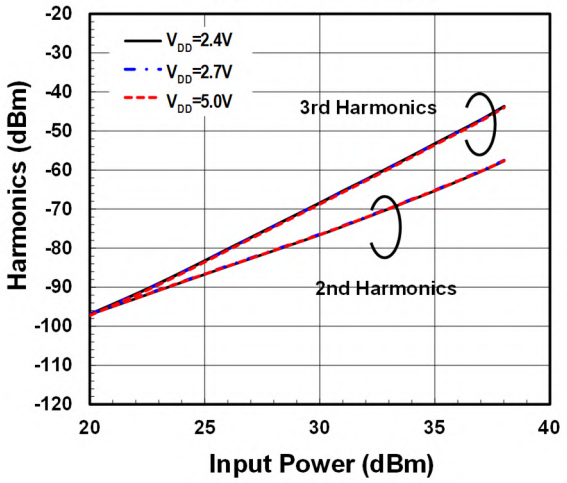




■ **ELECTRICAL CHARACTERISTICS** (With application circuit, loss of external circuit are excluded.)

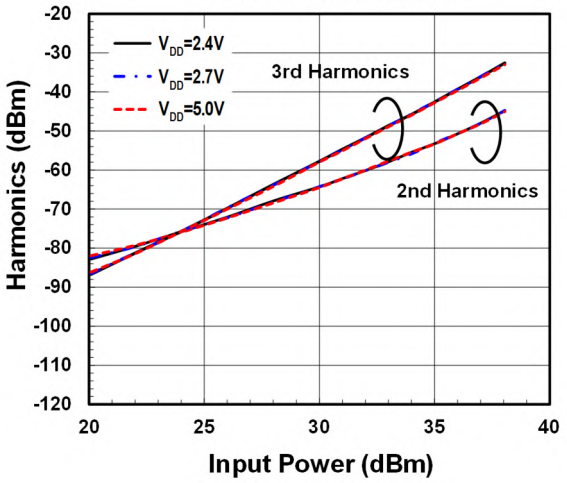
Harmonics vs. Input Power

(f=900MHz, P2-P3 ON, $V_{CTL(L)}$=0V)



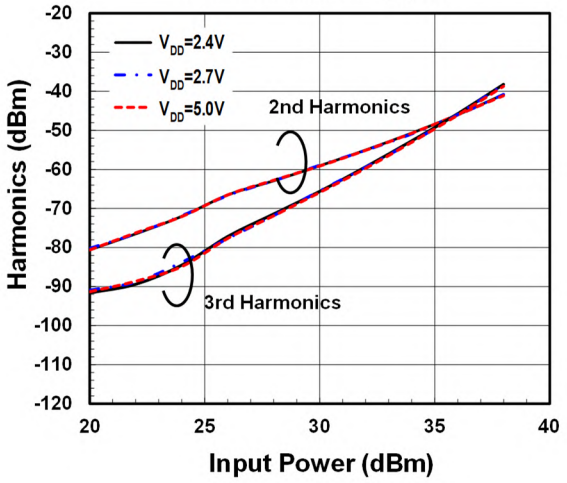
Harmonics vs. Input Power

(f=1900MHz, P2-P3 ON, $V_{CTL(L)}$=0V)



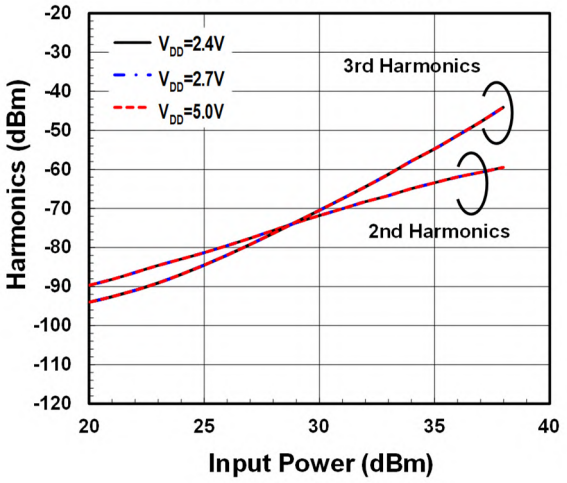
Harmonics vs. Input Power

(f=2700MHz, P2-P3 ON, $V_{CTL(L)}$=0V)



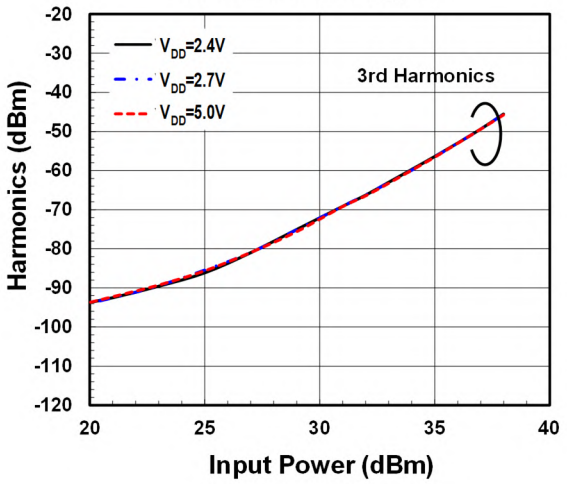
Harmonics vs. Input Power

(f=786.5MHz, P2-P3 ON, $V_{CTL(L)}$=0V)



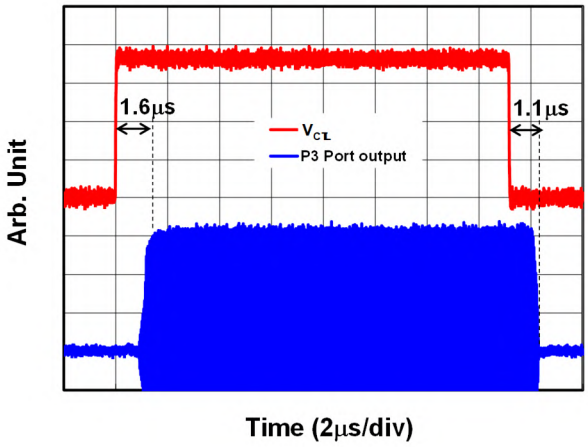
Harmonics vs. Input Power

(f=710MHz, P2-P3 ON, $V_{CTL(L)}$=0V)

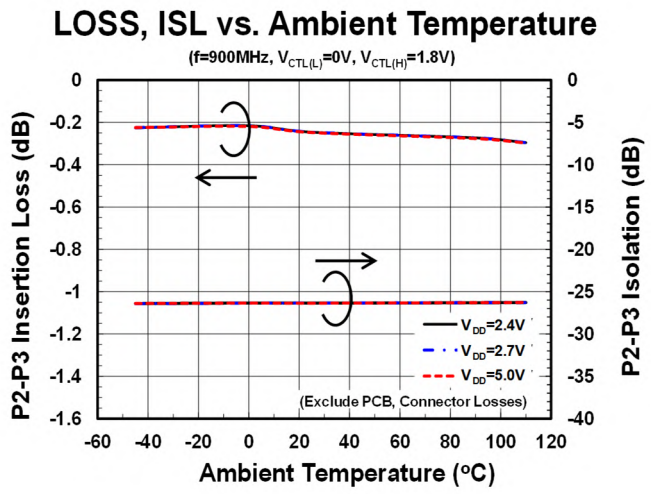


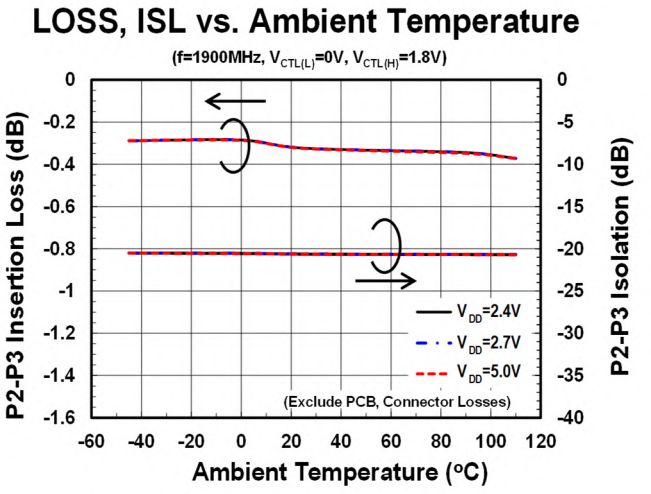
Switching time

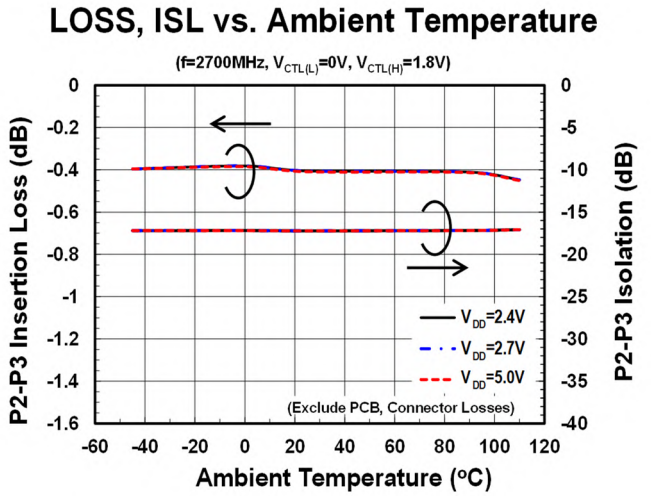
(V_{DD}=2.7V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V, P1 Port input)

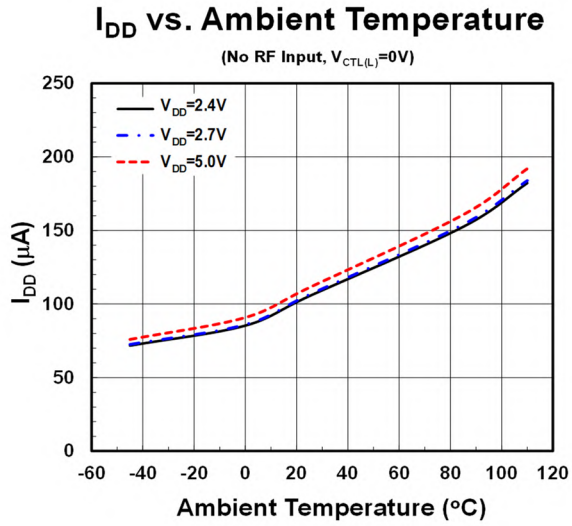


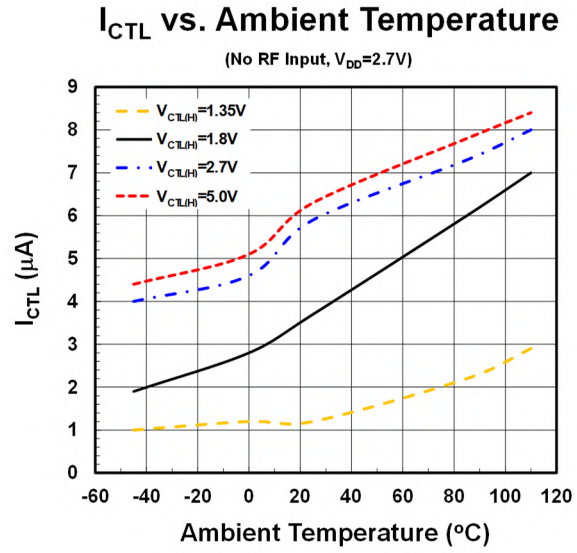
■ **ELECTRICAL CHARACTERISTICS** (With application circuit, loss of external circuit are excluded.)

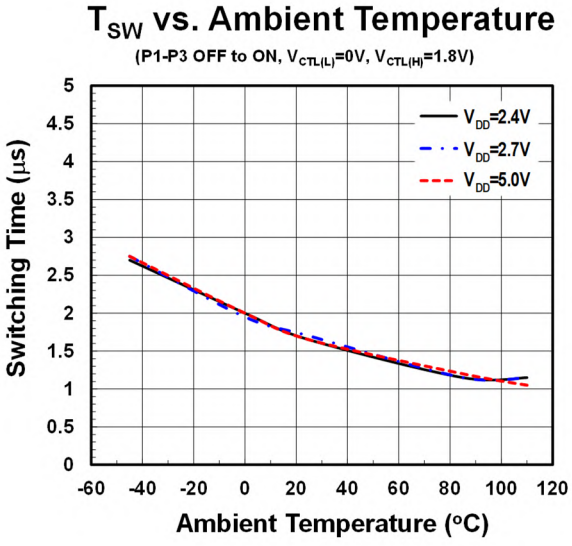






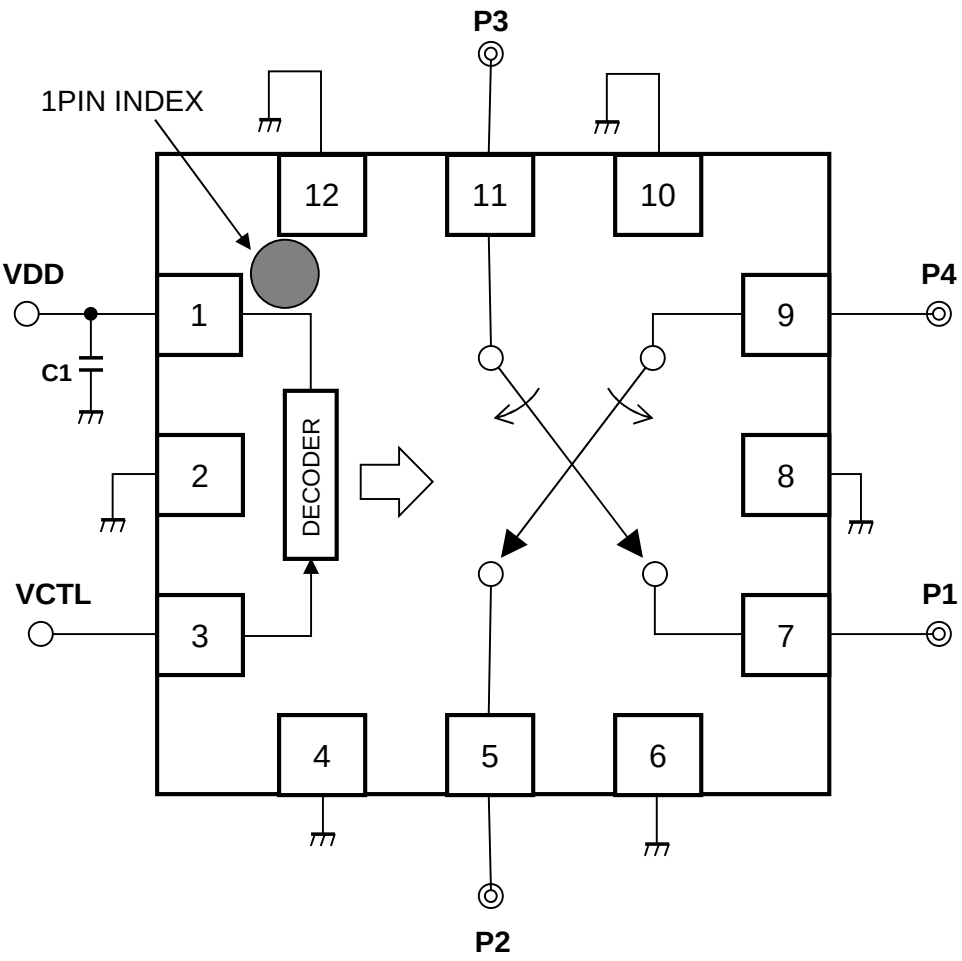






■ APPLICATION CIRCUIT

(Top view)

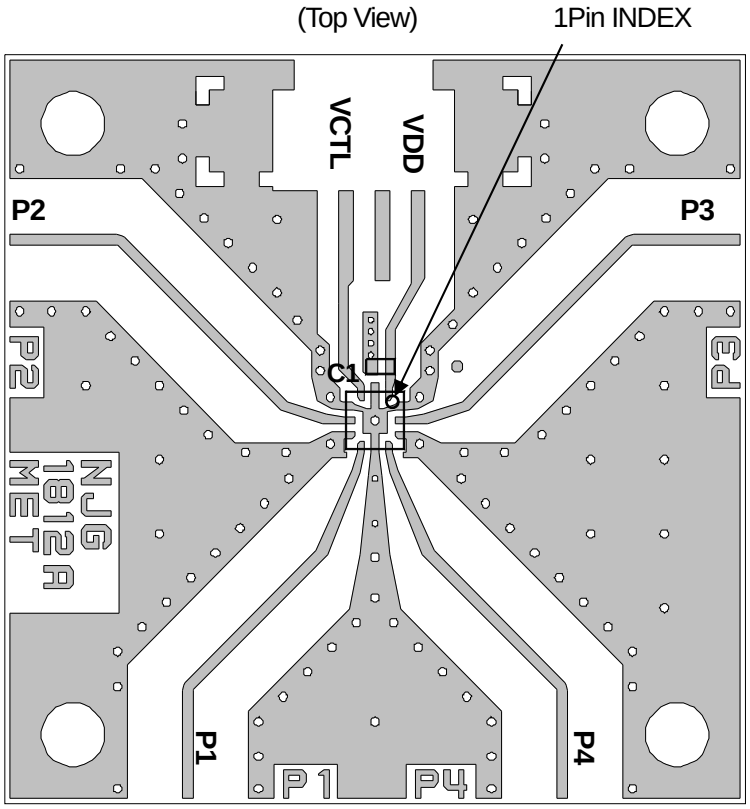


Note:
No DC blocking capacitors are required on all RF ports, unless DC is biased externally.

■ PARTS LIST

Part ID	Value	Notes
C1	1000 pF	MURATA (GRM15)

■ EVALUATION BOARD

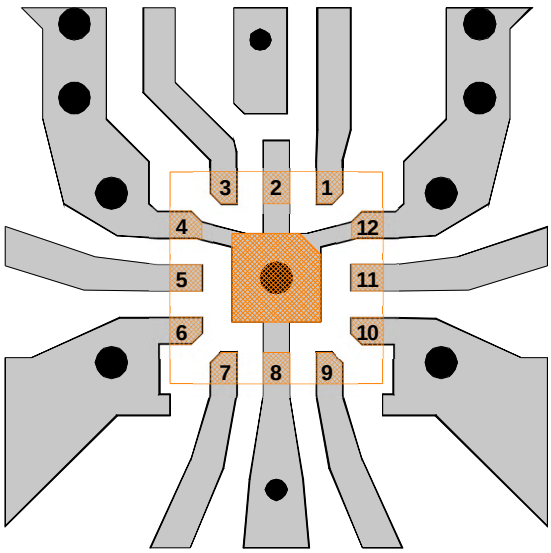


PCB (FR-4):
t = 0.2 mm
MICROSTRIP LINE WIDTH = 0.37 mm (Z_0 = 50 Ω)
PCB SIZE = 26 mm x 26 mm

Losses of PCB and connectors, Ta = +25°C

Frequency [GHz]	Loss [dB]
0.9	0.23
1.9	0.43
2.7	0.55

■ PCB LAYOUT GUIDELINE (EQFN12-ET)



PCB
PKG terminal
PKG outline
Ground via hole
Diameter Φ = 0.3 mm
Ground via hole
Diameter Φ = 0.2 mm

PRECAUTIONS

[1] For avoiding the degradation of RF performance, the bypass capacitor (C1) should be placed as close as possible to VDD terminal

[2] For good RF performance, all GND terminals are must be connected to PCB ground plane of substrate, and through - holes for GND should be placed near the IC.

[3] Please connect Exposed PAD to PCB ground plane of substrate, and through - holes for ground should be placed under the IC.

■ HANDLING PRECAUTIONS

PIN NO.	SYMBOL	ESD RATINGS			
		Human Body Model(3)			Charged Device Model(4)
Common terminal		Ground	VDD	I/O	
1	VDD	Class 2	COM.	-	Class C6
2	GND	COM.	Class 2	-	Class C6
3	VCTL	Class 2	Class 1C	Class 1C	Class C6
4	GND	COM.	Class 1C	-	Class C6
5	P2	Class 2	Class 1A	Class 2	Class C6
6	GND	COM.	Class 1A	-	Class C6
7	P1	Class 2	Class 1B	Class 2	Class C6
8	NC(GND)	COM.	Class 2	-	Class C6
9	P4	Class 2	Class 1C	Class 2	Class C6
10	NC(GND)	COM.	Class 1C	-	Class C6
11	P3	Class 2	Class 1B	Class 2	Class C6
12	GND	COM.	Class 1C	-	Class C6

(3): According to JEDEC JS-001
(4): According to JEDEC JS-002

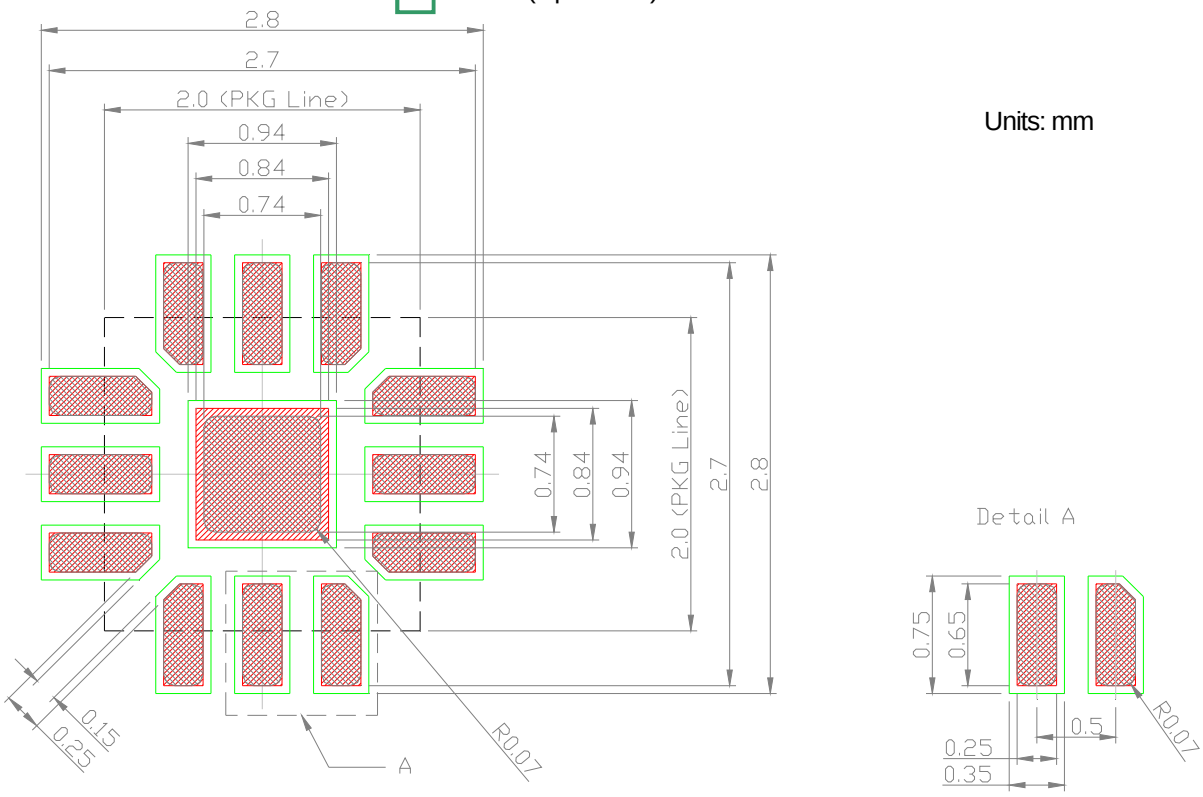
CAUTION: This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.

■ RECOMMENDED FOOTPRINT PATTERN (EQFN12-ET PACKAGE) <Reference>

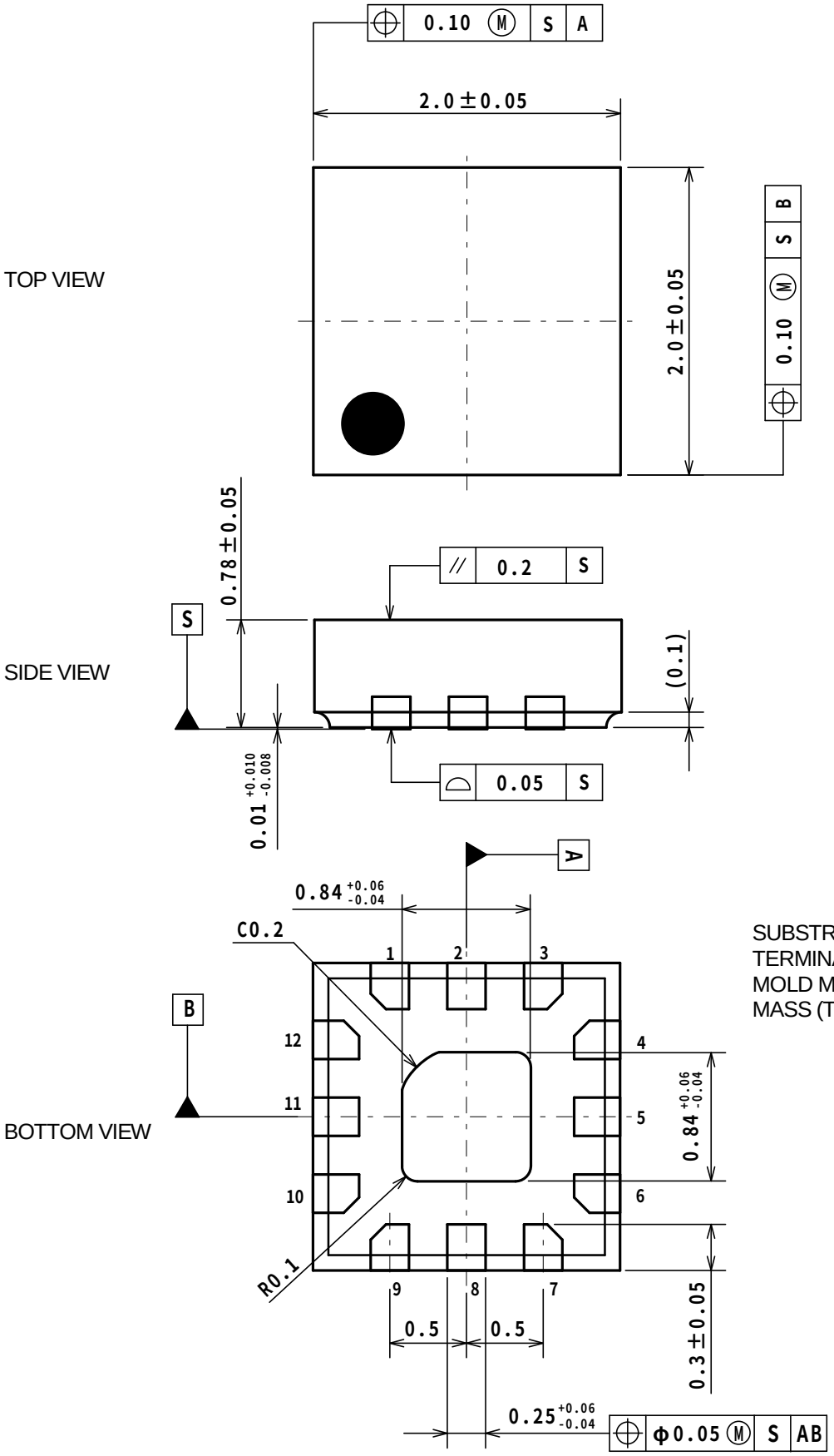
Package: 2.0 mm x 2.0 mm
Pin pitch: 0.5 mm

: Land
: Mask (Open area) *Metal mask thickness : 100 μm
: Resist(Open area)

Units: mm



■PACKAGE OUTLINE (EQFN12-ET)



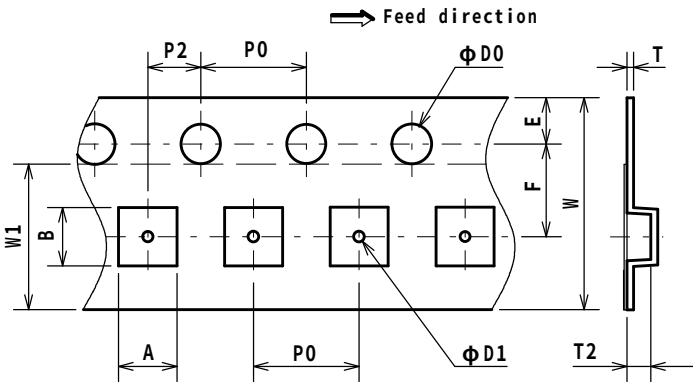
SUBSTRATE MATERIAL: Copper
TERMINAL FINISH: Sn-Bi plating
MOLD MATERIAL: Epoxy resin
MASS (TYP.): 8.5 mg

Unit: mm

■ PACKING SPECIFICATION (EQFN12-ET)

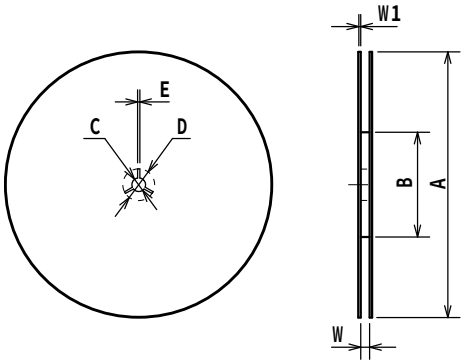
TAPING DIMENSIONS

UNIT: mm



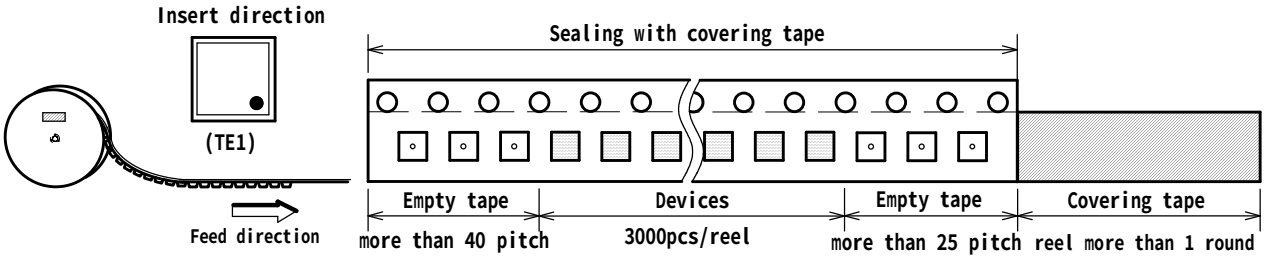
SYMBOL	DIMENSION	REMARKS
A	2.26±0.05	BOTTOM DIMENSION
B	2.26±0.05	BOTTOM DIMENSION
D0	$1.5^{+0.1}_{0}$	
D1	$0.5^{+0.1}_{0}$	
E	1.75±0.1	
F	3.5±0.05	
P0	4.0±0.1	
P1	4.0±0.1	
P2	2.0±0.05	
T	0.25±0.05	
T2	0.95±0.05	
W	$8.0^{+0.3}_{-0.1}$	
W1	5.5	THICKNESS 0.1max

REEL DIMENSIONS

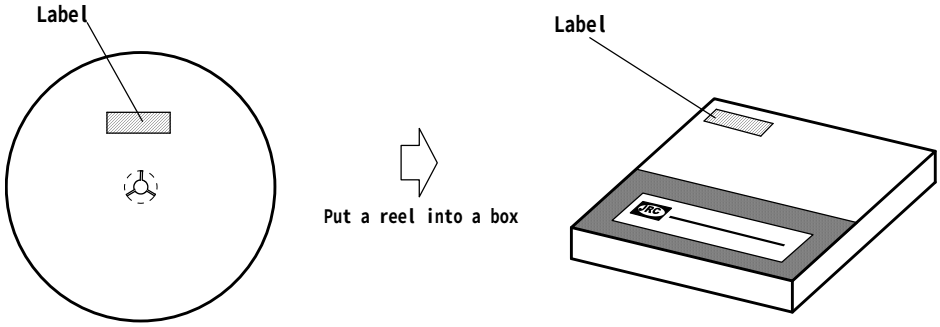


SYMBOL	DIMENSION
A	$\phi 180^{0}_{-1.5}$
B	$\phi 60^{+1}_{0}$
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	9^{+1}_{0}
W1	1.2

TAPING STATE



PACKING STATE



■ **REVISION HISTORY**

Date	Revision	Changes
5.Nov.2021	Ver.1.2	Revised RECOMMENDED FOOTPRINT PATTERN
15.Oct.2021	Ver.1.1	Revised FEATURES Revised TRUTH TABLE Revised ELECTRICAL CHARACTERISTICS (No change for spec values) Revised EVALUATION BOARD (added 1 pin index mark) Revised PCB LAYOUT GUIDELINE Revised CAUTION
20.Aug.2020	Ver.1.0	New Release

[CAUTION]

1. NJR strives to produce reliable and high quality semiconductors. NJR's semiconductors are intended for specific applications and require proper maintenance and handling. To enhance the performance and service of NJR's semiconductors, the devices, machinery or equipment into which they are integrated should undergo preventative maintenance and inspection at regularly scheduled intervals. Failure to properly maintain equipment and machinery incorporating these products can result in catastrophic system failures

2. The specifications on this datasheet are only given for information without any guarantee as regards either mistakes or omissions. The application circuits in this datasheet are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial property rights.
   All other trademarks mentioned herein are the property of their respective companies.

3. To ensure the highest levels of reliability, NJR products must always be properly handled.
   The introduction of external contaminants (e.g. dust, oil or cosmetics) can result in failures of semiconductor products.

4. NJR offers a variety of semiconductor products intended for particular applications. It is important that you select the proper component for your intended application. You may contact NJR's Sale's Office if you are uncertain about the products listed in this datasheet.

5. Special care is required in designing devices, machinery or equipment which demand high levels of reliability. This is particularly important when designing critical components or systems whose failure can foreseeably result in situations that could adversely affect health or safety. In designing such critical devices, equipment or machinery, careful consideration should be given to amongst other things, their safety design, fail-safe design, back-up and redundancy systems, and diffusion design.

6. The products listed in this datasheet may not be appropriate for use in certain equipment where reliability is critical or where the products may be subjected to extreme conditions. You should consult our sales office before using the products in any of the following types of equipment.

   - Aerospace Equipment
   - Equipment Used in the Deep Sea
   - Power Generator Control Equipment (Nuclear, steam, hydraulic, etc.)
   - Life Maintenance Medical Equipment
   - Fire Alarms / Intruder Detectors
   - Vehicle Control Equipment (Airplane, railroad, ship, etc.)
   - Various Safety Devices

7. NJR's products have been designed and tested to function within controlled environmental conditions. Do not use products under conditions that deviate from methods or applications specified in this datasheet. Failure to employ the products in the proper applications can lead to deterioration, destruction or failure of the products. NJR shall not be responsible for any bodily injury, fires or accident, property damage or any consequential damages resulting from misuse or misapplication of the products. The products are sold without warranty of any kind, either express or implied, including but not limited to any implied warranty of merchantability or fitness for a particular purpose.

8. Warning for handling Gallium and Arsenic (GaAs) Products (Applying to GaAs MMIC, Photo Reflector). These products use Gallium (Ga) and Arsenic (As) which are specified as poisonous chemicals by law. For the prevention of a hazard, do not burn, destroy, or process chemically to make them as gas or power. When the product is disposed of, please follow the related regulation and do not mix this with general industrial waste or household waste.

9. The product specifications and descriptions listed in this datasheet are subject to change at any time, without notice.